Positive Temperature Coefficient of Impact Ionization in Strained-Si

Niamh S. Waldron, *Student Member, IEEE*, Arthur J. Pitera, Minjoo L. Lee, Eugene A. Fitzgerald, *Member, IEEE*, and Jesús A. del Alamo, *Senior Member, IEEE*

***Abstract*—We have experimentally studied impact ionization (II) in the strained-Si layer of a strained-Si/SiGe heterostructure. Our key finding is that the impact ionization multiplication coefficient has a *positive* temperature coefficient which is opposite to that of bulk Si. Furthermore, the temperature dependence of the multiplication coefficient has been found to be exponential in nature. Our experimental work shows that the combination of a strong and positive temperature dependence of the II coefficient and the significant self-heating that this structure suffers from results in an overall impact ionization rate that is more than an order of magnitude higher than that of reference Si devices operating under identical bias conditions.**

***Index Terms*—Impact ionization, self-heating, strained-Si.**

I. Introduction

STRAINED-SI technology holds great promise in the continuing drive to push CMOS along the scaling roadmap [1]. Currently, research in this area is mainly focused on its use for digital or logic applications. However, as with all CMOS generations, there will eventually be strong interest in mixed-signal applications such as for wireless communication products. At this time, little is known about the potential of strained-Si technology for the high-frequency power amplifier function. For this, impact ionization (II) is a key consideration because it ultimately determines the breakdown voltage and by extension the maximum power that a technology can deliver. II is also a significant consideration in device design for most other applications as it greatly affects device reliability, substrate noise, and latchup performance.

In this paper, we present the first experimental study of II that we know of in this material system. A key finding is that II in the strained-Si/SiGe system is more than an order of magnitude higher than that of bulk Si under identical operating conditions. We have found that this is the result of the interplay between the severe self-heating that occurs as a result of the low thermal conductivity of the SiGe buffer coupled with a strong *positive* temperature dependence of II in the strained-Si layer. Our findings cast a cloud over the radio-frequency (RF) power potential of strained-Si/SiGe heterostructures. This paper contains an augmented version of an earlier presentation [2].

Manuscript received December 20, 2004; revised March 29, 2005. This work was supported by the Defense Research Advanced Projects Agency (DARPA). The review of this paper was arranged by Editor J. N. Burghartz.

The authors are with the Massachusetts Institute of Technology, Cambridge, MA 02139 USA.

Digital Object Identifier 10.1109/TED.2005.850620

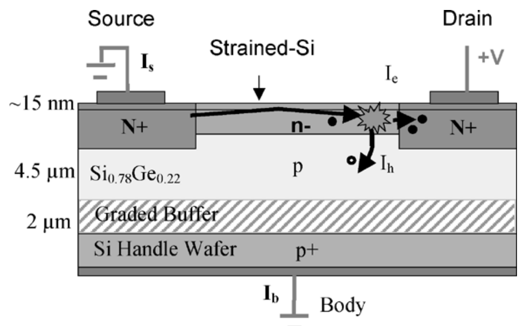

Fig. 1. Schematic cross section of the II test structure used in this paper. The hole current (I_h) produced by II in the n- region is collected by the body.

II. Test Structure Design

Our device choice for investigating II effects in the strained-Si/SiGe heterostructure is essentially an integrated resistor with a body contact on the back side of the wafer (Fig. 1). The heterostructure was grown by ultrahigh voltage chemical vapor deposition (UHVCVD) on a p+ (boron doped 10^{19} cm^{-3}) Si handle wafer. It is comprised of a 2-μm compositionally graded buffer followed by a 4-μm relaxed p-type $Si_{0.78}Ge_{0.22}$ layer and a 15-nm strained-Si layer on top. After the growth of the graded buffer layer, the samples received a chemical–mechanical polish prior to the growth of the compositional layer for the purpose of reducing surface roughness [3] thereby obtaining a smooth interface upon subsequent oxide growth. The uniform composition $Si_{0.78}Ge_{0.22}$ layer thickness and doping (2×10^{16} cm^{-3}) were chosen to prevent the n+ depletion region associated with the n+/p junctions reaching the dislocations in the graded region and causing unwanted junction leakage current. The device active area was defined by an low temperatur oxide (LTO) deposition and etch. This was followed by surface passivation using a 4-nm thermal oxide grown at 800 °C for 30 min. The active areas were then implanted with 1×10^{13} cm^{-2} 20 keV As to form the n- resistor region. Contact regions were given a high dose As 5×10^{15} cm^{-2} 20 keV implant. The process was completed by LTO deposition, an rapid thermal anneal (RTA) spike anneal at 1000 °C, contact cuts, and metallization (Ti/Al). The final resistor length is 1 μm. Bulk Si samples were simultaneously processed as a reference. The starting material of the reference bulk Si was p epi on p+ with the thickness and doping of the epi layer set to match that of the strained-Si/SiGe samples.

The resistor resembles the n- drift region of a power laterally diffused MOSFET (LD-MOSFET) if it were implemented in this technology [4]. In this device, parallel current conduction

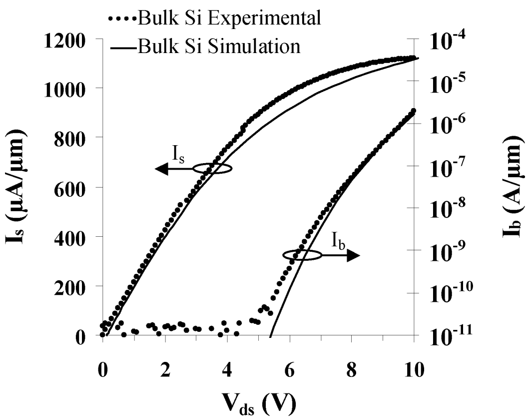

Fig. 2. MEDICI simulation of the bulk Si reference test structure. The close match of the simulated and experimental data indicates that the body current is a clean measurement of II in the test structure and that surface effects do not play a significant role.

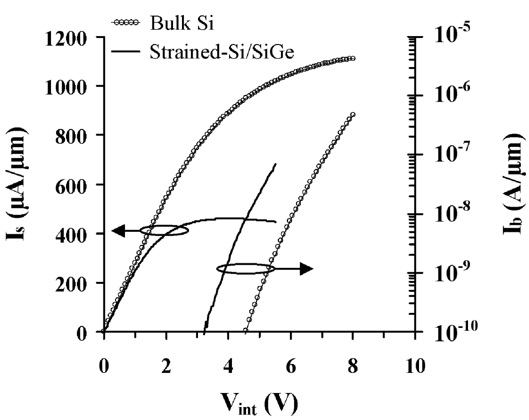

Fig. 3. Source and body current for the strained-Si/SiGe and bulk Si test structures as a function of the intrinsic voltage (V_{int}).

would take place through the strained-Si layer and the underlying SiGe buffer layer. This is, therefore, the proper structure to study II for RF power applications. This test structure is operated with a voltage applied across the two n+ contacts referred to here as drain and source. The body is kept at ground. At high enough voltages, the lateral electric field across the n- region results in II events. Any generated holes are collected by the body and extracted as body current. As we will show in this paper, impact ionization takes place preferentially in the strained-Si layer of this heterostructure.

III. Results

Fig. 2 graphs the current–voltage (*I*–*V*) characteristics of the bulk Si reference resistor taken at 300 K. This figure shows source current (I_s) and body current (I_b) as a function of the drain/source voltage across the n- region (V_{ds}). The source current has a typical shape indicative of velocity saturation. The body current is nearly exponentially dependent on V_{ds}. MEDICI simulations of the bulk Si reference sample (also shown in Fig. 2) confirm that in this test structure design, the body current is a clean measurement of II and that surface effects do not play a significant role.

I–V characteristics of a strained-Si/SiGe resistor taken at 300 K are shown in Fig. 3. The data obtained from the identical

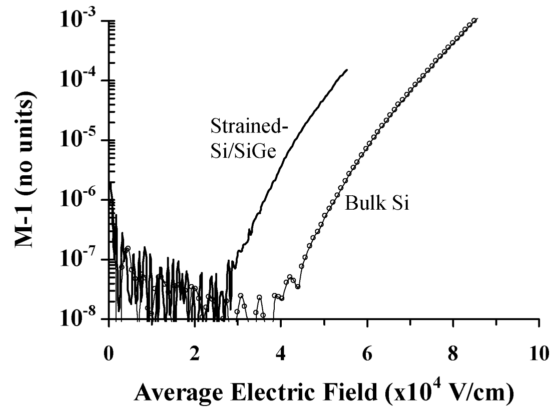

Fig. 4. $M-1$ versus average lateral electric field for the strained-Si/SiGe and bulk Si test structures.

bulk Si reference structure are shown for reference. This graph now shows I_s and I_b as a function of the intrinsic drain-source voltage across the n- region (V_{int}) This has been corrected from the applied drain-to-source voltage to account for the parasitic resistances of the n+ regions and contacts. These parasitic resistances were measured using suitable Kelvin test structures. Under identical conditions, the strained-Si samples exhibit a lower high-field source current than the bulk samples. In contrast, the body current is more than one order of magnitude higher. The strained-Si/SiGe sample also shows visible negative output conductance indicating the presence of significant self-heating.

The lower high-field source current of the Si/SiGe sample was found to partially arise from both self-heating and the lower mobility of the underlying SiGe buffer region [5]. The lower mobility of the SiGe region results in the current preferentially flowing through the high-mobility strained-Si layer resulting in effectively a thinner resistor compared to the bulk Si sample.

The higher body current of the strained-Si sample is indicative of higher impact ionization rate as measured by the II multiplication coefficient. This is extracted as

$$M-1=\frac{I_b}{I_s} \tag{1}$$

where $M-1$ is a useful figure of merit to gauge the extra current generated by II. Fig. 4 plots $M-1$ for the two devices as a function of the average lateral electric field in the n- layer (E_{avg}). As seen in this figure, for the same E_{avg}, $M-1$ in the strained-Si/SiGe devices is close to two orders of magnitude higher than in the bulk Si sample.

Further evidence of enhanced II in the strained-Si/SiGe samples is the breakdown voltage of the resistor structure. This is seen in Fig. 5 which shows that the strained-Si/SiGe heterostructure device has a breakdown voltage nearly 4 V lower than the bulk Si sample. In order to ensure repeatable measurements of II current for all conditions, the maximum voltage applied to the devices was kept well below the breakdown voltage. The body current was found not to change with the body voltage (V_{bs}), and all measurements shown are for $V_{\mathrm{bs}}=0$ V.

Figs. 6–8 show, respectively, the temperature dependence of the source and body currents and the multiplication coefficient

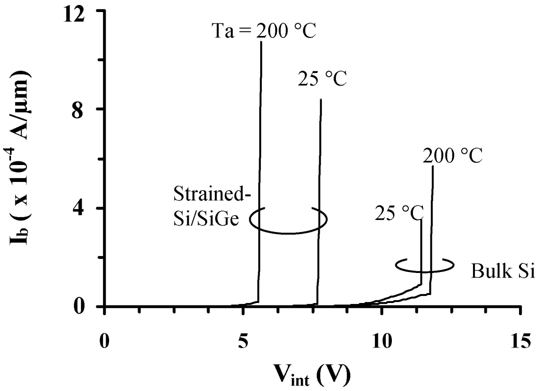

Fig. 5. I_b versus V_{int} for the strained-Si/SiGe and bulk Si samples biased to breakdown. The strained-Si/SiGe test structure has a much sharper breakdown than bulk Si and also breaks down about 4 V earlier when compared to room temperature. At 200 °C, the breakdown voltage of the bulk Si samples increases slightly but decreases by 2 V for the strained-Si/SiGe samples.

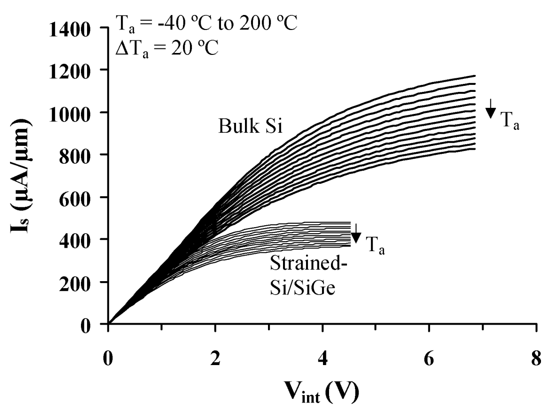

Fig. 6. I_s versus V_{int} for the range of ambient temperatures between −40 °C and 200 °C. $\downarrow T_a$ indicates the direction in which the temperature is increasing. As expected, both the strained-Si/SiGe and bulk Si samples show reduced current for increasing temperature indicating enhanced phonon scattering.

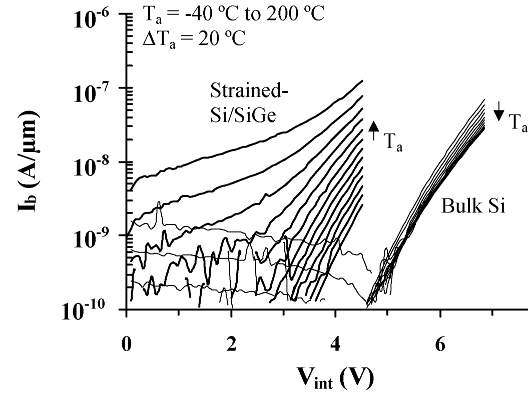

Fig. 7. I_b versus V_{int} for the range of ambient temperatures between −40 °C and 200 °C. The strained-Si/SiGe sample exhibits a strong positive temperature dependence in contrast to bulk Si, which has a much weaker and negative temperature dependence. Leakage current in both structures increases at higher temperatures.

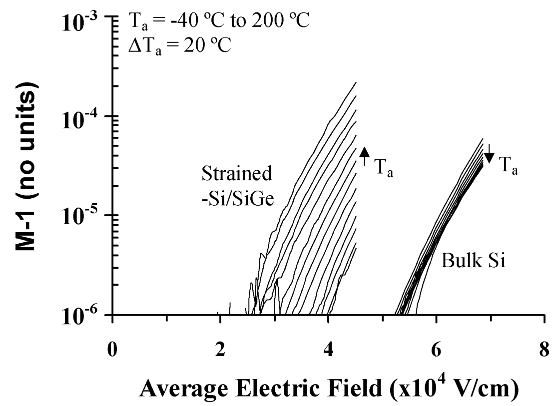

Fig. 8. Experimentally determined $M-1$ for a range of ambient temperatures between −40 °C and 200 °C. The leakage current seen at higher temperatures in Fig. 7 was factored out of I_b before the $M-1$ extraction was made. The positive temperature coefficient of II in the strained-Si/SiGe is evident and contrasts with the small but negative TC of the bulk Si reference sample.

for both structures. In both devices, the high-field source current decreases with increasing temperature (Fig. 6) indicating enhanced phonon scattering at elevated temperatures. In contrast with this the body current in the strained-Si/SiGe sample exhibits a strong positive dependence on temperature, which is opposite to what is seen in bulk Si (Figs. 7 and 8). This translates into a multiplication coefficient that increases with the temperature in the case of the strained-Si/SiGe heterostructure while that of the bulk Si structure decreases with temperature, as commonly observed [6] (Fig. 8). The positive temperature dependence of II is also apparent in the breakdown characteristics of the devices depicted in Fig. 5. At 200 °C the breakdown voltage of the strained-Si/SiGe devices decreases by 2 V from its room temperature value; whereas, it increases by 0.3 V for the bulk Si samples (Fig. 5).

In order to make a proper comparison of II in the strained-Si/SiGe heterostructure and bulk Si, self-heating needs to be accounted for. Toward this end, we have carried out pulsed measurements of the I–V characteristics (Fig. 9) at different ambient temperatures. A schematic diagram of the setup is shown in Fig. 9. A pulse generator was applied to the drain of the device. The source was connected to ground through a 50 ohm resistor. The current through the resistor was obtained from the

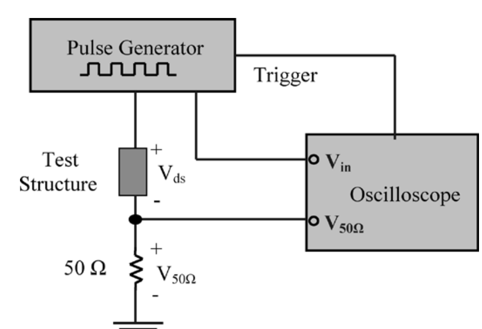

Fig. 9. Schematic of the pulse setup used to measure self-heating effects in the strained-Si/SiGe test structures.

source voltage. The slope of the line constructed from the intersection points of the pulsed I–V curves with the static curve (Fig. 10) versus the static power yields the thermal resistance of the sample. A nominal pulsewidth of 20 ns with a duty cycle of 0.02% was used. However, the frequency response of the pulse setup was limited by parasitic capacitance of the device pads. To account for this the thermal resistance was estimated for a number of different pulse widths.

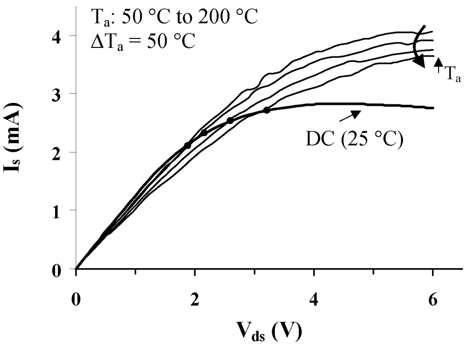

Fig. 10. Comparison of the pulsed I–V curves of the strained-Si/SiGe measured at 50 °C, 100 °C, 150 °C, and 200 °C to the static curve measured at 25 °C.

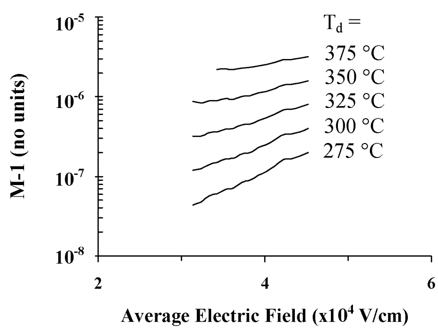

Fig. 11. II isotherms for strained-Si/SiGe structure reconstructed from static dc curves measured at ambient temperatures from −40 °C to 200 °C. Curves have been labeled with estimated device temperature ($T_{\rm d}$).

Using this method, the thermal resistance of these devices was estimated to be $170(+/-40)$ μm· K/mW. Test structures with a thinner $Si_{0.78}Ge_{0.22}$ layer of 2 μm were also fabricated and the same level of self-heating was observed in these samples. These results suggest that for our thick buffer layers, the main heat losses take place through the wafer's top surface. Our estimate of the thermal resistance compares reasonably well to the value of 122 μm· K/mW found by Jenkins for a 1.5-μm buffer [7]. In our experiments, the power levels are such that large temperature increases take place. A device operating at an ambient temperature of 25 °C can rise up to over 400 °C at reasonable bias points.

Using the extracted value of thermal resistance, II isotherms can be reconstructed from the static dc measurements taken over a wide range of temperatures (Fig. 11). Correcting for the self-heating still results in a positive temperature coefficient of impact ionization.

The I–V characteristics of the resistor structure shown so far cannot alone be used to determine if the positive temperature coefficient of II is due to impact ionization in the strained-Si or in the SiGe layer. To identify this, we examined the breakdown of the n+ source and drain/p-body junction of the resistor structure. This junction is mainly contained in the SiGe layer whereas transport in the resistor is predominantly in the strained Si layer. The source and drain terminals were held at ground and a negative bias applied to the body. As shown in Fig. 12, increasing the temperature increases the breakdown voltage of the junction

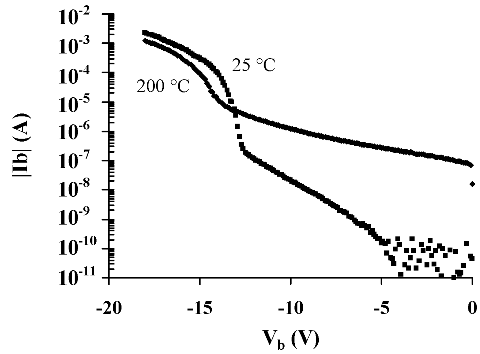

Fig. 12. Breakdown characteristics of the n+ source and drain/p-body junction at 25 °C and 200 °C. The junction exhibits a negative TC_{II} as the breakdown voltage increases with temperature. As the junction is mainly contained in the SiGe layer this implies that the positive TC_{II} observed in the resistors originates in the strained-Si layer.

which is indicative of a negative temperature coefficient for impact ionization. This result implies that the positive temperature coefficient of impact ionization that is observed in lateral transport in the resistors is indeed due to the strained-Si layer.

IV. Discussion

II in SiGe has previously been experimentally studied by means of photodiodes [8]. Theoretical Monte Carlo simulations of II in strained-Si have also been carried out [9]. Both studies show an increase in the impact ionization coefficient over that of bulk Si. However, to our knowledge, a positive temperature coefficient (TC) for II has not been predicted for strained-Si. Nonetheless, this is not an entirely surprising result. The same anomalous temperature dependence has previously been observed in the $In_xGa_{1-x}As$ system [10]. The temperature coefficient of II in this material system changes from being negative for GaAs ($x=0$) to becoming positive for InAs ($x=1$) at a composition around $x = 0.4$. This is now understood to reflect a competition between the temperature dependence of the mean-free path and that of the energy bandgap which exhibit opposing dependences [11].

To better understand how these parameters affect the ionization rate, it is instructive to examine a simple first order model for impact ionization. The model we use is based on the Chynoweth formula [12]

$$\alpha(E) = a\exp\left(\frac{-b}{\varepsilon}\right) \tag{2}$$

where α is the impact ionization coefficient, ε the lateral electric field, and a, b fitting parameters. Shockley [13] gave physical meaning to the fitting parameter b in his lucky electron model where

$$b = \frac{E_i(T)}{q\lambda(T)} \tag{3}$$

and E_i is the threshold energy for ionization and λ the mean-free path. For bulk silicon, the mean-free path has been given by Crowell and Sze [14] as

$$\lambda(T) = \lambda_0 \tanh\left(\frac{E_p}{2kT}\right) \tag{4}$$

where E_p is the optical phonon energy and λ_0 is the high-energy low-temperature asymptotic value of the phonon mean-free path. Using the values taken from Sze [15] of 0.063 eV and 76 Å for E_p and λ_0 respectively, $\lambda = 64$ Å at room temperature. The threshold energy has been modeled by Erschov and Ryzhii [16] where they assume that E_i is proportional to the bandgap energy of silicon, which depends on temperature, giving

$$E_i(T) = C_1 + C_2 T + C_3 T^2 \tag{5}$$

where $C_1 = 1.1785$ eV, $C_2 = -9.025 \times 10^{-5}$ eV K^{-1}, and $C_3 = -3.05 \times 10^{-7}$ eV K^{-2} for $T > 170$ K. At room temperature, this gives $E_i = 1.12$ eV which is the bandgap $E_{\rm g}$.

From (2) and (3), it can be seen that the probability of an ionization event increases as E_g decreases because a carrier needs less kinetic energy to cause an II event. As λ increases, the probability of an II event also increases because the carrier has gained more energy between scattering events.

The temperature dependence of the ionization rate can be determined by examining the temperature coefficient of II ($\mathrm{TC_{II}}$) defined as

$$\mathrm{TC_{II}} \equiv \frac{1}{\alpha}\frac{d\alpha}{dT} \tag{6}$$

which when applied to (2) and (3) yields

$$\mathrm{TC_{II}} = \frac{E_i}{q\varepsilon\lambda}\left(\frac{1}{\lambda}\frac{d\lambda}{dT} - \frac{1}{E_i}\frac{dE_i}{dT}\right). \tag{7}$$

Using (4) and (5), we get

$$\frac{d\lambda}{dT} = -\lambda_0 \frac{E_p}{2kT^2}\mathrm{sech}^2\left(\frac{E_p}{2kT}\right) \tag{8}$$

and

$$\frac{dE_i}{dT} = C_2 + 2C_3 T. \tag{9}$$

Both (8) and (9) are negative and work in opposition to each other. Whether the $\mathrm{TC_{II}}$ is positive or negative depends on the relative magnitude of the two bracketed terms in (7). If the $(1/\lambda)(d\lambda/dT)$ term is larger than the $(1/E_i)(dE_i/dT)$ then $\mathrm{TC_{II}}$ is negative and *vice versa* for a positive $\mathrm{TC_{II}}$. In the case of bulk Si at room temperature this analysis yields a negative value for the $\mathrm{TC_{II}}$ of

$$\mathrm{TC_{II}} = -\frac{1}{\varepsilon} 2077\ \mathrm{V \cdot cm^{-1} \cdot K^{-1}} \tag{10}$$

at 300 K. Fig. 13 shows II plotted as a function of device temperature for constant average electric field, and it can indeed be seen that the bulk Si sample has a negative dependence on temperature albeit a very weak one. This is consistent with Ershov [16] who has noted that the theoretical models tend to predict a much stronger temperature dependence of the II coefficient compared to experimental results.

In contrast to bulk Si, impact ionization in the strained-Si samples has a very strong positive and exponential dependence on temperature. The analytical expressions for the temperature

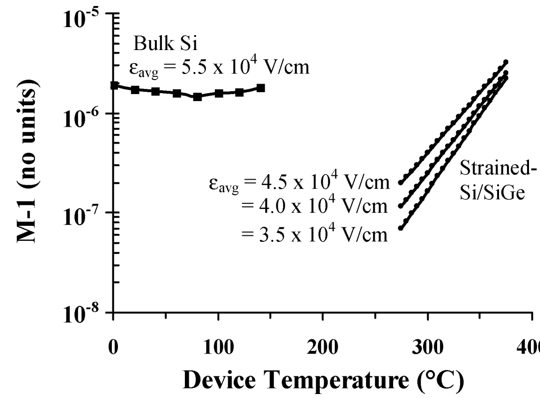

Fig. 13. Plot of II in the strained-Si/SiGe test structure at different $E_{\rm avg}$ as a function of temperature. A plot of Si data at $E_{\rm avg} = 5.5 \times 10^4$ V/cm is shown for reference. II in strained-Si/SiGe exhibits an exponential dependence on temperature.

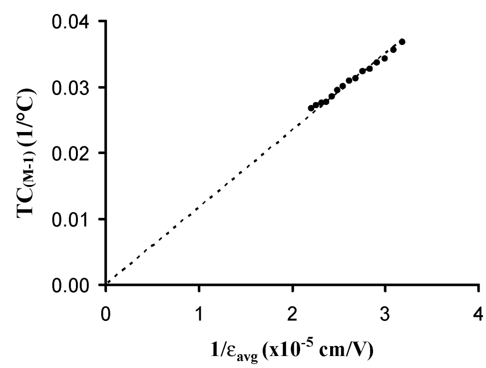

Fig. 14. Plot of $\mathrm{TC}_{(M-1)}$ versus inverse average electric field. As predicted by the model given in (7), this yields a linear dependency with an intercept that passes through the origin.

dependence of E_i and λ such as in (4) and (5) have not been formulated for strained-Si, and so a numerical estimate for $\mathrm{TC_{II}}$ cannot be made. Fig. 14 plots the temperature coefficient of $M - 1$

$$\mathrm{TC}_{(m-1)} = \frac{1}{M-1}\frac{d(M-1)}{dT} \tag{11}$$

versus $1/\varepsilon_{\rm avg}$. The temperature dependence of II shows a linear dependence on inverse field and the intercept of the graph passes through the origin which is consistent with the model presented in (7).

To have such a strong exponential positive temperature dependence, as shown in Fig. 13, implies that the normalized rate of change of the threshold energy with respect to temperature dominates over that of the mean-free path term in (7). It is conceivable that the $(1/E_i)(dE_i/dT)$ term strongly dominates over the $(1/\lambda)(d\lambda/dT)$ term as the mean-free path in strained-Si is expected to be longer and the room temperature $E_{\rm g}$ smaller [17]. dE_i/dT may also be more complicated than just simply $\sim dE_{\rm g}/dT$ because of the band splitting of the strained-Si.

A direct comparison of II in the strained-Si/SiGe and bulk Si at the same temperature and field cannot be made due to the experimental limitations of this paper. The maximum operating temperature of the measurement chuck and therefore the bulk Si samples is 200 °C. Self-heating in the strained-Si devices resulted in operating temperatures that exceeded this 200 °C limit. To reduce the operating temperature of the strained-Si samples to less than 200 °C the chuck would have to be cooled to less than its lower limit of −50°C. Self-heating also resulted in II occurring at lower fields in the strained-Si samples because of the exponential temperature dependence. At these lower fields leakage current obscured II in the bulk Si samples. An extrapolation of the temperature dependence of the II in strained-Si/SiGe would show that the II is on the same order of that in bulk Si at room temperature as predicted by Rashed [9]. However, since this is an exponential extrapolation, this estimate is highly dependent on the accuracy of the determination of the thermal resistance. Higher temperature measurements of the bulk Si or lower temperature measurements of the strained-Si samples are needed for a direct comparison to be possible.

A positive TC for II has very significant implications in device applications, particularly in RF power applications. First, as the II rate increases with temperature, high-temperature reliability at high voltages becomes a critical consideration. Second, as temperature increases, the breakdown voltage decreases and thermal runaway could occur more easily. This limits the power handling ability of the technology. The situation is more severe in the case of the strained-Si/SiGe system because of the poor thermal conductivity of the SiGe buffer. This greatly enhances the overall II rate under a given set of conditions.

V. Conclusion

We have experimentally studied electron II in the strained-Si/SiGe material system and found that the strained-Si has a positive temperature dependence. We have also shown that the temperature dependence of II in this material system is exponential in nature. When combined with severe levels of self-heating in the structure, we have demonstrated that the positive TC of II results in significantly higher levels of II being observed in strained-Si devices operating at the same ambient temperature and bias point as reference bulk Si devices.

Acknowledgment

The authors would like to thank Prof. J. Hoyt, Prof. D. Antoniadis, and J. Fiorenza for helpful discussions, and the staff at the Microelectronics Technology Laboratory, MIT for their assistance in the fabricaction of the devices.

References

[1] J. L. Hoyt, H. M. Nayfeh, S. Eguchi, I. Aberg, G. Xia, T. Drake, E. A. Fitzgerald, and D. A. Antoniadis, "Strained silicon MOSFET technology," in *IEDM Tech. Dig.*, 2002, pp. 23–26.

[2] N. S. Waldron, A. J. Pitera, M. L. Lee, E. A. Fitzgerald, and J. A. del Alamo, "Impact ionization in strained-Si/SiGe heterostructures," in *IEDM Tech. Dig.*, 2003, pp. 33.7.1–33.7.4.

[3] M. T. Currie, S. B. Samavedam, T. A. Langdo, C. W. Leitz, and E. A. Fitzgerald, "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing," *Appl. Phys. Lett.*, vol. 72, no. 14, pp. 1718–1720, Apr. 1998.

[4] J. G. Fiorenza, D. A. Antoniadis, and J. A. del Alamo, "RF power LDMOSFET on SOI," *IEEE Electron Device Lett.*, vol. 22, no. 3, pp. 139–141, Mar. 2001.

[5] M. V. Fischetti and S. E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," *J. Appl. Phys.*, vol. 80, no. 4, pp. 2234–52, Aug. 1996.

[6] W. Maes, K. de Meyer, and R. van Overstraeten, "Impact ionization in silicon: A review and update," *Solid State Electron.*, vol. 33, no. 6, pp. 705–18, Jun. 1990.

[7] K. A. Jenkins and K. Rim, "Measurement of the effect of self-heating in strained-silicon MOSFETs," *IEEE Electron Device Lett.*, vol. 23, no. 6, pp. 360–2, Jun. 2002.

[8] J. Lee, A. L. Gutierrez-Aitken, S. H. Li, and P. K. Bhattacharya, "Impact ionization coefficients in $Si_{1-x}Ge_x$," *Appl. Phys. Lett.*, vol. 66, no. 2, pp. 204–5, Jan. 1995.

[9] M. Rashed, S. Jailepalli, R. Zaman, W. Shih, T. J. T. Kwan, and C. M. Maziar, "Simulation of electron transport in strained silicon on relaxed $Si_{1-x}Ge_x$ substrates," in *Proc. University/Government/Industry Microelectronics Symp.*, 1995, pp. 168–171.

[10] D. Ritter, R. A. Hamm, A. Feygenson, and M. B. Panish, "Anomalous electric field and temperature dependence of collector multiplication in InP/$Ga_{0.47}In_{0.53}As$ heterojunction bipolar transistors," *Appl. Phys. Lett.*, vol. 60, no. 25, pp. 3150–2, Jun. 1992.

[11] A. Neviani, G. Meneghesso, E. Zanoni, M. Hafizi, and C. Canali, "Positive temperature dependence of the electron impact ionization coefficient in $In_{0.53}Ga_{0.47}As$/InP HBTs," *IEEE Electron Device Lett.*, vol. 18, no. 12, pp. 619–621, Dec. 1997.

[12] A. G. Chynoweth, "Ionization rates for electrons and holes in silicon," *Phys. Rev.*, vol. 109, no. 5, pp. 1537–1540, Mar. 1958.

[13] W. Shockley, "Problems related to p-n junctions in silicon," *Solid State Electron.*, vol. 2, no. 1, pp. 35–67, 1961.

[14] C. R. Crowell and S. M. Sze, "Temperature dependence of avalanche multiplication in semiconductors," *Appl. Phys. Lett.*, vol. 9, pp. 242–4, 1966.

[15] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1981, p. 851.

[16] M. Ershov and V. Ryzhii, "Temperature dependence of the electron impact ionization coefficient in silicon," *Semicond. Sci. Technol.*, vol. 10, no. 2, pp. 138–42, Feb. 1995.

[17] C. G. Van de Walle and R. M. Martin, "Theoretical calculations of heterojunction discontinuities in the Si/Ge system," *Phys. Rev. B, Condens. Matter*, vol. 34, pp. 5621–34, 1986.

Niamh S. Waldron (S'03) received the B.Sc. degree in applied physics from the University of Limerick, Limerick, Ireland, in 1996, and the S.M. degree in electrical engineering from the Massachusetts Institute of Technology (MIT), Cambridge, in 2002 for her work on strained-Si technology for RF power devices. She is currently pursuing the Ph.D. degree at MIT, studying InP-based HEMTs for large-scale digital circuits.

From 1996 to 2000, she was with Analog Devices Ireland, Limerick, where she specialized in ion implantation and RTA. She was also involved with the integration and development of their BiCMOS processes.

Arthur J. Pitera, photograph and biography not available at the time of publication.

Minjoo L. Lee, photograph and biography not available at the time of publication.

Eugene A. Fitzgerald (M'01) received the B.S. degree from the Massachusetts Institute of Technology (MIT), Cambridge, and the Ph.D. degree from Cornell University, Ithaca, NY, in 1985 and 1989, respectively, both in materials science and engineering.

He was a Researcher in lattice-mismatched materials and devices at AT&T Bell Laboratories from 1988 to 1994. In 1994, he became an Associate Professor, Department of Materials Science and Engineering, MIT, where he is currently a Full Professor. In 1998, he cofounded AmberWave Systems Corporation, Salem, NH. He has coauthored or authored more than 150 papers, predominately in the field of lattice-mismatched materials and devices, and he has 28 issued U.S. patents. His interests include engineered substrates and devices, in particular strained SiGe and III-V-based devices.

Dr. Fitzgerald is the recipient of the TMS 1994 Robert Lansing Hardy Medal Award. In 2000, he received a Lord Career Development Chair, and in 2003 became the Merton C. Flemings—SMA Professor of Materials Engineering. He became a Fellow in the Singapore-MIT Alliance in 1999. He is a member of APS, MRS, TMS, and ECS.

Jesús A. del Alamo (SM'00) received the degree in telecommunications from the Polytechnic University of Madrid, Madrid, Spain, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1980, 1983, and 1985, respectively. At Stanford University he carried out his Ph.D. dissertation on minority carrier transport in heavily doped silicon.

From 1977 to 1981, he was with the Institute of Solar Energy, Polytechnic University of Madrid, working on silicon solar cells. From 1985 to 1988, he was Research Engineer with Nippon Telegraph and Telephone-LSI Laboratories, Atsugi, Japan, where he conducted research on III-V heterostructure field-effect transistors. Since 1988, he has been with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology (MIT), Cambridge, where he is currently a Professor. His research interests are gigahertz power transistors, including Si LDMOS on SOI, RF power CMOS, GaAs PHEMTs, and InP HEMTs. He is also active in online laboratories for science and engineering education.

Dr. del Alamo was awarded the Baker Memorial Award for Excellence in Undergraduate Teaching at MIT in 1992. In 1993, he received the H. E. Edgerton Junior Faculty Achievement Award at MIT. In 1999, he was elected a Corresponding Member of the Royal Spanish Academy of Engineering. In 2001, he received the Louis D. Smullin Award for Excellence in Teaching and the Class of 1960 Innovation in Education Award, both at MIT. In 2002, he received the Amar Bose Award for Excellence in Teaching from MIT. In 2003, he was selected as a MacVicar Faculty Fellow at MIT. From 1991 to 1996, he was an NSF Presidential Young Investigator.