Enhancement-mode BEOL In_2O_3 FETs with Record Logic Performance: Experiments and Compact Modeling

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***Abstract*—**We demonstrate record logic performance in back-end-of-the-line (BEOL)-compatible enhancement-mode (E-mode) amorphous oxide semiconductor (AOS) field-effect transistors (FETs). These devices exhibit near-ideal scalability down to 40 nm in channel length (L_{ch}). Using an In_2O_3 channel by plasma-enhanced atomic-layer deposition (PEALD), we achieve E-mode operation in L_{ch} = 40 nm devices with a maximum drive current (I_{max}) of 1.35 mA/μm, a peak transconductance ($g_{m,peak}$) of 490 μS/μm, and a close-to-thermal-limit average room-temperature subthreshold swing (S_{avg}) of 63 mV/dec, all at a drain-to-source voltage (V_{ds}) of 0.5 V. A total source (S) and drain (D) resistance (R_{sd}) of 169 Ω.μm, record-low among E-mode AOS-FETs, is demonstrated. Capacitance-voltage (*C-V*) characteristics reveal different threshold voltages (V_t) in the intrinsic channel and in the S/D to gate (G) overlap regions. We develop a physics-based MVS-AOS model which accurately captures the essential physics at play in our experimental devices, including *C* with frequency dispersion in the S/D region. This work advances state-of-the-art BEOL AOS-FET technology, and paves the way for future design-technology co-optimization (DTCO) on this promising device platform for BEOL monolithic 3D integration.

I. Introduction

AOSs have emerged as promising channel material candidates for BEOL monolithic 3D integration, thanks to large-area low-thermal-budget processing capability, decent electron mobility (μ_e), and ultralow leakage current [1-12]. Especially, In_2O_3-channel FETs have demonstrated impressive performance [13]. However, they generally display depletion-mode (D-mode) operation with $V_t < 0$ [12-14]. Many emerging applications such as 1T1C and 2T0C embedded dynamic random-access memory (eDRAM) desire high-performance E-mode FETs to achieve long retention, fast switching, and high energy efficiency [15]. Recently, we have demonstrated E-mode BEOL FETs based on a PEALD-In_2O_3 channel [16]. This earlier work as well as that of other authors, however, suffered from relatively poor scalability. The full potential of this novel device technology and the development of a physically meaningful compact model have yet to be realized.

In this work, we have fabricated nanoscale PEALD-In_2O_3 FETs and carried out systematic *I-V* and *C-V* characterization together with compact modeling. We have achieved record logic performance among any E-mode AOS FETs [1-12] (**Fig. 1**), including record-high I_{max} = 1.35 mA/μm and $g_{m,pk}$ = 490 μS/μm at V_{ds} = 0.5 V with a near-ideal S_{avg} = 63 mV/dec and a record-low R_{sd} = 169 Ω.μm in L_{ch} = 40 nm devices. We demonstrate near-ideal L_{ch} scaling with negligible short-channel effects (SCEs) down to 40 nm, the smallest L_{ch} in this work. A compact model (MVS-AOS) has been formulated following classic drift-diffusion theory that includes quantum effects. Our model accurately captures key device operation features over the entire range of L_{ch}, including intrinsic and extrinsic *C-V* behavior, as well as bias-dependent μ_e and R_{sd}.

II. Device Fabrication

Schematic device structure and key fabrication steps are shown in **Figs. 2(a)-(b)**. We adopted a tungsten (W) gate by sputtering, a 4.8-nm-thick HfO_2 gate insulator by PEALD at 250 °C, a 2.3-nm-thick In_2O_3 channel by PEALD at 150 °C, and a Ni/Au bilayer for S/D contact. Channel isolation was done with a Cl-based reactive-ion etching (RIE) process. Our devices feature channel widths (*W*) ranging from 5 μm to 60 nm and L_{ch} ranging from 970 nm to 40 nm. **Fig. 2(c)** shows an SEM image of a representative device with L_{ch} = 40 nm.

III. Electrical Characteristics

Fig. 3 shows transfer and output characteristics of FETs with *W* = 5 μm and different L_{ch}. Linear turn-on in all the devices indicates good Ohmic contacts [**Figs. 3(d)-(f)**]. In the L_{ch} = 40 nm device [**Fig. 3(a)**], a nearly ideal S_{avg} = 63 mV/dec over three decades of drain current (I_d) is obtained at both V_{ds} = 0.05 and 0.5 V with negligible drain-induced barrier lowering (DIBL). I_{max} > 1 mA/μm is obtained at V_{ds} = 0.5 V in this device [**Fig. 3(d)**]. Remarkable S_{avg} down to the thermionic limit, 60 mV/dec, is observed over two decades of current in long-channel devices [**Fig. 3(c)**], suggesting a very high-quality metal-oxide-semiconductor (MOS) interface.

Transfer characteristics of a set of *W* = 5 μm devices with different L_{ch} in both log and linear scales at V_{ds} = 0.05 and 0.5 V are shown in **Fig. 4**. Again, for all the devices, S_{avg} approaches 60 mV/dec. The tight V_t distribution highlights the excellent electrostatic scaling in our transistors.

We have further characterized devices with different *W* down to 60 nm. **Fig. 5** shows transfer and output characteristics of a transistor with *W* = 60 nm and L_{ch} = 40 nm. In this device, I_{max} = 1.35 (1.9) mA/μm is obtained at V_{ds} = 0.5 (0.7) V together with S_{avg} = 69 mV/dec, a value limited by the instrument noise floor. **Fig. 6** shows *W* scaling leads to substantial improvement in I_{max} with a slight positive V_t shift and little S_{avg} degradation.

We have performed gated transmission line method (G-TLM) measurements for multiple values of L_{ch} and *W* (**Fig. 7**). Total resistance (R_{total}) is extracted at V_{ds} = 0.05 V and varying gate overdrive ($V_{ov} = V_{gs} - V_t$). V_t is defined at a constant 4 nA× W/L_{ch}, corresponding to 100 nA/μm @ L_{ch} = 40 nm. Examples of R_{total} vs. L_{ch} at V_{ov} = 3.8, 3.9 V are shown in **Fig. 7** where good linear dependences are demonstrated. This enables us to extract channel sheet resistance (R_{sh}) and unit-width R_{sd}. We observe a clear decrease of both R_{sd} and R_{sh} as V_{ov} increases (**Fig. 8**). This is due to an increase in μ_e as sheet carrier concentration (N_{sheet}) increases, as will be shown later. A clear decrease of R_{sd} is also seen with decreasing *W*, while R_{sh} remains nearly *W*-independent. This suggests that intrinsic channel properties (N_{sheet} and μ_e) are likely independent of *W*, while the S/D regions become more conductive in narrower devices, likely induced by mechanical strain. Further study of

strain effect is required. Remarkably, a record-low R_{sd} = 169 Ω.μm is achieved at W = 60 nm suggesting a transfer length (L_T) of ~30 nm. Such a short L_T highlights the high-performance potential in E-mode PEALD-In_2O_3 FETs with a scaled contact length.

Fig. 9 presents the scaling behavior for key figures-of-merit at V_{ds} = 0.5 V. **Fig. 9(a)** graphs g_m characteristics for L_{ch} = 40 nm devices with different W as a function of V_{ov}. At a low V_{ov} < ~0.5 V, all the curves overlap, indicating intrinsic-channel-dominated electron transport. As V_{ov} increases, g_m saturation appears first in wider devices leading to a lower $g_{m,peak}$ limited by the higher R_{sd}. We obtain a high $g_{m,peak}$ = 490 μS/μm at V_{ds} = 0.5 V in the W/L_{ch} = 60/40 nm device. **Figs. 9(b)** and **9(c)** show excellent SCE as L_{ch} scales down but a slightly positive V_t shift and a minor S_{avg} degradation as W scales down. This is attributed to the steepest slope region of the I-V characteristics not being resolved in narrow-W devices due to limited instrument resolution. The scaling of $g_{m,peak}$ [**Fig. 9(d)**] clearly demonstrates the gradual transition of channel-limited transport at long L_{ch} to R_{sd}-limited current at short L_{ch}. At L_{ch} = 970 nm, all the devices display nearly identical $g_{m,peak}$, while at L_{ch} = 40 nm, clear increase of $g_{m,peak}$ is visible as W decreases.

To understand charge-control physics, we characterized C-V behavior in W = 5 um devices, the same set as shown in **Figs. 3** and **4**. S/D were shorted during the measurements. **Fig. 10(a)** shows mild frequency dispersion of C for the L_{ch} = 970 nm device. The frequency-independent C at low V_g when the device turns on from full depletion to weak accumulation indicates a nearly trap-free MOS interface, aligning well with the observed S_{avg} = 60 mV/dec. **Fig. 10(b)** shows 50-kHz C-V curves for devices with varying L_{ch}. All the curves converge to a nearly constant C at negative bias, likely originating in the fully-depleted S/D contact regions, as well as bias-independent pad parasitics. Thanks to a nearly L_{ch}-insensitive V_t as shown in **Fig. 8(b)**, we can extract intrinsic channel C through normalized differential C (C_{diff}) between several pairs of devices with different L_{ch}. Despite unavoidable noise due to the very small C magnitude, reproducible C_{diff} results are obtained [**Fig. 10(c)**] corresponding to a capacitance equivalent thickness (CET) of ~1.4 nm. With this result, we can then study L_{ch}-independent C components. This includes a bias-dependent overlap C (C_{ov}) originating from accumulation and depletion in the S/D regions, as well as a bias-independent parasitic C (C_{par}). Taking the L_{ch} = 40 nm device as an example, we show the split of C components in **Fig. 10(d)**. Bias-dependent C_{ov} dominates in this short device. This explains the nearly saturated C-V curves in **Fig. 10(b)** when $L_{ch} \leq$ 70 nm. We have further extracted C_{ov} + C_{par} at 50 kHz and 1 MHz, showing L_{ch}-independent behavior at both frequencies [**Fig. 10(e)-(f)**]. Minor variation is due to the unavoidable process uncertainty in the fabrication. An interesting finding from this C analysis is that V_t in the S/D regions (V_{tov}) is ~0.9 V, substantially more positive than the channel V_t of ~0.1 V. Examining the frequency dispersion of C-V, we find that it is almost L_{ch}-independent in magnitude [**Fig. 10(g)**] and it suddenly appears at ~0.9 V. This strongly suggests that prominent trapping effect is taking place in the S/D regions, as opposed to the intrinsic channel.

We summarize the unique physics of our devices in **Fig. 10(h)** that suggests a lower doping level under the contacts. This observation might explain the excellent L_{ch} scaling of SCE in our devices in contrast with other Ni-contacted In_2O_3 FETs with severe V_t roll-off ascribed to oxygen-scavenging-induced heavier doping in the Ni-contacted S/D regions [17].

From the I-V and C-V characteristics, we calculate N_{sheet} by integrating C_{diff} as shown in **Fig. 11(a)**. We then extract intrinsic field-effect mobility ($\mu_{FE,i}$) using the linear-regime transfer characteristics of the W/L_{ch} =5 μm /970 nm device [**Fig. 11(b)**], obtaining a peak $\mu_{FE,i}$ of 21.5 $cm^2/(V.s)$.

IV. MVS-AOS Modeling and Device Physics

A physics-based compact model (MVS-AOS) is developed following the equivalent circuit in **Fig. 12** and key equations listed in **Fig. 13**. The basic current and charge in the intrinsic regions [Eqs. (1)-(3)] are formulated following the classic drift-diffusion theory used in [18]. Additional effects critical to AOS FETs are implemented on top of the basic model, including (i) quantum effects [19] in both channel and S/D regions, (ii) Coulomb scattering limited effective mobility, (iii) C_{ov} with frequency dispersion and (iv) bias-dependent R_{sd} and C_{ov}. In R_{sd} = 2(R_B + R_C), R_B decreases with V_{gs} due to decreasing Coulomb scattering. The frequency dispersion in C_{ov} is captured by adding r_{ov} (**Fig. 12**). A coefficient of 1.2 is used for empirically modeling the power-law V_{ov} dependence of both $\mu_{FE,i}$ and $1/R_B$.

Modeled vs. experimental I-V and C-V characteristics are shown in **Fig. 3** and **Fig. 10**, respectively. Excellent accuracy across all L_{ch} is achieved, validating that correct physics are captured. Channel current, even at L_{ch} = 40 nm, appears to be mobility-limited (rather than saturation-velocity-limited) over the range of measured V_{ds}. Our modeling results emphasize the importance of parasitic engineering in short-L_{ch} AOS-FETs.

Finally, we benchmark R_{sd} vs. V_t for short-L_{ch} AOS FETs, as well as maximum $g_{m,peak}$ achieved in each AOS material with E-mode FET operation at V_{ds} = 0.5 V (**Fig. 14**). Our devices show significant performance improvement in the on-state and exhibit the lowest R_{sd} when compared to any E-mode AOS-based FETs [1-12,14-16,20-27].

V. Conclusions

This work demonstrated an E-mode BEOL AOS-FET technology with record logic performance and excellent scalability. Our comprehensive study reveals unique physics under the contacts. An MVS-AOS compact model has been developed that accurately describes transistor behavior over the entire dimensional range. Our results should be instrumental in facilitating future high-performance AOS-FET development for BEOL monolithic 3D integration.

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References

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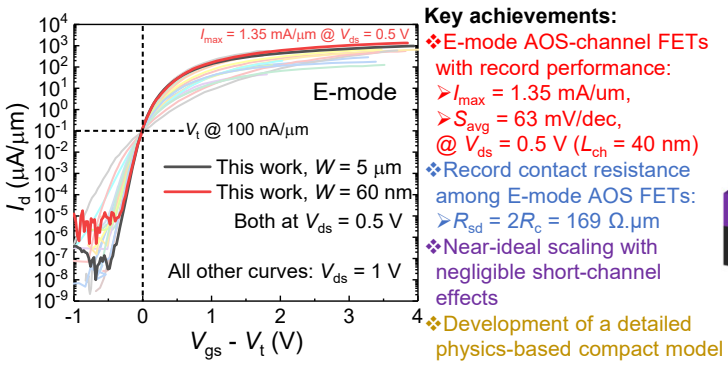


Fig. 1. Benchmarking our L_{ch} = 40 nm E-mode devices (red, black) at V_{ds} = 0.5 V against E-mode AOS FETs reported in the literature at V_{ds} = 1 V [1-12]. V_{gs} have been shifted to match 100 nA/μm at V_{gs} = 0. Our devices show highest I_{max} (even at a much reduced V_{ds}) with steepest S.

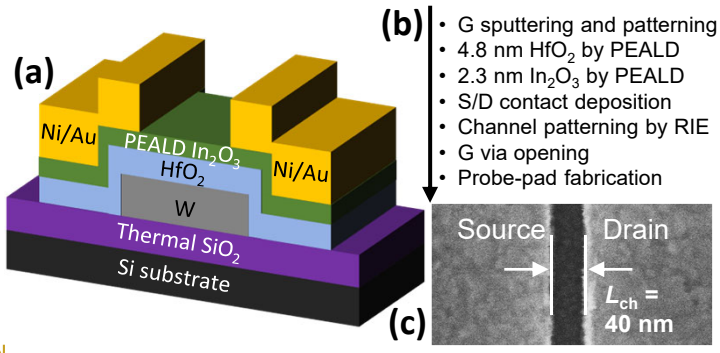


Fig. 2. (a) Schematic BEOL PEALD-In_2O_3-channel FET studied in this work. (b) Key fabrication steps. (c) Top-down SEM image from a representative W = 5 μm device showing L_{ch} = 40 nm.

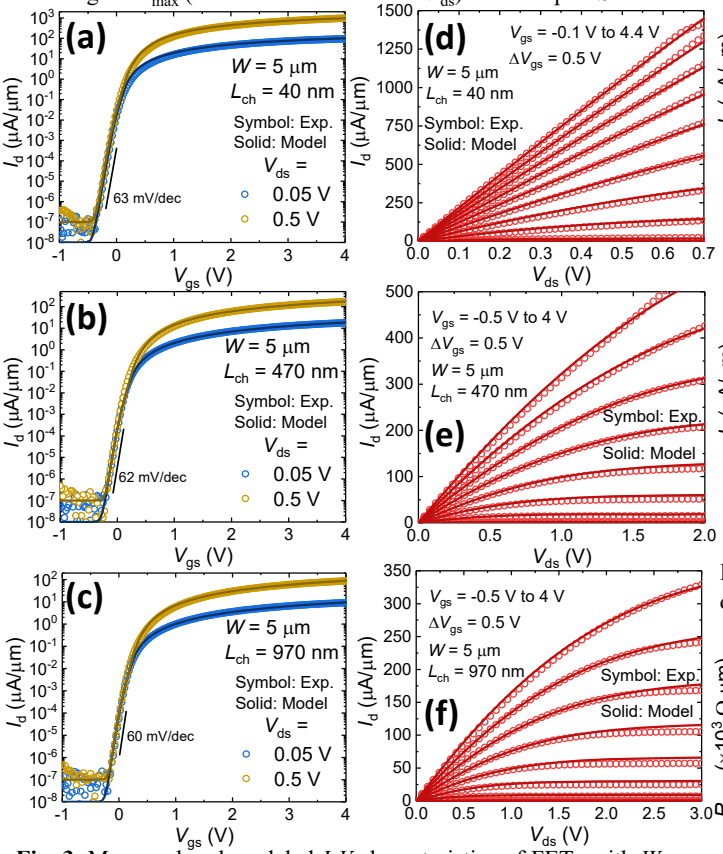


Fig. 3. Measured and modeled I-V characteristics of FETs with W = 5 μm and different L_{ch}: (a)-(c) Transfer characteristics, (d)-(f) Output characteristics. The MVS-AOS model (Section IV) shows good accuracy and scalability.

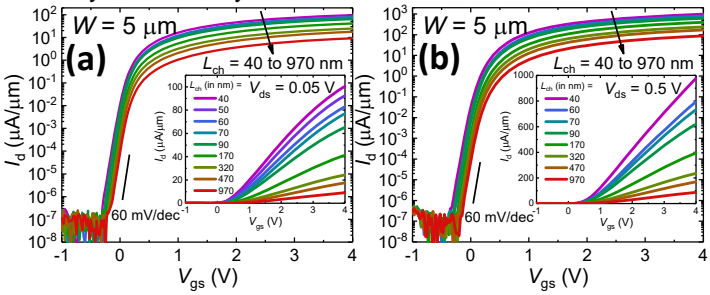


Fig. 4. Transfer characteristics for FETs with W = 5 μm and L_{ch} ranging from 40 to 970 nm at (a) V_{ds} = 0.05 V and (b) V_{ds} = 0.5 V. Both log and linear scales are shown. A tight V_t distribution with near-ideal S for all L_{ch} values demonstrates excellent electrostatic scaling.

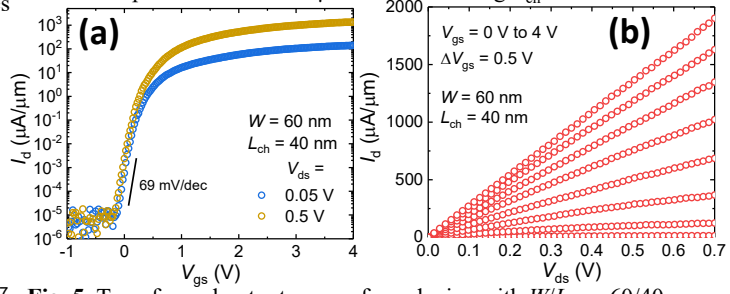


Fig. 5. Transfer and output curves for a device with W/L_{ch} = 60/40 nm.

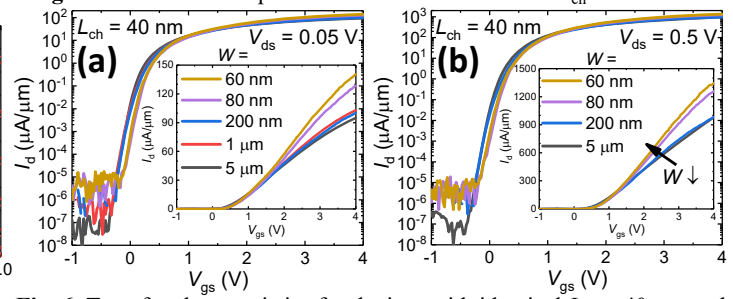


Fig. 6. Transfer characteristics for devices with identical L_{ch} = 40 nm and different W ranging from 5 μm to 60 nm in both log and linear scales.

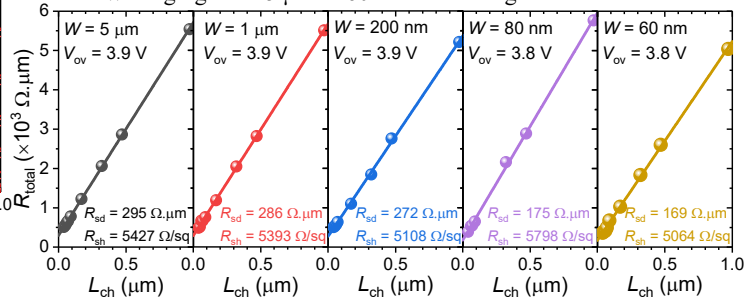


Fig. 7. Gated-TLM analysis of FETs with different W. Symbols: exp. data; solid: linear fittings. R_{sd} and R_{sh} are extracted for each set of devices.

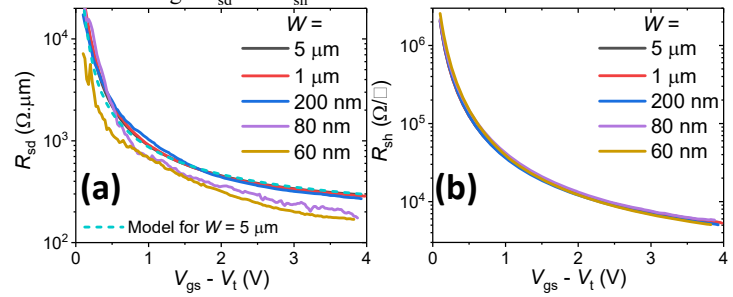


Fig. 8. (a) R_{sd} and (b) R_{sh} as a function of gate overdrive for devices with different W, extracted using gated-TLM analyses as shown in **Fig. 7**. The bias-dependent component of R_{sd} (R_B in **Fig. 12**) is found to be proportional to ~$V_{ov}^{-1.2}$ and is used in the model.

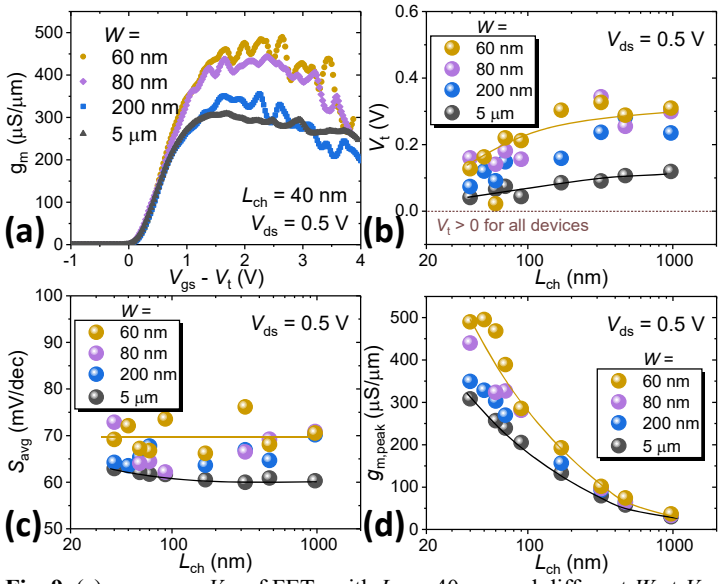


Fig. 9. (a) g_m versus V_{ov} of FETs with L_{ch} = 40 nm and different W at V_{ds} = 0.5 V. (b)-(d) Extracted V_t, S_{avg} and $g_{m,peak}$ at V_{ds} = 0.5 V versus L_{ch} for different W. Trend lines for W = 5 um and 60 nm are drawn in (b)-(d).

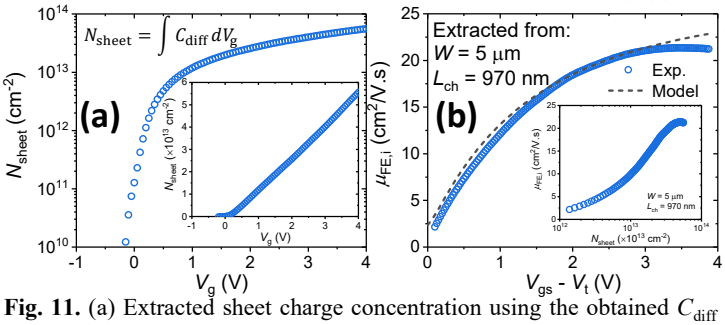
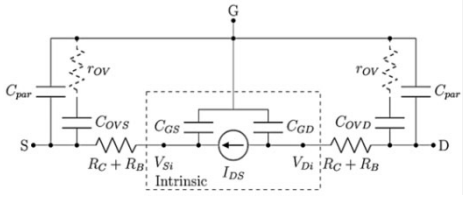


Fig. 11. (a) Extracted sheet charge concentration using the obtained C_{diff} in **Fig. 10(c)**. (b) Extracted intrinsic field-effect mobility. Empirically, to the first order $\mu_{FE,i}$ is proportional to $V_{ov}^{1.2}$, which is used in the model.



Key elements:
- I_{DS}: intrinsic channel current
- R_B: bias-dep. series R
- R_C: bias-indep. series R
- r_{ov}: small-signal R
- $C_{G(S,D)}$: intrinsic channel C
- $C_{ov(S,D)}$: bias-dep. overlap C
- C_{par}: bias-indep. parasitic C

Fig. 12. Netlist for MVS-AOS formulation. I_{DS}, C_{GS} and C_{GD} scale with L_{ch} following classic drift-diffusion theory. R_B, R_C, $C_{ov\,(S,D)}$ and C_{par0} are attributed to the S/D regions, hence independent of L_{ch}. r_{ov} (proportional to trap time constant) is a small-signal resistance to capture the C-V frequency dispersion due to the inertia of charge responding to high frequency signal in the trap-rich S/D regions.

$$Q_{i(S,D)} = C_{inv} \cdot 2n\varphi_T \ln\left(1+\exp\left(\frac{V_{GX(Si,Di)}-V_t}{2n\varphi_T}\right)\right) \quad (1) \qquad I_{DS} = \mu\frac{W}{L}\frac{(Q_{iS}^2-Q_{iD}^2)}{2C_{inv}} \quad (2) \qquad S = n\varphi_T ln(10) \quad (5)$$

$$Q_{(S,D)} = \frac{2WL}{(Q_{iS}^2-Q_{iD}^2)^2}\left[\mp Q_{i(D,S)}^3\frac{Q_{iS}^2-Q_{iD}^2}{3} \pm \frac{Q_{iS}^5-Q_{iD}^5}{5}\right]; \quad C_{G(S,D)} = -\frac{\partial Q_{(S,D)}}{\partial V_{G(Si,Di)}} \quad (3) \qquad \mu_{FE,i} \propto V_{ov}^{\theta_{FE}} \quad (6)$$

$$Q_{ov(S,D)} = WC_{ovQB}\cdot n_{ov}\varphi_T \ln\left(1+\exp\left(\frac{V_{G(S,D)}-V_{t,ov}}{n_{ov}\varphi_T}\right)\right); \quad C_{ov(S,D)} = \frac{\partial Q_{ov(S,D)}}{\partial V_{G(S,D)}} \quad (4) \qquad R_B \propto V_{ov}^{\theta_R} \quad (7)$$

Fig. 13. Key equations for MVS-AOS. $Q_{i(S,D)}$: areal charge density at the (S,D) edge of the channel following [18]. φ_T: thermal voltage. S: subthreshold swing. C_{inv}: areal gate capacitance in the channel, including quantum effects [19]. V_t is the threshold voltage accounting for DIBL and trap-induced V_t shift. $Q_{(S,D)}$: S/D terminal charge. $\theta_{(FE,R)}$ are fitting parameters. $C_{ov(S,D)}$ is computed similarly as $Q_{i(S,D)}$ with threshold voltage V_{tov} and includes the quantum effects through C_{ovQB}. Almost identical parameter set is used to fit devices with different L_{ch} at W = 5 μm, with only minor adjustment of the S, DIBL, V_t and the unit-width overlap capacitances used to calculate C_{ovQB}.

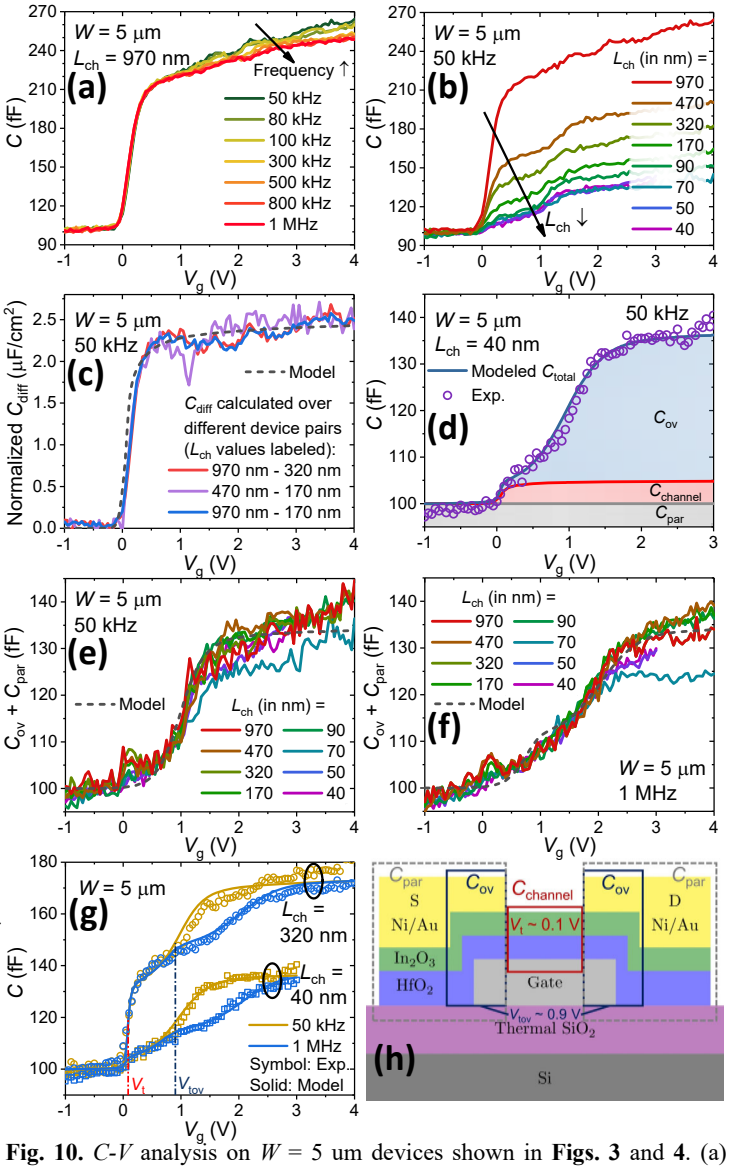


Fig. 10. C-V analysis on W = 5 um devices shown in **Figs. 3** and **4**. (a) Frequency (f)-dependent C-V of the L_{ch} = 970 nm device, measured with S/D shorted. (b) C-V curves at 50 kHz. (c) Normalized differential capacitance (C_{diff}) curves evaluated from different pairs of devices show excellent agreement with each other. Modeled C_{diff} is also shown. (d) Measured and modeled total capacitance (C_{total}), showing individual contributions of parasitic capacitance (C_{par}), overlap capacitance (C_{ov}) and channel capacitance ($C_{channel}$). (e)-(f) Extracted and modeled C_{par} + C_{ov} at (e) 50 kHz and (f) 1 MHz. Minor variation is due to unavoidable process uncertainty. (g) Measured and modeled f-dependent C-V. (h) Schematic device structure showing different regional V_t and C components.

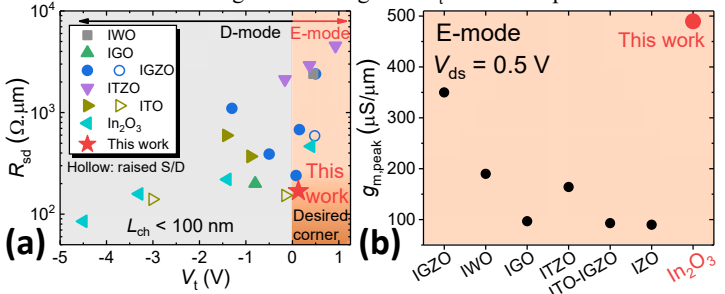


Fig. 14, Benchmarking of (a) R_{sd} vs. V_t for short-L_{ch} AOS FETs and (b) Maximum $g_{m,peak}$ achieved at V_{ds} = 0.5 V in E-mode FETs made of each AOS material [1-12,14-16,20-27]. V_t is defined @ 100 nA/μm.