INVITED FEATURE PAPER

Gate dielectric reliability and instability in GaN metal-insulator-semiconductor high-electron-mobility transistors for power electronics

Jesús A. del Alamo,[a] Alex Guo, and Shireen Warnock
Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA

(Received 6 June 2017; accepted 18 August 2017)

GaN field-effect transistors with impressive power switching characteristics have been demonstrated. Preventing their widespread field deployment are reliability and instability concerns. Some emanate from the use of a dielectric in the gate stack. Under typical operation, the gate dielectric comes periodically under intense electric field. This causes trapping and detrapping of electrons and introduces transient shifts in the threshold voltage, a phenomenon known as Bias-Temperature Instability (BTI). A high electric field also results in the formation of defects inside the dielectric. Over time, the defects accumulate and eventually result in the abrupt creation of a conducting path that shorts the dielectric and renders the device inoperable. This process, known as Time-Dependent Dielectric Breakdown (TDDB), often imposes a maximum lifetime for the FET technology. This article presents a methodology for the study of BTI and TDDB in insulated-gate GaN FETs. Our findings paint a picture of BTI and TDDB that in many respects is similar to that of Si transistors but with some unique characteristics. Understanding the physics and developing appropriate lifetime models is essential to enabling the deployment of this important new power electronics technology.

I. INTRODUCTION

In the last few years, GaN has emerged as a semiconductor with extraordinary capabilities in photonics and electronics. GaN packs a unique set of physical attributes: a wide and large direct band gap, high breakdown field, excellent thermal conductivity, and a relatively high electron mobility.[1] GaN belongs to a family of ternaries, including InGaN and AlGaN, which span a wide range of bandgaps and make possible GaN-based light-emitting diodes (LED) with colors from red to ultra-violet.[2] GaN LEDs today represent a multibillion dollar market. Blue GaN lasers are also commercial for high-density recording.

Heterostructures based on GaN and AlGaN also lead to the formation of a two-dimensional electron gas (2DEG) on the GaN side of the interface even in the absence of doping.[3] This is due to the large spontaneous polarization of AlGaN as well as stress-induced polarization in AlGaN that arises from its lattice mismatch with GaN. The lack of doping confers electrons with very high mobility, about 2000 $cm^2/V.s$ at room temperature. The excellent quality of this heterostructure system has been demonstrated in the observation of the quantum-Hall effect and the fractional quantum-Hall effect.[4] AlGaN/GaN High Electron Mobility Transistors (HEMT) were first demonstrated in 1993.[5] The combination of a high breakdown field in GaN with the high mobility and good electron confinement of the 2DEG at the AlGaN/GaN interface brings about a unique suitability of GaN HEMTS for power amplifier applications in the radio frequency (RF), microwave, and millimeter-wave regimes.[6]

Electrical power management is another application field where the unique properties of GaN shine.[7] Power electronics systems are becoming ubiquitous as electrification permeates deeper into human society. Semiconductor Si dominates the active components in power electronics. Compared with Si, GaN power transistors offer lower resistive losses, smaller size, and can operate at higher frequency. This brings about significant savings in the size of energy storage elements (capacitors and inductors) and, therefore, the overall system volume, as well as relaxed packaging and cooling needs.

The Metal-Insulator-Semiconductor High-Electron Mobility Transistor (MIS-HEMT) is the preferred active device structure for power management applications based on GaN.[8] The MIS-HEMT combines the excellent transport characteristics of the HEMT with the gate current blocking capabilities associated with the gate dielectric of a MOSFET. As a power switch, the

Contributing Editor: Don W. Shaw
[a]Address all correspondence to this author.
e-mail: alamo@mit.edu
This paper has been selected as an Invited Feature Paper.
DOI: 10.1557/jmr.2017.363

transistor alternatively operates in two states: a highly conducting ON state and a highly insulating OFF state that can sustain a large voltage. The MIS-HEMT structure is effective in balancing both requirements and realizes the great potential of GaN for power electronics. A simplified cross section of a MIS-HEMT is shown in Fig. 1. Impressive GaN MIS-HEMT power switching performance has been demonstrated[9] and the expectations are for substantial improvement over the most advanced Si power transistors and for wide displacement of Si in many applications.[10]

In spite of these great attributes, GaN MIS-HEMTs have yet to be widely deployed in commercial applications. The main bottleneck is establishing adequate stability and reliability. This is often the case with a new electronic technology. However, GaN power MIS-HEMTs face an unusual hurdle that derives from their use of a Si substrate. This is an economic imperative. Native GaN substrates are too small and expensive. SiC substrates, commonly used in GaN HEMTs for microwave power amplifiers, are also relatively small for the volume productions that are expected, as well as excessively expensive. Si, on the other hand, is available in large diameter wafers, is inexpensive, and there is a well-established manufacturing infrastructure around the world. A remarkable fact is that, in spite of the large lattice mismatch between GaN and Si, high performance GaN transistors are routinely demonstrated. However, the use of an Si substrate comes with a price of high defectivity in the AlGaN/GaN active layers that takes a toll on the stability of the device and creates reliability concerns.

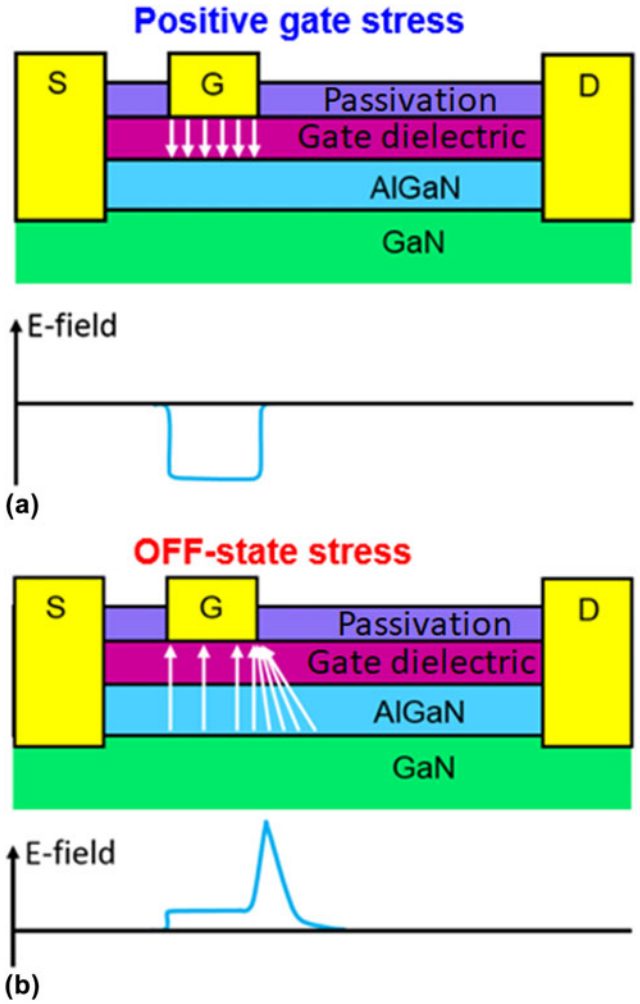

FIG. 1. Sketches of the electric field in the gate dielectric of an AlGaN/GaN MIS-HEMT for the positive gate stress (a) and OFF-state stress (b). Positive gate stress yields a relatively uniform electric field underneath the gate, whereas the OFF-state stress results in a peak in the electric field on the drain-side edge of the gate.

This article is not about reliability and stability concerns associated with the AlGaN/GaN structure grown on a mismatched substrate. This has been extensively studied in HEMTs.[11–14] Our goal in this paper is to investigate the unique and novel issues brought in with the introduction of a gate dielectric in a power MIS-HEMT structure. As in other Metal-Insulator-Semiconductor (MIS) systems, Bias-Temperature Instability (BTI) issues in which the threshold voltage of the device shifts around depending on the operating conditions is a problem.[15–17] Furthermore, a sudden breakdown arising from defect formation induced by a high electric field across the gate dielectric, a process known as Time-Dependent Dielectric Breakdown (TDDB), also imposes a maximum lifetime to a transistor.[18–20] Until recently, both phenomena received scant attention in GaN MIS-HEMTs. Filling this gap is the purpose of this work. A complication in these studies has been the very significant trapping associated with the GaN heterostructure that presumably emanates from the defectivity that was mentioned above. This introduces very large shifts in the electrical characteristics of the devices in the course of the experimental studies as well as very complex dynamics that obstruct the unique issues associated with the gate dielectric.

In this work, we summarize our efforts in the development of a methodology designed to mitigate trapping effects associated with the semiconductor heterostructure of GaN MIS-HEMTs so as to bring to the forefront the unique issues introduced by the gate dielectric. This has allowed us to identify the dominant mechanisms associated with BTI and TDDB in these devices and build models that contribute toward the estimation of device lifetimes under field operating conditions.

II. TIME-DEPENDENT DIELECTRIC BREAKDOWN

One of the most prominent concerns facing GaN MIS-HEMTs is a failure mode known as TDDB. While well

https://doi.org/10.1557/jmr.2017.363

studied in the Si CMOS system,[18,21–23] it was not until several years ago that efforts to understand TDDB in the GaN MIS-HEMT system began.[20,24–26]

The devices we study, like many GaN MIS-HEMTs today, are depletion-mode or normally-ON transistors. This is problematic from a safety perspective for power applications. To solve this, a MIS-HEMT is often put in a cascode configuration with a silicon MOSFET.[27,28] During switching operation, in the OFF state (with $V_{GS} < V_T$), the MIS-HEMT must be able to block a high voltage applied to the drain.[29–31] This is the state of greatest concern as it comes to TDDB. The ON-state is more benign since 0 V is applied to the gate, and the drain is under a small bias.[28]

The cascode configuration is designed such that the GaN devices are never subjected to a positive gate bias. However, the positive gate stress condition yields a relatively uniform electric field across the gate dielectric, as illustrated by the top image of Fig. 1. This makes this stress condition ideal to provide fundamental understandings of TDDB in GaN MIS-HEMTs. The OFF-state stress condition, which mimics the blocking voltage a MIS-HEMT must sustain, is shown in the bottom of Fig. 1. A negative bias is applied on the gate terminal to turn the FET off, and a high bias is applied to the drain. This bias point yields a rather nonuniform electric field profile with a peak at the drain-side edge of the gate. The use of field plates moderates the peak electric field and brings it out further into the gate-drain gap. Nevertheless, in the OFF state with a high blocking voltage, a high electric is present across the dielectric that can trigger TDDB.

Our goal in this research is to contribute toward fundamental understanding of TDDB in GaN MIS-HEMTs. We therefore study devices without field plates, which have a simpler geometry. Our devices feature a SiN gate dielectric with a thickness of a few tens of nm and a gate area of 2000 μm^2. We begin our study under a positive gate stress to establish a robust foundational understanding. We later turn our focus to the OFF-state stress condition that mimics the more realistic stress of a cascode circuit.

Figure 2 shows the gate current (I_G) evolution as a function of stress time for a series of positive gate stress experiments on 20 devices at a $V_{GS,stress}$ of 12.4 V with $V_{DS,stress}$ = 0 V. The very uniform evolution of the gate current leading to breakdown across all transistors suggests that we are observing an intrinsic breakdown in a set of well-matched devices.[32] Thus the spread of breakdown times is not brought about by process-induced imperfections such as impurities, roughness, thinning, structural weakness, etc. but by the inherent randomness of the defect formation process.

The slight decrease of I_G in the initial stages of the experiment is indicative of trapping,[33] and the increase of I_G thereafter can be attributed to stress-induced leakage current, SILC.[34] Dielectric hard, i.e., catastrophic breakdown is observed to take place after 1000 s and is characterized by a very sharp vertical jump in the gate current of each device.

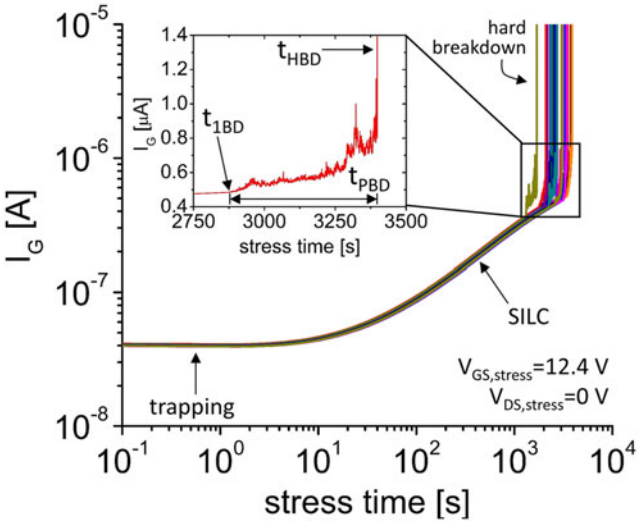

FIG. 2. Gate current I_G as a function of stress time during a series of constant $V_{GS,stress}$ TDDB experiments on 20 devices. The FETs are held at $V_{GS,stress}$ = 12.4 V until they break down. $V_{DS,stress}$ = 0 V. The inset shows detail of a representative device of the I_G evolution right before HBD. The clear onset of noise in I_G marks the beginning of PBD.

The inset, showing the late stage time evolution of the gate current in a representative device, indicates that approaching hard breakdown (HBD), I_G becomes noisy: a condition known as progressive breakdown (PBD).[19] This is distinct from the SILC regime we have seen before. While the increased leakage during SILC results from defects being generated everywhere within the dielectric in accordance with the percolation model,[35] PBD reflects the formation of a breakdown path created by these defects within the dielectric.[36] After the onset of PBD, further stress increases the I_G noise until HBD occurs. We denote the time at which gate noise appears as the time-to-first-breakdown, t_{1BD}, the time at which final hard breakdown occurs as t_{HBD}, and the time lapse in between as the length of PBD, or t_{PBD}.

Figure 3 shows the corresponding Weibull plot for the devices in Fig. 2. Time-to-breakdown in Si MOSFETs through an intrinsic mechanism has been found to follow Weibull statistics.[32] Here, we have separated time-to-first-breakdown, t_{1BD}, from time-to-hard breakdown, t_{HBD}. In these experiments, well-behaved Weibull statistics are observed with a Weibull slope[37] β of 4.4 and 4.8 for 1BD and HBD, respectively. The nearly parallel shift in the Weibull distributions of 1BD and HBD suggests a common origin for the two phenomena. Once the first breakdown occurs, additional gate stress continues to generate defects at random. Eventually, HBD takes place when enough energy is suddenly delivered to the PBD breakdown path so that it becomes nearly ohmic.[38] Thus, from device to device, we expected t_{1BD} and t_{HBD} to be uncorrelated but the overall statistics to be similar. Indeed, if, as suggested in Ref. 39, we plot t_{1BD} with its

corresponding PBD time, t_{PBD}, as shown in the inset of Fig. 3, we see that the two are independent of one another.

Not described here are stress-and-measure experiments that aim to understand the impact that the high electric field stress has on the device transfer characteristics. The transient instabilities by which GaN MIS-HEMTs are plagued[17,39] make this understanding more difficult. A methodology to address these issues and develop suitable experimental techniques has been described elsewhere.[24]

These experiments yield a good initial understanding of TDDB in the GaN MIS-HEMT system. The classic TDDB behavior that has emerged provides us with assurance that it should be possible to develop lifetime models that can be used for device lifetime estimations under operating conditions. From here, we can turn our attention to the OFF-state stress regime that emulates the stress a MIS-HEMT sees in its cascode configuration.

Figure 4 shows the evolution of the gate leakage current for a constant-voltage OFF-stress experiment. Here, the blue line corresponds to the evolution of the gate current I_G upon the application of a gate bias of $V_{GS,stress} = V_{T0} - 5$ V (V_{T0} is the threshold voltage defined at $I_D = 1$ μA for $V_{DS} = 0.1$ V on a virgin device) and a drain bias of $V_{DS,stress} = 118$ V. We observe multiple jumps in I_G (equal to the drain current I_D, not shown) before final hard breakdown occurs near 10^5 s. The jumps, except for the final one, are reminiscent of soft dielectric breakdown in silicon MOSFETs.[40] Hard breakdowns can occur either after a number of soft breakdown events, or for harsher stress conditions, it can be the very first instance of breakdown.[41]

The corresponding Weibull statistics for time-to-hard breakdown in the OFF-state experiment at $V_{DS,stress} = 118$ V are shown in the inset of Fig. 4. It is clear that the breakdown statistics do not follow a simple Weibull distribution, and the times-to-breakdown span many orders of magnitude. From these data, the physics of failure are unclear and one might conclude that we are in front of an extrinsic TDDB mechanism,[32] in contrast with our positive gate experiments described above. As we show next, this anomalous behavior is related to trapping effects, most likely taking place in the AlGaN/GaN structure.

Device characterization performed between periods of OFF-state stress reveals severe current collapse effects and large threshold voltage shifts.[42] It becomes clear that these transient effects have a significant impact on the OFF-state TDDB statistics as they are expected to affect the electric field distribution in a substantial way. Fortunately, ultraviolet (UV) light has previously been shown to be effective in recovering current collapse effects in GaN MIS-HEMTs after OFF-state stress.[43] In fact, trapping mitigation by means of UV light illumination during stress is known to result in an increase in the electric field for the same applied bias.[44] We therefore expect that the application of UV light during OFF-state TDDB experiments accelerates dielectric degradation.

The red data in Fig. 4 show the results from OFF-state stress experiments under a UV light of 3.5 eV (chosen based on Ref. 43). If we look first at the gate current evolution versus stress time, we find that despite a lower bias of $V_{DS,stress} = 89$ V, the device under UV light breaks down in a dramatically shorter amount of time than the device tested in the dark. There is also no evidence of any soft breakdown events before final catastrophic breakdown. This difference is another manifestation of the harsher stress conditions prevailing in the OFF state under UV. In Si devices, high stress voltage leads to "hard" breakdown characteristics (versus "soft" breakdown at lower voltages).[22]

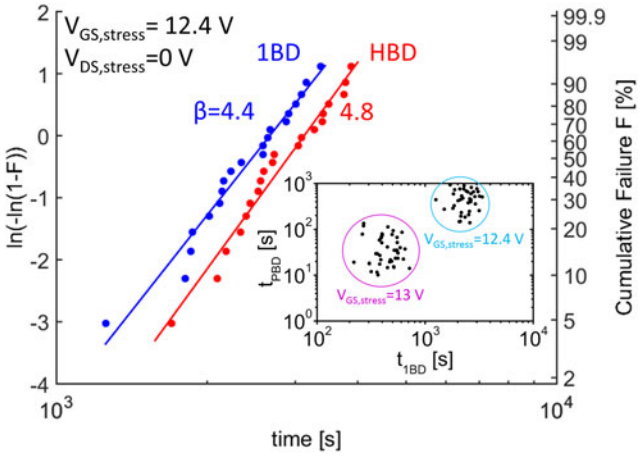

FIG. 3. Weibull plot of t_{1BD} and t_{HBD}. $V_{GS,stress} = 12.4$ V. $V_{DS,stress} = 0$ V. Nearly parallel statistics for time-to-first-breakdown t_{1BD} and time-to-hard-breakdown t_{HBD} suggest a unified degradation mechanism. Inset: PBD time versus t_{1BD} for samples stressed at $V_{GS,stress} = 12.4$ V and $V_{GS,stress} = 13$ V. Both sets of data show that t_{1BD} and t_{PBD} are uncorrelated. As $V_{GS,stress}$ increases both t_{1BD} and t_{PBD} decrease as well.

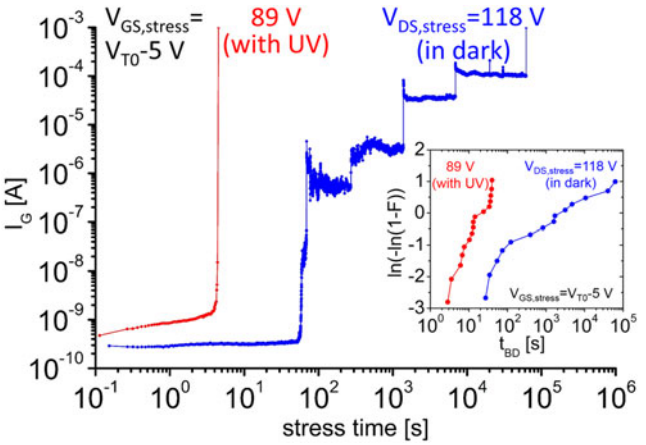

FIG. 4. Gate current I_G evolution for constant-voltage OFF-state TDDB experiments in the dark ($V_{DS,stress} = 118$ V) and under UV light ($V_{DS,stress} = 89$ V). Inset: Weibull plot of time-to-breakdown t_{BD} for OFF-state stress experiment in the dark and with UV light. $V_{GS,stress} = V_{T0} - 5$ V.

https://doi.org/10.1557/jmr.2017.363

The Weibull statistics in the inset, which compare OFF-state TDDB in the dark with OFF-state TDDB stress under UV light, show that under UV even with a 25% smaller $V_{DS,stress}$, the devices reach hard breakdown between 1 and 3 orders of magnitude faster than in the dark. We also see classic linear Weibull statistics that suggest we are now observing intrinsic TDDB behavior. This is what is expected from the positive-gate stress experiments described above.

The results of Fig. 4 highlight the importance of correctly isolating permanent degradation from transient effects that, in turn, can indirectly impact the degree of permanent degradation that is introduced. In our work, trapping effects cause a reduction of the applied electric field and this hastens permanent degradation. This complication, however, can be mitigated through UV illumination. To develop accurate lifetime models, it is clear that much care must be taken to ensure that device lifetime does not become distorted by transient trap-related degradation effects. However, use conditions must also be considered when evaluating device lifetimes since trapping affects the electric field that drives breakdown and location, and the degree of trapping depends on the actual operating conditions.

There are a number of further considerations that need to be addressed in a quest to develop lifetime models. Firstly, to accurately quantify the full extent of trapping in AlGaN/GaN MIS-HEMTs, device characterization needs to be performed using fast pulsed conditions. GaN MIS-HEMT dynamics are known to include very fast transients that dissipate before a relatively slow DC sweep can quantify them.[45–48] Also, when attempting to match device simulations and experimental data so that the electric field across the dielectric can be estimated, the simulations must account for the proper threshold voltage shift. It is the electric field during stress that must ultimately be used for lifetime extrapolation and, therefore, it is critical that this electric field be accurately estimated.

In addition, though this work has pursued a more physical understanding of TDDB, what is still missing is the exact nature of the defects in the dielectric. There was much controversy early on in the silicon MOS community over how the breakdown time scaled with the electric field, and much of this debate was focused on what the actual degradation mechanism was for TDDB in SiO_2.[49–57] A proper lifetime model for GaN MIS-HEMTs must draw upon this information to make precise extrapolations.

III. BIAS-TEMPERATURE INSTABILITY

The previous section has shown how prolonged electrical stress, even if relatively moderate, can result in noticeable transient changes in the electrical characteristics of MIS-HEMTs, most notably the threshold voltage V_T. In power switching applications, this is a serious problem as V_T marks the boundary in the gate bias between the ON state and the OFF state. Improper device turn-on or turn-off can result in device or system damage. Circuit and system designers expect a value of V_T that is kept within strict bounds.

The complex layer structure of GaN MIS-HEMTs and the defectivity that arises from the use of a Si substrate offer many possibilities for charge trapping that lead to transistor instability. Trapping in the GaN channel,[43] as well as in the AlGaN barrier has been reported.[48,58] When a thin AlN spacer is introduced between the AlGaN barrier and the GaN channel, additional trapping associated with the AlGaN/AlN interface has also been postulated.[58] Trapping at all these sites greatly obscures the contributions of the gate dielectric and its interface with the semiconductor to device instability, the object of this study.

To focus on the unique electrical instabilities associated with the gate dielectric in a GaN MIS-HEMT, we have carried out our studies instead on a simpler GaN MOSFET structure in which the dielectric is placed directly on top of the GaN channel. This is a device of interest for power applications in its own right.[59] While trapping effects associated with the GaN channel are still to be expected, the role of the dielectric and its interface with the channel should emerge with much more clarity.

Trapping studies require a carefully designed experimental methodology. Our approach consists of: (i) a benign transistor characterization suite and (ii) a thermal detrapping step that is both effective and benign. As in previous reliability studies in AlGaN/GaN[12] and InAlN/GaN HEMTs,[60] our characterization suite consists of measuring selected figures of merit (FOM) of the device that provide a view of the changes taking place as a result of electrical stress. However, repeated measurements of these FOMs should not affect the device in more than a minor way. As device FOMs, in our BTI studies, we have focused on the threshold voltage (V_T), peak transconductance, g_m, and subthreshold swing, S, all measured in the linear regime (low V_{DS}). These metrics provide a reasonably comprehensive view of trapping in the dielectric (V_T), impact on carrier scattering in the channel (g_m), and interface state formation at the oxide/semiconductor interface (S). The detailed measurement conditions for these metrics are given in Ref. 61. Though that is not always the case and great care has to be exercised, these FOMs are designed so that repeated measurements in the context of long stress-characterization experiments negligibly affect the device in the scale of what stress itself does.

The second tool in our study is a benign but an effective thermal detrapping step. This allows us to, following a benign stress experiment, detrap all trapped

carriers and recover the device initial conditions. It also enables isolation of the permanent and nonrecoverable device degradation that might originate under harsh stress conditions. We further use this thermal detrapping step to set a reproducible starting point for virgin devices in all our experiments. This erases any prior history of a given test device.

The devices used in our experiments are GaN MOSFETs with a SiO_2/Al_2O_3 composite dielectric with the Al_2O_3 directly on top of the GaN channel.[61] The gate oxide equivalent oxide thickness (EOT) is 40 nm. The channel width/length is 100/1 μm. Figure 5(a) shows the evolution of the threshold voltage in GaN MOSFETs as a function of time in stress-interrupt experiments at different gate stress voltages at room temperature ($V_{DS} = 0$).[61] Under positive gate voltage stress (PBTI), V_T shifts positive. Under negative voltage stress (NBTI), V_T shifts negative. The magnitude of the V_T shifts increases with time and stress voltage. Not shown are the changes of the transconductance. Under PBTI, g_m decreases with stress time and voltage while under NBTI, g_m increases in a similar manner. In both cases, there are no significant changes in the subthreshold swing. If the stress is interrupted, all FOMs slowly recover. For the conditions studied in Fig. 5, a final thermal detrapping step completely restores the device initial conditions.

An interesting observation is that there is a tight correlation between ΔV_T and Δg_m for both PBTI and NBTI during the stress and recovery phases, as shown in Fig. 5(b). The top-left quadrant of this figure graphs the PBTI data while the bottom-right quadrant contains the NBTI data. It is clear that the V_T and g_m changes are closely correlated across the entire experimental set with a continuous, linear relationship with a nearly constant slope. This suggests that NBTI and PBTI in GaN MOSFETs are the result of a common fully reversible mechanism.

Temperature has been found to accelerate all the observed changes. However, the acceleration rate is relatively small. Activation energies E_a between 0.06 and 0.37 eV have been extracted for the stress and recovery phases of the V_T evolution under PBTI and NBTI conditions.[61] This suggests the presence of small energy barriers to the prevailing processes and the preponderance of tunneling.

The recoverable changes in V_T and other electrical FOM are consistent with electron trapping and detrapping in preexisting oxide traps. Schematic diagrams of the processes are sketched in Fig. 6. It is known that Al_2O_3 contains traps that cluster in a band of an energy range and density that depends on the details of deposition and postdeposition treatment.[62] In our devices, we postulate that with the device under zero bias, the defect band extends from below the Fermi level to above the edge of the GaN conduction band, as sketched on the left of Fig. 6. The oxide defects that are located below the Fermi level are occupied, while those above are empty.

Under PBTI stress conditions, the defect band is brought below the Fermi level in the GaN channel and electrons tunnel into the available trap states [Fig. 6(b)]. This shifts V_T positive. Under PBTI recovery, electrons from the traps tunnel back to the GaN conduction band [Fig. 6(c)]. As a result, V_T recovers. Under NBTI, the contrary happens. During stress, occupied trap states emit their electrons to the GaN channel [Fig. 6(d)], while during the recovery, electrons tunnel back into the oxide defects [Fig. 6(e)]. This picture is consistent with the small activation energies that we have observed in the temperature-dependent experiments. PBTI stress and NBTI recovery are characterized by very small E_a, while PBTI recovery and NBTI stress exhibit comparatively higher E_a values.

The changes that are observed in the transconductance and the subthreshold swing are also consistent with this picture. Electron trapping in the oxide (as during PBTI stress and NBTI recovery) introduces additional Coulombic scattering for channel electrons. This results in a reduction of the device g_m. Electron detrapping during PBTI recovery and NBTI stress correspondingly reduces Coulombic scattering and g_m increases. With the oxide

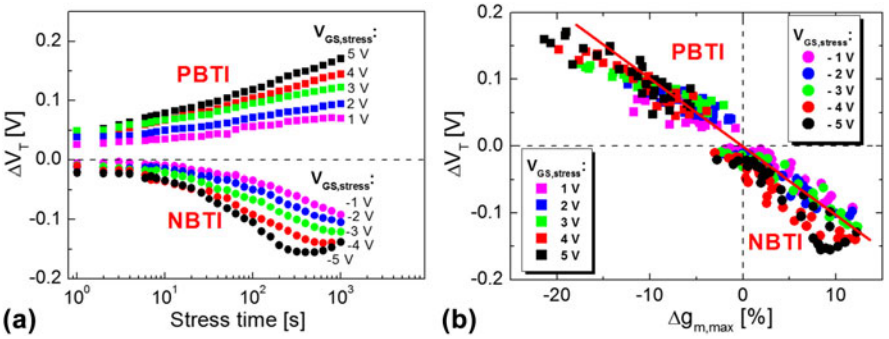

FIG. 5. (a) Time evolution of ΔV_T fin stress experiments with $V_{GS,stress}$ from −5 to 5 V at RT. (b) Correlation between ΔV_T and $\Delta g_{m,max}$ throughout stress and recovery for PBTI and NBTI experiments at RT. The universal relationship that is obtained suggests a common physical origin.

https://doi.org/10.1557/jmr.2017.363

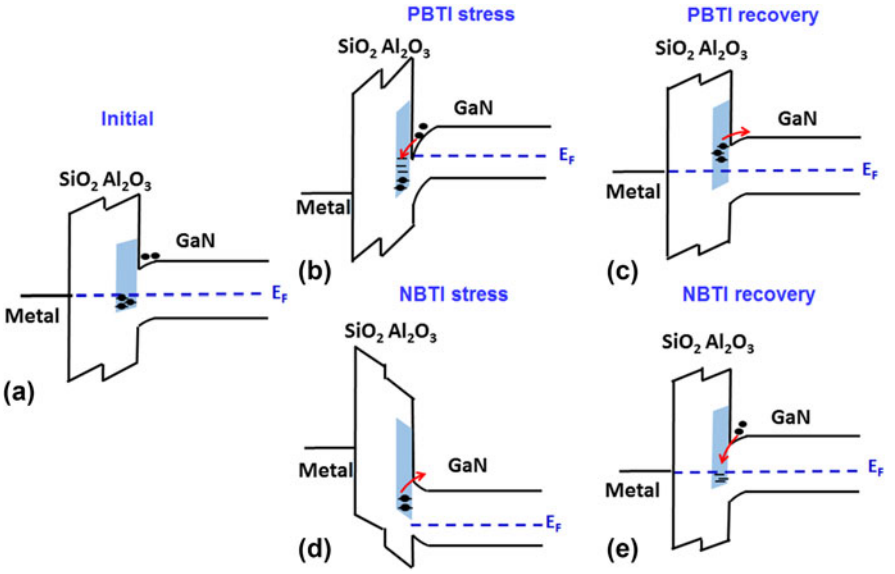

FIG. 6. Energy band diagram of GaN MOSFETs in equilibrium and under PBTI/NBTI stress and recovery. Electron trapping and detrapping from a single unified band of defects inside the Al_2O_3 barrier explains all results.

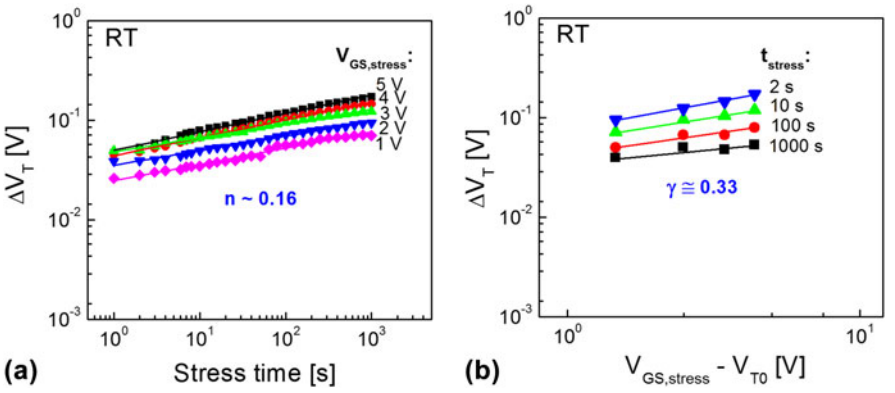

FIG. 7. (a) Empirical fits for ΔV_T evolution with stress time at RT, for $V_{GS,stress}$ from 1 to 5 V. (b) Empirical fits for ΔV_T evolution with stress voltage at RT, for positive $V_{GS,stress}$ at various t_{stress} values. Symbols: experimental data. Solid lines: empirical fitting results.

traps being located at some distance from the oxide/semiconductor interface and their response being rather sluggish [see time scale in Fig. 5(a)], during a relatively fast trace of the device subthreshold characteristics, no significant change in the trapped electron population is possible. Hence, the subthreshold swing of the device is unaffected in these experiments.

Our observations are consistent with those of other authors in similar MOS systems involving GaN and other semiconductors.[62–64] As in these and other works, simple power laws are found to describe relatively well the evolution of V_T with stress time and stress overdrive voltage. For our PBTI experiments, the time dependence is illustrated in Fig. 7(a). A power law with a relatively shallow exponent describes well all experiments at all stress voltages. The value of the exponent, $n = 0.16$, is close to that reported by other authors.[61–63] The dependence of ΔV_T on the stress gate voltage overdrive (with respect to the V_T of the virgin device, or V_{T0}) at different stress times is also well described by a power law with a single exponent $\gamma = 0.33$. This value reflects the energy distribution of traps inside the oxide.[62,63] The relatively small value of γ that we obtain under PBTI conditions suggests a broad distribution of empty traps in the oxide above the channel Fermi level. For NBTI, a higher value of γ is obtained, indicating that the trap density drops more quickly for lower energies inside the oxide band gap.[65]

The BTI experiments described so far are carried out under relatively moderate stress conditions. Harsher stress changes the picture substantially. PBTI experiments at higher stress voltages ($V_{G,stress} \sim 15$ V) produce nonrecoverable positive shifts in V_T that correlate well with permanent drops in g_m.[39] Both increase with time

https://doi.org/10.1557/jmr.2017.363

and temperature.[39] The subthreshold swing changes very little. This suggests the formation of new traps inside the oxide close to its interface with the semiconductor (although it could also indicate trapping of electrons in very deep traps that cannot be ejected during our thermal detrapping step).

NBTI experiments under harsher stress conditions offer a very rich picture. A summary is shown in Fig. 8.[65] This graph shows the evolution of V_T in an experiment at a relatively high negative stress voltage at high temperatures. The evolution of V_T indicates three distinct regimes. For short times, V_T shifts negative (regime I). This is consistent with electron detrapping from the oxide, as discussed above. For medium times, V_T shifts positive and increases with time (regime II). Eventually, V_T peaks and starts shifting negative (regime III). At the end of the experiment, we are left with a nonrecoverable negative V_T shift.

Further experiments[65] have indicated that regime II is fully recoverable, and it comes accompanied by a recoverable increase in S and a small recoverable drop in g_m. Temperature accelerates all changes. This is a puzzling set of results that can be explained by electron trapping in the GaN substrate under the gate edges, as illustrated in Fig. 8(b). In this hypothesis, under a high negative gate bias, a strong vertical electric field appears under the edges of the gate. This enables electron trapping in defect states close to the valence band inside the GaN band gap. This process involves electron tunneling, but it also has a thermal component. Electron trapping in this region lifts the bands of the GaN channel up, effectively increasing the local hole concentration under both edges of the gate. This temporarily shifts V_T positive, increases S, and reduces g_m. This mechanism is fully reversible. A similar mechanism has been invoked to explain current collapse under the edge of the field plates in high-voltage AlGaN/GaN MIS-HEMTs.[43]

Under harsher conditions (high negative stress voltage or very long stress time), the situation changes again: V_T shifts negative, S increases, and g_m drops. At the end of the experiment, even after thermal detrapping, we are left with a permanent net $\Delta V_T < 0$, a permanent increase in S, and a permanent drop in g_m.[65] There is an excellent correlation between the permanent changes in V_T, S, and g_m for a broad range of stress time/temperature/voltage combinations. This is all consistent with the formation of interface states as a result of, perhaps, broken H bonds at the oxide/semiconductor interface. Similar phenomena have been documented to take place in other MOS systems.[19,66]

To summarize our BTI studies in the GaN MOS system with a SiO_2/Al_2O_3 composite dielectric, under moderate stress conditions, the dominant source of instability appears to be reversible electron trapping and detrapping in preexisting defects in the gate oxide. Under harsh stress, nonrecoverable interface state formation at the oxide/semiconductor interface is also likely to be taking place. Not easily recoverable deeper trapping in the oxide might be a factor as well. The well-behaved power law dependencies observed for oxide trapping and detrapping suggest the possibility of lifetime models that can be used by circuit and system designers. Deposition conditions and postdeposition process treatments are likely to impact the density, energy distribution, and characteristic energy of the responsible traps. Other dielectrics such as SiO_2, Si_3N_4, or others are likely to behave in different ways.[39] Systematic studies need to be carried out.

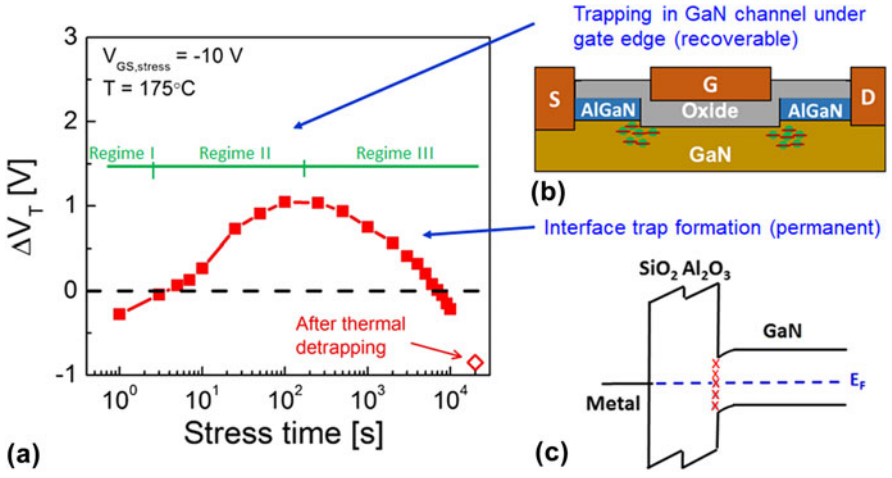

FIG. 8. (a) ΔV_T as a function of stress time for $V_{GS,stress} = -10$ V at 175 °C. The open symbol at the end indicates final ΔV_T after a benign thermal detrapping step. (b) Channel trapping mechanism postulated for regime II. Through a combination of thermal emission and tunneling, electrons from the valence band get trapped in defect states as a result of the high vertical electric field in the GaN channel caused by a high reverse bias stress. Trapping preferentially takes place in the GaN channel under the source and drain edges of the gate. (c) Energy band diagram illustrating the formation of interface states responsible for regime III and the final nonrecoverable degradation.

Our experimental methodology has been able to tease these mechanisms out of a background of trapping in the GaN channel/substrate, which can affect the electrical behavior of the device in a major way. In actual power AlGaN/GaN MIS-HEMTs, all the phenomena come in action at the same time. Without proper physical understanding, it will be difficult to develop a sense of the most relevant mechanisms at the selected operating conditions and to develop suitable lifetime models. Our work is a contribution in this direction, but much more work is needed.

IV. CONCLUSIONS

We have summarized recent research in the instability and electrical reliability of GaN MIS-HEMTs for power management applications. These devices offer impressive performance but widespread commercial use is prevented due to concerns on ruggedness and stability. In this article, we have focused on issues associated with the introduction of a gate dielectric in GaN MIS-HEMTs. Among them, TDDB and bias-temperature instability are major concerns. Studies of these phenomena in these devices are complicated by the severe trapping that takes place in the semiconductor and at interfaces and the complexity of the layer structure. We have devised experimental techniques to work around these difficulties. The picture that emerges is largely one of the classical metal-insulator-semiconductor behaviors observed in other dielectric/semiconductor systems. This gives us the confidence that suitable device lifetime models can be developed for circuit and system designers to use.

REFERENCES

1. H. Morkoc: *Nitride Semiconductors and Devices*, 1st ed. (Springer-Verlag Berlin Heidelberg, Weinheim, Germany, 1999).
2. S. Nakamura: Nobel lecture: Background story of the invention of efficient blue InGaN light emitting diodes. *Rev. Mod. Phys.* **87**, 1139 (2015).
3. M. Asif Khan, R.A. Skogman, J.M. Van Hove, D.T. Olson, and J.N. Kuznia: Atomic layer epitaxy of GaN over sapphire using switched metalorganic chemical vapor deposition. *Appl. Phys. Lett.* **60**, 1366 (1992).
4. M.J. Manfra, N.G. Weimann, J.W.P. Hsu, L.N. Pfeiffer, K.W. West, S. Syed, H.L. Stormer, W. Pan, D.V. Lang, S.N.G. Chu, G. Kowach, A.M. Sergent, J. Caissie, K.M. Molvar, L.J. Mahoney, and R.J. Molnar: High mobility AlGaN/GaN heterostructures grown by plasma-assisted molecular beam epitaxy on semi-insulating GaN templates prepared by hydride vapor phase epitaxy. *J. Appl. Phys.* **92**, 338 (2002).
5. M. Asif Khan, A. Bhattarai, J.N. Kuznia, and D.T. Olson: High electron mobility transistor based on a GaN–$Al_xGa_{1-x}N$ heterojunction. *Appl. Phys. Lett.* **63**, 1214 (1993).
6. R.S. Pengelly, S.M. Wood, J.W. Milligan, S.T. Sheppard, and W.L. Pribble: A review of GaN on SiC high electron-mobility power transistors and MMICs. *IEEE Trans. Microwave Theory Tech.* **60**, 1764 (2012).
7. A. Lidow, J. Strydom, M. de Rooij, and Y. Ma: *GaN Transistors for Efficient Power Conversion*, 1st ed. (Power Conversion Publications, El Segundo, California, 2012).
8. M. Van Hove, S. Boulay, S.R. Bahl, S. Stoffels, X. Kang, D. Wellekens, K. Geens, A. Delabie, and S. Decoutere: CMOS process-compatible high-power low-leakage AlGaN/GaN MIS-HEMT on silicon. *IEEE Electron Device Lett.* **33**, 667 (2012).
9. H.W. Then, L.A. Chow, S. Dasgupta, S. Gardner, M. Radosavljevic, V.R. Rao, S.H. Sung, G. Yang, and P. Fischer: High-K gate dielectric depletion-mode and enhancement-mode GaN MOS-HEMTs for improved off-state leakage and DIBL for power electronics and RF applications. In *IEEE International Electron Devices Meeting* (IEEE, Washington D.C., 2015); pp. 16–23.
10. G. Deboy, M. Treu, O. Haeberlen, and D. Neumayr: Si, SIC and GaN power devices: An unbiased view on key performance indicators. In *IEEE International Electron Devices Meeting* (IEEE, San Francisco, California 2016); pp. 20–22.
11. E. Zanoni, M. Meneghini, A. Chini, D. Marcon, and G. Meneghesso: AlGaN/GaN-based HEMTs failure physics and reliability: Mechanisms affecting gate edge and Schottky junction. *IEEE Trans. Electron Devices* **60**, 3119 (2013).
12. J.A. del Alamo and J. Joh: GaN HEMT reliability. *Microelectron. Reliab.* **49**, 1200 (2009).
13. D. Marcon, J. Viaene, P. Favia, H. Bender, X. Kang, S. Lenci, S. Stoffels, and S. Decoutere: Reliability of AlGaN/GaN HEMTs: Permanent leakage current increase and output current drop. *Microelectron. Reliab.* **52**, 2188 (2012).
14. T. Ohki, T. Kikkawa, Y. Inoue, M. Kanamura, N. Okamoto, K. Makiyama, K. Imanishi, H. Shigematsu, K. Joshin, and N. Hara: Reliability of GaN HEMTs: Current status and future technology. In *IEEE International Reliability Physics Symposium* (IEEE, Montreal, Canada 2009); pp. 61–70.
15. S. Zafar, Y. Kim, V. Narayanan, C. Cabral, V. Paruchuri, B. Doris, J. Stathis, A. Callegari, and M. Chudzik: A comparative study of NBTI and PBTI (charge trapping) in SiO_2/HfO_2 stacks with FUSI, TiN, Re gates. In *International Symposium on VLSI Technology* (IEEE, Honolulu, Hawaii, 2006); pp. 23–25.
16. J.H. Stathis and S. Zafar: The negative bias temperature instability in MOS devices: A review. *Microelectron. Reliab.* **46**, 270 (2006).
17. P. Lagger, C. Ostermaier, G. Pobegen, and D. Pogany: Towards understanding the origin of threshold voltage instability of AlGaN/GaN MIS-HEMTs. In *IEEE International Electron Devices Meeting* (IEEE, San Francisco, California, 2012); pp. 13–21.
18. C. Svensson and A. Shumka: Time dependent breakdown in silicon dioxide films. *Int. J. Electron.* **38**, 69 (1975).
19. G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo: Review on high-k dielectrics reliability issues. *IEEE Trans. Device Mater. Reliab.* **5**, 5 (2005).
20. T-L. Wu, D. Marcon, M.B. Zahid, M. Van Hove, S. Decoutere, and G. Groeseneken: Comprehensive investigation of on-state stress on D-mode AlGaN/GaN MIS-HEMTs. In *IEEE International Reliability Physics Symposium* (IEEE, Monterrey, California, 2013); pp. 3C–5C.
21. M.A. Alam, B.E. Weir, and P.J. Silverman: A study of soft and hard breakdown-part I: Analysis of statistical percolation conductance. *IEEE Trans. Electron Devices* **49**, 232 (2002).
22. M.A. Alam, B.E. Weir, and P.J. Silverman: A study of soft and hard breakdown-part II: Principles of area, thickness, and voltage scaling. *IEEE Trans. Electron Devices* **49**, 239 (2002).
23. X. Li, C.H. Tung, K.L. Pey, and V.L. Lo: The chemistry of gate dielectric breakdown. In *IEEE International Electron Devices Meeting* (IEEE, San Francisco California, 2008); pp. 1–4.

https://doi.org/10.1557/jmr.2017.363

24. S. Warnock and J.A. del Alamo: Stress and characterization strategies to assess oxide breakdown in high-voltage GaN field-effect transistors. In *Compound Semiconductor Manufacturing Technology Conference* (CS MANTECH, Scottsdale, Arizona, 2015); pp. 311–314.
25. M. Hua, C. Liu, S. Yang, S. Liu, K. Fu, Z. Dong, Y. Cai, B. Zhang, and K.J. Chen: Characterization of leakage and reliability of SiN_x gate dielectric by low-pressure chemical vapor deposition for GaN-based MIS-HEMTs. *IEEE Trans. Electron Devices* **62**, 3215 (2015).
26. S. Warnock and J.A. del Alamo: Progressive breakdown in high-voltage GaN MIS-HEMTs. In *IEEE International Reliability Physics Symposium* (IEEE, Pasadena, California, 2016); pp. 4A–6A.
27. X. Huang, Z. Liu, Q. Li, and F.C. Lee: Evaluation and application of 600 V GaN HEMT in cascode structure. *IEEE Trans. Power Electron.* **29**, 2453 (2014).
28. M. Meneghini, I. Rossetto, C. De Santi, R. Rampazzo, A. Tajalli, A. Barbato, M. Ruzzarin, M. Borga, E. Canato, E. Zanoni, and G. Meneghesso: Reliability and failure analysis in power GaN-HEMTs: An overview. In *IEEE International Reliability Physics Symposium* (IEEE, Monterrey, California 2017); pp. 3B-2.1–3B-2.8.
29. B.J. Baliga: Gallium nitride devices for power electronic applications. *Semicond. Sci. Technol.* **28**, 074011 (2013).
30. F.A. Marino, D. Bisi, M. Meneghini, G. Verzellesi, E. Zanoni, M. Van Hove, S. You, S. Decoutere, D. Marcon, S. Stoffels, N. Ronchi, and G. Meneghesso: Analysis of off-state leakage mechanisms in GaN-based MIS-HEMTs: Experimental data and numerical simulation. *Solid-State Electron.* **113**, 9 (2015).
31. M. Meneghini, I. Rossetto, F. Hurkx, J. Sonsky, J.A. Croon, G. Meneghesso, and E. Zanoni: Extensive investigation of time-dependent breakdown of GaN-HEMTs submitted to off-state stress. *IEEE Trans. Electron Devices* **62**, 2549 (2015).
32. D.R. Wolters and J.J. van der Schoot: Dielectric breakdown in MOS devices, part I: Defect-related and intrinsic breakdown. *Philips J. Res.* **45**, 115 (1985).
33. S. Demirtas, J. Joh, and J.A. del Alamo: High voltage degradation of GaN high electron mobility transistors on silicon substrate. *Microelectron. Reliab.* **50**, 758 (2010).
34. R. Degraeve, T. Kauerauf, M. Cho, M. Zahid, L-A. Ragnarsson, D.P. Brunco, B. Kaczer, P. Roussel, S. De Gendt, and G. Groeseneken: Degradation and breakdown of 0.9 nm EOT SiO/sub 2/ ALD HfO/sub 2/metal gate stacks under positive constant voltage stress. In *IEEE International Electron Devices Meeting* (IEEE, Washington, D.C., 2005); pp. 408–411.
35. R. Degraeve, B. Kaczer, and G. Groeseneken: Degradation and breakdown in thin oxide layers: Mechanisms, models and reliability prediction. *Microelectron. Reliab.* **39**, 1445 (1999).
36. F. Palumbo, M. Eizenberg, and S. Lombardo: General features of progressive breakdown in gate oxides: A compact model. In *IEEE International Reliability Physics Symposium* (2015); pp. 5A.1.1–5A.1.6.
37. E.Y. Wu, J.H. Stathis, and L-K. Han: Ultra-thin oxide reliability for ULSI applications. *Semicond. Sci. Technol.* **15**(5), 425 (2000).
38. G. Bersuker, N. Chowdhury, C. Young, D. Heh, D. Misra, and R. Choi: Progressive breakdown characteristics of high-k/metal gate stacks. In *IEEE International Reliability Physics Symposium* (IEEE, Phoenix, Arizona, 2007); pp. 49–54.
39. A. Guo and J.A. del Alamo: Positive-bias temperature instability (PBTI) of GaN MOSFETs. In *IEEE International Reliability Physics Symposium* (IEEE, Monterrey, California, 2015); pp. 6C.5.1–6C.5.7.
40. F. Crupi, R. Degraeve, G. Groeseneken, T. Nigam, and H.E. Maes: On the properties of the gate and substrate current after soft breakdown in ultrathin oxide layers. *IEEE Trans. Electron Devices* **45**, 2329 (1998).
41. J. Sune, E.Y. Wu, D. Jiménez, R.P. Vollertsen, and E. Miranda: Understanding soft and hard breakdown statistics, prevalence ratios and energy dissipation during breakdown runaway. In *IEEE International Electron Devices Meeting* (IEEE, Washington, D.C., 2001); pp. 117–120.
42. S. Warnock and J.A. del Alamo: OFF-state TDDB in high-voltage GaN MIS-HEMTs. In *IEEE International Reliability Physics Symposium* (2017); pp. 4B-3.1–4B-3.6.
43. D. Jin, J. Joh, S. Krishnan, N. Tipirneni, S. Pendharkar, and J.A. del Alamo: Total current collapse in high-voltage GaN MIS-HEMTs induced by Zener trapping. In *IEEE International Electron Devices Meeting* (IEEE, Washington D.C., 2013); pp. 148–151.
44. S. Demirtas and J.A. del Alamo: Effect of trapping on the critical voltage for degradation in GaN high electron mobility transistors. In *IEEE International Reliability Physics Symposium* (IEEE, Anaheim, California, 2010); pp. 134–138.
45. P. Lagger, M. Reiner, D. Pogany, and C. Ostermaier: Comprehensive study of the complex dynamics of forward bias-induced threshold voltage drifts in GaN based MIS-HEMTs by stress/recovery experiments. *IEEE Trans. Electron Devices* **61**, 1022 (2014).
46. P. Lagger, S. Donsa, P. Spreitzer, G. Pobegen, M. Reiner, H. Naharashi, J. Mohamed, H. Mosslacher, G. Prechtl, D. Pogany, and C. Ostermaier: Thermal activation of PBTI-related stress and recovery processes in GaN MIS-HEMTs using on-wafer heaters. In *IEEE International Reliability Physics Symposium* (IEEE, Monterrey, California, 2015); pp. 6C.2.1–6C.2.7.
47. R. Stradiotto, G. Pobegen, C. Ostermaier, and T. Grasser: On the fly characterization of charge trapping phenomena at GaN/dielectric and GaN/AlGaN/dielectric interfaces using impedance measurements. In *IEEE Solid State Device Research Conference* (IEEE, Sapporo, Japan, 2015); pp. 72–75.
48. D. Jin and J.A. del Alamo: Methodology for the study of dynamic on-resistance in high-voltage GaN field-effect transistors. *IEEE Trans. Electron Devices* **60**, 3190 (2013).
49. M.A. Alam, J. Bude, and A. Ghetti: Field acceleration for oxide breakdown—Can an accurate anode hole injection model resolve the E vs. $1/E$ controversy? In *IEEE International Reliability Physics Symposium* (IEEE, San Jose, California, 2000); pp. 21–26.
50. J.F. Conley, P.M. Lenahan, H.L. Evans, R.K. Lowry, and T.J. Morthorst: Observation and electronic characterization of two E' center charge traps in conventionally processed thermal SiO_2 on Si. *Appl. Phys. Lett.* **65**, 2281 (1994).
51. J.F. Conley, P.M. Lenahan, H.L. Evans, R.K. Lowry, and T.J. Morthorst: Electron-spin-resonance evidence for an impurity-related E'-like hole trapping defect in thermally grown SiO_2 on Si. *J. Appl. Phys.* **76**, 8186 (1994).
52. A.Y. Kang, P.M. Lenahan, and J.F. Conley: Electron spin resonance observation of trapped electron centers in atomic-layer-deposited hafnium oxide on Si. *Appl. Phys. Lett.* **83**, 3407 (2003).
53. M. Kimura: Oxide breakdown mechanism and quantum physical chemistry for time-dependent dielectric breakdown. In *IEEE International Reliability Physics Symposium* (IEEE, Denver, Colorado, 1997); pp. 190–200.
54. X. Li, C.H. Tung, and K.L. Pey: The nature of dielectric breakdown. *Appl. Phys. Lett.* **93**, 072903 (2008).
55. J.W. McPherson: Determination of the nature of molecular bonding in silica from time-dependent dielectric breakdown data. *J. Appl. Phys.* **95**, 8101 (2004).
56. J.W. McPherson, V.K. Reddy, and H.C. Mogul: Field-enhanced Si–Si bond-breakage mechanism for time-dependent dielectric breakdown in thin-film SiO_2 dielectrics. *Appl. Phys. Lett.* **71**, 1101 (1997).

57. J.W. McPherson, R.B. Khamankar, and A. Shanware: Complementary model for intrinsic time-dependent dielectric breakdown in SiO_2 dielectrics. *J. Appl. Phys.* **88**, 5351 (2000).
58. J. Joh and J.A. del Alamo: A current-transient methodology for trap analysis for GaN high electron mobility transistors. *IEEE Trans. Electron Devices* **58**, 132 (2011).
59. N. Ikeda, Y. Niiyama, H. Kambayashi, Y. Sato, T. Nomura, S. Kato, and S. Yoshida: GaN power transistors on Si substrates for switching applications. *Proc. IEEE* **98**, 1151 (2010).
60. Y. Wu and J.A. del Alamo: Electrical degradation of InAlN/GaN HEMTs operating under on conditions. *IEEE Trans. Electron Devices* **63**, 3487 (2016).
61. A. Guo and J.A. del Alamo: Unified mechanism for positive- and negative-bias temperature instability in GaN MOSFETs. *IEEE Trans. Electron Devices* **64**, 2142 (2017).
62. J. Franco, A. Alian, B. Kaczer, D. Lin, T. Ivanov, A. Pourghaderi, K. Martens, Y. Mols, D. Zhou, N. Waldron, S. Sioncke, T. Kauerauf, N. Collaert, A. Thean, M. Heyns, and G. Groeseneken: Suitability of high-k gate oxides for II–V devices: A PBTI study in $In_{0.53}Ga_{0.47}As$ devices with Al_2O_3. In *IEEE International Reliability Physics Symposium* (IEEE, Waikoloa, Hawaii 2014); pp. 6A.2.1–6A.2.6.
63. T-L. Wu, J. Franco, D. Marcon, B. De Jaeger, B. Bakeroot, S. Stoffels, M. Van Hove, G. Groeseneken, and S. Decoutere: Toward understanding positive bias temperature instability in fully recessed-gate GaN MISFETs. *IEEE Trans. Electron Devices* **63**, 1853 (2016).
64. M. Cho, J-D. Lee, M. Aoulaiche, B. Kaczer, P. Roussel, T. Kauerauf, R. Degraeve, J. Franco, L-Å. Ragnarsson, and G. Groeseneken: Insight into N/PBTI mechanisms in sub-1-nm-EOT devices. *IEEE Trans. Electron Devices* **59**, 2042 (2012).
65. A. Guo and J.A. del Alamo: Negative-bias temperature instability of GaN MOSFETs. In *IEEE International Reliability Physics Symposium* (IEEE, Pasadena, California 2016); pp. 4A.1–4A.1.6.
66. N. Wrachien, A. Cester, Y.Q. Wu, P.D. Ye, E. Zanoni, and G. Meneghesso: Effects of positive and negative stresses on III–V MOSFETs with Al_2O_3 gate dielectric. *IEEE Electron Device Lett.* **32**, 488 (2011).

https://doi.org/10.1557/jmr.2017.363