Unified Mechanism for Positive- and Negative-Bias Temperature Instability in GaN MOSFETs

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***Abstract*— We present a comprehensive study of bias temperature instability (BTI) in GaN MOSFETs under moderate positive and negative gate bias stress. We investigate the evolution of threshold voltage (V_T), maximum transconductance ($g_{m,max}$), and subthreshold swing (S). Our results show a universal continuous, symmetrical, and reversible V_T shift and $g_{m,max}$ change as gate stress voltage ($V_{GS,stress}$) increases from −5 to 5 V at room temperature. The time evolution of V_T is well described by a power law model. The voltage dependence, time dependence, and temperature dependence of our results suggest that for moderate gate bias stress, positive BTI and negative BTI are due to a single reversible mechanism. This is electron trapping/detrapping in preexisting oxide traps that form a defect band very close to the GaN/oxide interface and extend in energy beyond the conduction band edge of GaN and below the Fermi level at the channel surface at 0 V.**

***Index Terms*— Bias temperature instability (BTI), gallium nitride MOSFETs, oxide trapping, semiconductor device reliability.**

I. Introduction

GaN high electron mobility transistors (HEMTs) are promising for future power electronic systems [1]. For high voltage applications, the GaN MIS-HEMT is the most attractive device structure. Thanks to the insulated gate, the MIS-HEMT offers lower gate leakage and a larger gate swing as compared with the more traditional HEMT structure [2], [3]. On the other hand, gate dielectrics also introduce additional reliability and instability challenges that hamper technology commercialization [4].

One of the critical instabilities in GaN MIS-HEMTs is bias temperature instability (BTI), in which electrical parameters, in particular, the device threshold voltage, V_T, shift around under prolonged gate bias stress at high temperature [5]. It has been reported that V_T shift due to BTI in GaN MIS-HEMTs is much larger than in GaN HEMTs, even at low gate stress, which is detrimental to circuit performance [6]. It is challenging to understand the mechanisms behind BTI in MIS-HEMTs, because the gate-stack has multiple layers and interfaces with many possible trapping sites [7].

To contribute fundamental understanding relevant to this problem, we study a simpler GaN MOSFET structure. This allows us to investigate the role of the oxide and the oxide/GaN interface in BTI [8], [9]. In earlier studies, we found that under moderate gate stress, positive BTI (PBTI) causes a reversible positive V_T shift attributed to electron trapping in preexisting oxide traps [8]. Similarly, negative BTI (NBTI) under moderate conditions causes a reversible negative V_T shift that is hypothesized to arise from electron detrapping from preexisting oxide traps, and trapping in the GaN channel has also been observed under harsher NBTI conditions [9]. Other authors have drawn similar conclusions for PBTI [10], [11], but there are different views for the mechanisms behind NBTI [12]. Also, harsher stress, positive or negative, leads to irreparable damage presumably caused by other mechanisms, which is a serious reliability concern [8], [9], [13].

Nevertheless, in this paper, we focus on device instabilities under moderate stress. With our findings so far, it is reasonable to postulate that PBTI and NBTI in GaN MOSFETs under moderate stress arise from a single physical origin. Such is the case of irradiated Si MOSFETs under alternating positive and negative gate stress that causes electrons to tunnel back and forth from/to oxide traps [14]. Similar observations have been made in SiC MOSFETs [15]. In GaN MOSFETs, to date, PBTI and NBTI have been studied separately and it is not possible to assess whether they have a common mechanism that can be described by a single model.

In this paper, in search for a unified origin for PBTI and NBTI in GaN MOSFETs, we have carried out a study that spans positive and negative moderate gate stress voltages, different lengths of stress times, and different temperatures. This paper clearly reveals a common theme for both mechanisms that we attribute to electron trapping and detrapping from preexisting traps in the oxide.

II. Experiment

The devices studied here are E-mode AlGaN/GaN recessed-gate MOSFETs sketched in Fig. 1. The gate oxide consists of a SiO_2/Al_2O_3 composite with Al_2O_3 next to the GaN channel. The gate oxide EOT is 40 nm (both SiO_2 and Al_2O_3 layers are

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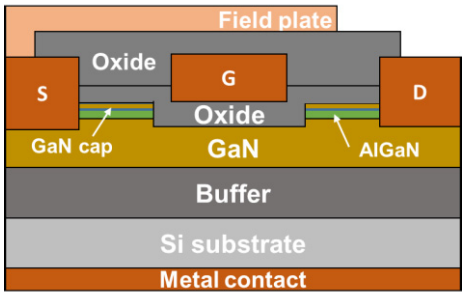

Fig. 1. Schematic cross section of recessed-gate GaN MOSFET structure studied in this paper.

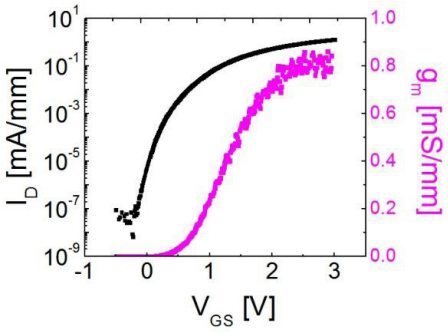

Fig. 2. Subthreshold and transconductance characteristics of a virgin GaN MOSFET in the linear regime ($V_{DS} = 0.1$ V) used in this paper. $V_T = 0.34$ V, S = 148 mV/decade, and $g_{m,max} = 0.91$ mS/mm.

relatively thick). The channel width/length is 100/1 μm. Fig. 2 shows the subthreshold and transconductance characteristics of a virgin device in the linear regime ($V_{DS} = 0.1$ V).

In this paper, we characterize the impact of prolonged moderate gate voltage stress on device behavior. We focus our interest on the stability of device figures of merit (FOMs), including V_T (defined at drain current $I_D = 1$ μA/mm), maximum transconductance ($g_{m,max}$), and linear subthreshold swing (S) (defined at drain current $I_D = 0.1$ μA/mm), all at $V_{DS} = 0.1$ V. We use a benign characterization scheme developed in our earlier studies [8], [9], where the characterization itself produces a minor change in the device characteristics in the scale of the electrically induced effects we are studying here (50 successive characterizations yield $\Delta V_T < 10$ mV and $\Delta S < 15$ mV/decade, where we carry out g_m extractions, $\Delta g_m < 0.02$ mS/mm). Here, all measurements of $g_{m,max}$ for both PBTI and NBTI are carried out using $I_D - V_{GS}$ sweeps that start from $V_{GS} = -0.5$ V and stop at $V_T + 1.5$ V. We utilize a thermal detrapping (TD) step that was calibrated to completely reset the device between runs [8], [9].

A typical experiment starts with device "initialization" in which the devices are first flushed with microscope light for 5 min followed by TD (we use a single set of TD conditions throughout this paper). This step helps create a "stable" initial state for the device. On average, the change of device characteristics before and after initialization is $\Delta V_T < 20$ mV and $\Delta S < 30$ mV/decade. Following this, we carry out an initial characterization in which we extract the device FOMs, which serve as a reference for subsequent stress/recovery measurements.

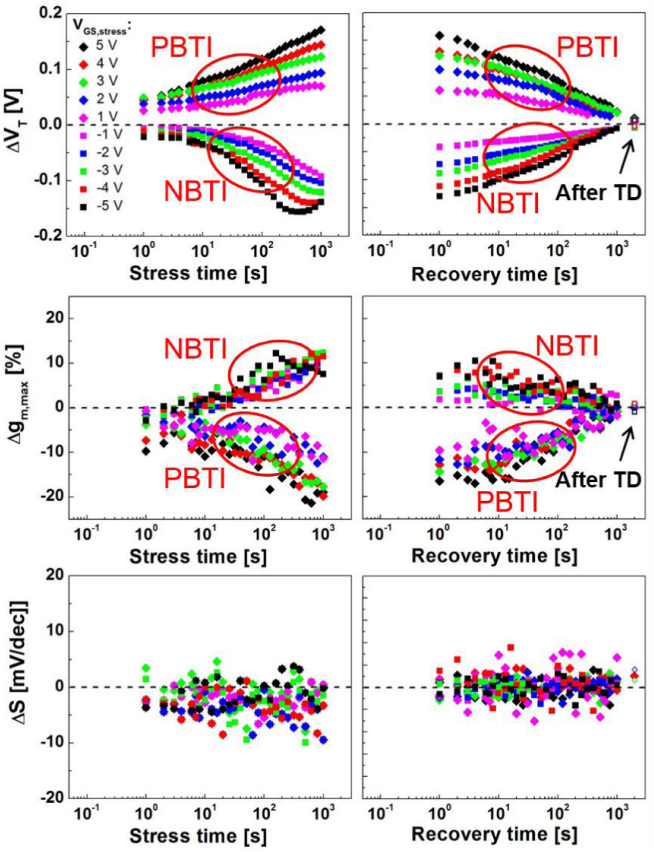

Fig. 3. Time evolution of ΔV_T, $\Delta g_{m,max}$, and ΔS for $V_{GS,stress}$ from -5 to 5 V at RT. Left: stress phase. Right: recovery phase. Open symbols at the end of the recovery represent final values after TD.

In a typical experiment, there is a stress phase and a recovery phase, In the stress phase, a device is subjected to a constant dc gate bias ($V_{GS,stress}$) with the source, drain, and substrate grounded. We periodically pause the stress and perform benign $I_D - V_{GS}$ sweeps to track changes in the device FOMs. In these characterization periods, the first V_T measurement is obtained through an $I_D - V_{GS}$ sweep about 1–2 s after the interruption of the stress. Following the stress phase, the device is allowed to recover for ~1000 s during which all terminals are grounded. Periodically, we monitor device recovery through benign $I_D - V_{GS}$ sweeps. At the end of the stress/recovery segment, the device is reinitialized using TD and final characterization is performed to confirm complete device recovery.

III. Results

A. Gate Bias Stress at Room Temperature

Fig. 3 shows the time evolution of ΔV_T, $\Delta g_{m,max}$, and ΔS under gate stress from -5 to 5 V (equivalent to oxide electric field of -1 to 1 MV/cm) at room temperature (RT) during stress and recovery. We use one device for the PBTI measurements and another device for the NBTI experiments.

For positive $V_{GS,stress}$, ΔV_T is positive and it increases with stress time and stress voltage. At the same time, we observe $g_{m,max}$ degradation that is also accelerated by stress time and voltage. Both ΔV_T and $\Delta g_{m,max}$ completely recover after TD. Changes in S are minimal. The gate bias current

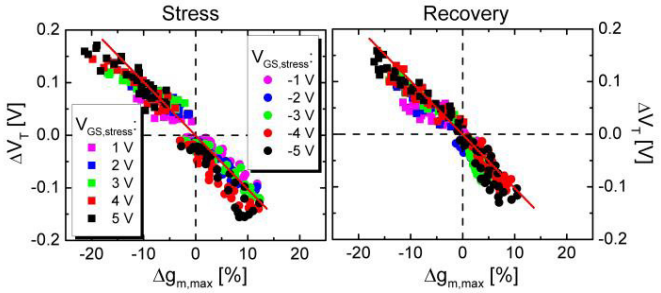

Fig. 4. Correlation between ΔV_T and $\Delta g_{m,\max}$ throughout stress and recovery for all PBTI and NBTI experiments at RT. The universal relationship that is obtained suggests a common physical origin.

during stress also shows minimal change (not shown). These observations are consistent with our earlier study of PBTI in similar devices [8].

For negative gate stress, the picture is nearly completely symmetric. ΔV_T is negative and its magnitude increases with stress time and the magnitude of stress voltage. $\Delta g_{m,\max}$ is positive and evolves in a similar way. Both ΔV_T and $\Delta g_{m,\max}$ are fully recovered after TD. ΔS is also minimal. All these observations are also consistent with our earlier NBTI work under moderate stress (labeled regime 1 in [9]). Note that for the highest stress voltages ($V_{\mathrm{GS,stress}} = -4$ and -5 V), a second regime of degradation causes a turnaround in the V_T evolution for long time. This was attributed in [9] to GaN substrate trapping and was labeled as regime 2. In this paper, we do not study this instability regime that prevails at higher negative gate voltages.

Fig. 4 shows the correlation of ΔV_T and $\Delta g_{m,\max}$ throughout the stress and recovery phases for $V_{\mathrm{GS,stress}}$ from -5 to 5 V at RT. The two parameters are closely correlated across all experiments following a continuous, linear relationship with a nearly constant slope. This symmetrical continuum strongly suggests that NBTI and PBTI in GaN MOSFETs under moderate stress are the result of a common reversible mechanism.

B. Impact of Temperature

We have also investigated the temperature dependence of ΔV_T under moderate positive and negative gate bias stress. Figs. 5 and 6 show the time evolution of ΔV_T and ΔS during stress and recovery for $V_{\mathrm{GS,stress}} = 2$ and -2 V at different T values. For PBTI, there appears to be a fast trapping phenomenon for very short stress times. Since we are limited to studies beyond 1 s, we cannot ascertain that it is saturated by then. Following [10], nevertheless, we assume that this is the case. To eliminate this effect, we examine the rate of ΔV_T change for $V_{\mathrm{GS,stress}} = 2$ V. We observe that ΔV_T increases faster during stress as T increases, and V_T recovery is also sped up by temperature, especially at $T = 20$ °C and 40 °C. For $V_{\mathrm{GS,stress}} = -2$ V, ΔV_T exhibits a stronger T dependence during stress but a weaker T dependence during recovery as compared with PBTI. ΔS is minimal for both PBTI and NBTI.

Fig. 7 shows Arrhenius plots for PBTI/NBTI stress and recovery dynamics. For the stress phase, we extract stress time needed to reach a certain ΔV_T at different T values ($\Delta V_T = 0.06$ V for PBTI and $\Delta V_T = -0.018$ V for NBTI). NBTI

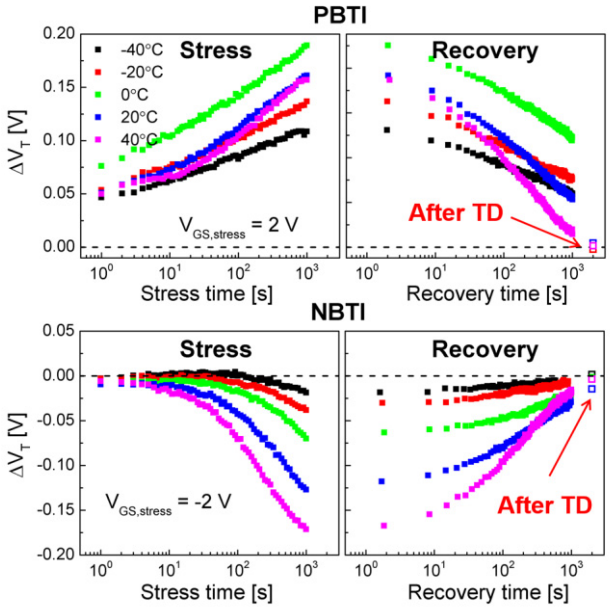

Fig. 5. Time evolution of ΔV_T during stress (left) and recovery (right) at different T values, for $V_{\mathrm{GS,stress}} = 2$ and -2 V. Open symbols at the end of the recovery represent final ΔV_T and ΔS values after TD.

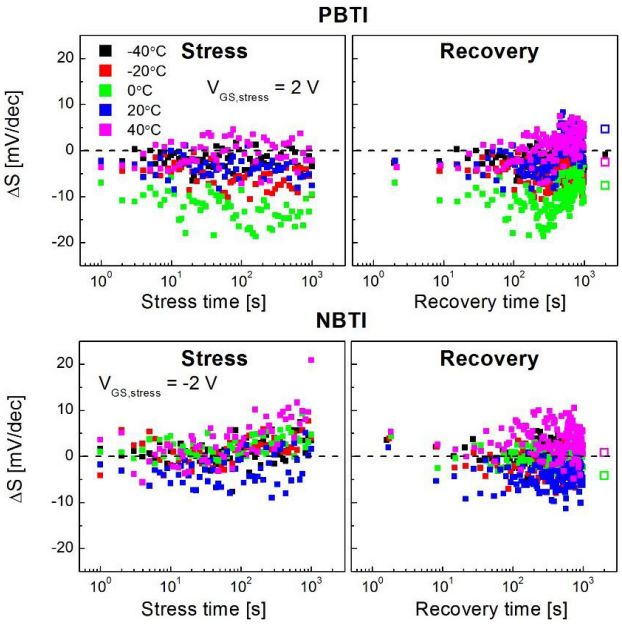

Fig. 6. Time evolution of ΔS during stress (left) and recovery (right) at different T values, for $V_{\mathrm{GS,stress}} = 2$ and -2 V. Open symbols at the end of the recovery represent final ΔV_T and ΔS values after TD.

stress has a clear T dependence with apparent $E_A = 0.37$ eV. PBTI shows time dispersion and does not have a clear T dependence. Nevertheless, we still show the Arrhenius plot as a reference. For recovery, we extract the recovery time needed for 50% ΔV_T recovery. PBTI recovery again does not show a simple picture, while NBTI has a weak T dependence with apparent $E_A = 0.056$ eV.

IV. Discussion

This paper reveals a symmetrical continuum of V_T shift and recovery as a result of gate stress voltage from -5 to 5 V at RT.

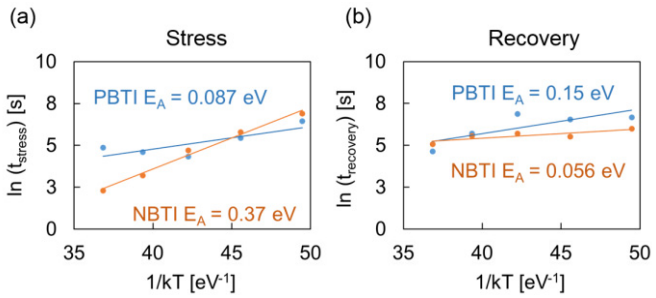

Fig. 7. Arrhenius plot of (a) stress time needed for ΔV_T to reach a fixed value during stress ($\Delta V_T = 0.06$ V for PBTI and $\Delta V_T = -0.018$ V for NBTI) and (b) recovery time needed for 50% ΔV_T recovery.

TABLE I
SUMMARY OF EMPIRICAL FITTING TIME EXPONENT VALUES

PBTI, RT

$V_{GS,stress}$ (V)	1	2	3	4	5
n	0.16	0.15	0.14	0.18	0.18

NBTI, RT

$V_{GS,stress}$ (V)	-1	-2	-3	-4	-5
n	0.5	0.45	0.40	0.40	0.46

PBTI, $V_{GS,stress}$ = 2 V

T (°C)	-40	-20	0	20	40
n	0.13	0.13	0.13	0.17	0.18

NBTI, $V_{GS,stress}$ = -2 V

T (°C)	-40	-20	0	20	40
n	0.77	0.71	0.55	0.56	0.56

We postulate that the positive V_T shifts during stress for PBTI and during recovery for NBTI are due to electron trapping in preexisting oxide traps. Furthermore, the negative V_T shifts during PBTI recovery and NBTI stress are due to electron detrapping from the same oxide traps.

It is well known that border traps exist inside Al_2O_3 gate dielectric close to the oxide–semiconductor interface in various MOS systems [16]–[18]. These border traps might be responsible for the reversible trapping/detrapping phenomena observed here. Because the trapping sites are close to the Al_2O_3–semiconductor interface, PBTI under moderate stress leads to channel mobility degradation through Coulomb scattering and a decrease in $g_{m,\max}$, with the contrary taking place during electron detrapping for NBTI.

We have observed that ΔV_T during stress follows a power law relationship with stress time and stress voltage. This is consistent with BTI observations in other GaN and Si technologies [11], [19], [20]. Following prior studies, we have modeled our results using the following relationship [11]:

$$\Delta V_T = A(V_{GS,stress} - V_{T0})^{\gamma} t_{stress}^{n} \quad (1)$$

where n is the time exponent, γ is the stress voltage exponent, and A is a constant. V_{T0} is the initial V_T of the device under test.

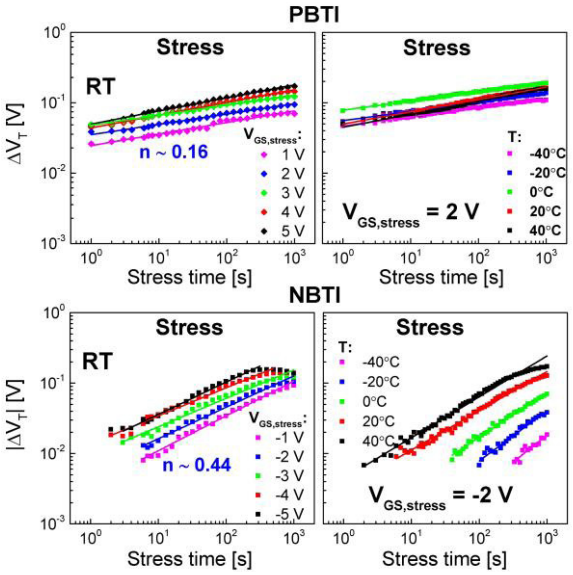

Fig. 8. Empirical fits for ΔV_T evolution with stress time at RT, for $V_{GS,stress}$ from −5 to 5 V (left), and at $V_{GS,stress} = 2$ and −2 V, for T from −40 °C to 40 °C (right). Symbols: experimental data. Solid lines: empirical fitting results.

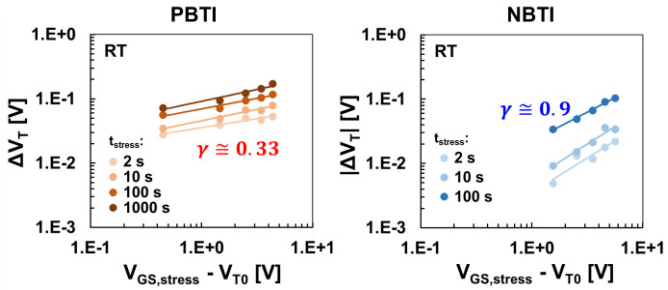

Fig. 9. Empirical fits for ΔV_T evolution with stress voltage at RT, for positive $V_{GS,stress}$ (left) and negative $V_{GS,stress}$ (right) at various t_{stress} values. Symbols: experimental data. Solid lines: empirical fitting results.

Fig. 8 shows the time dependence of ΔV_T during stress for $V_{GS,stress} = -5$ to 5 V at RT, and for $V_{GS,stress} = \pm 2$ V at various T values. n values used in the empirical fitting are summarized in Table I. At RT, $n \sim 0.16$ for PBTI stress and $n \sim 0.44$ for NBTI stress yield excellent fits to the entire data set, regardless of stress voltage. On the other hand, n increases with T ($n \sim 0.13$ to 0.18) for PBTI and decreases with T for NBTI ($n \sim 0.7$ to 0.5). Note that for NBTI at $T = 40$ °C, ΔV_T shows a different behavior as stress time approaches 1000 s as a result of GaN substrate trapping [9]. n values extracted for PBTI are close to those reported in the literature for high-k dielectrics [10], [11], [19], [21], while n values for NBTI are larger than the values reported in Si devices [13], [22].

Fig. 9 shows the ΔV_T dependence on gate stress overdrive at RT. Voltage-dependent exponents of $\gamma \sim 0.33$ for PBTI and $\gamma \sim 0.9$ for NBTI provide excellent fits for various t_{stress} values (ΔV_T for NBTI at t_{stress} approaching 1000 s shows a different behavior as a result of GaN substrate trapping [9]). Overall, PBTI stress produces larger $|\Delta V_T|$ than NBTI stress. This indicates that there are more oxide traps accessible under positive stress. The lower γ for PBTI is explained in the following.

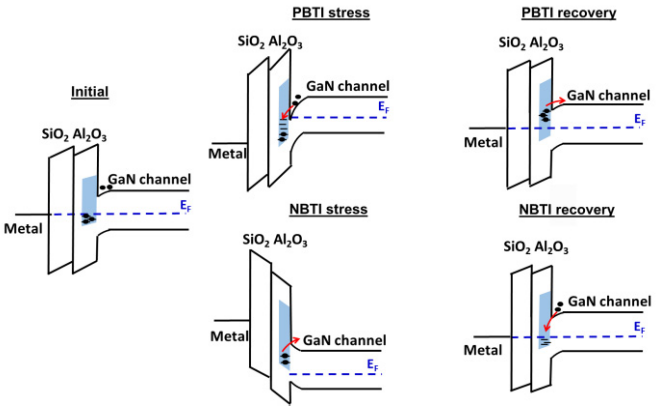

Fig. 10. Energy band diagram of GaN MOSFETs in equilibrium and under PBTI/NBTI stress and recovery. Electron trapping and detrapping from a single unified band of defects inside the Al_2O_3 barrier explains all results.

All these observations suggest a distribution of preexisting oxide traps in Al_2O_3 that is clustered in a band that spans from below the Fermi level at the surface of the GaN channel at zero bias to above the edge of the GaN conduction band, as sketched in Fig. 10 (blue band). During PBTI stress, empty trap states become aligned with the conduction band of GaN and channel electrons tunnel into them (hence the low apparent E_A). During PBTI recovery, trapped electrons tunnel back to the channel. During NBTI stress, the process is similar to PBTI recovery. Here, trapped electrons have to overcome an energy barrier before they can be emitted into the GaN conduction band, hence the larger observed apparent E_A (Fig. 7). During NBTI recovery, the mechanism is similar to that of PBTI stress, i.e., trap states available in the oxide and channel electrons tunnel into them (again, consistent with the low apparent E_A).

Because γ indicates how fast the number of accessible trapping/detrapping states changes with stress voltage [11], [19], the larger value of γ under NBTI stress, as compared with PBTI stress, arises from a density of trapping sites in the oxide that sharply increases for lower energies. The weak voltage acceleration of PBTI reflects a broad distribution of empty traps in the oxide above the channel Fermi level.

We eliminate the possibility of hole trapping under NBTI. This is because with a threshold voltage close to 0 V and given the large bandgap of GaN, at the moderate bias used in this paper, the hole supply is very limited.

Recently, the nonradioactive multiphonon process has been used to explain the relatively large activation energy found in Si BTI especially for the hole trapping/detrapping process [23]. In our case, even though we have also observed a temperature dependence for NBTI, the apparent activation energy is very small and an electronic-only picture provides a satisfactory explanation.

To gain further insight into BTI recovery, we stressed devices with $V_{GS,stress} = \pm 2$ V at RT for different stress times and traced the ΔV_T recovery as a function of time (Fig. 11). The starting data points represent ΔV_T values recorded right after the removal of stress. To model these recovery data, we used the well-studied universal recovery

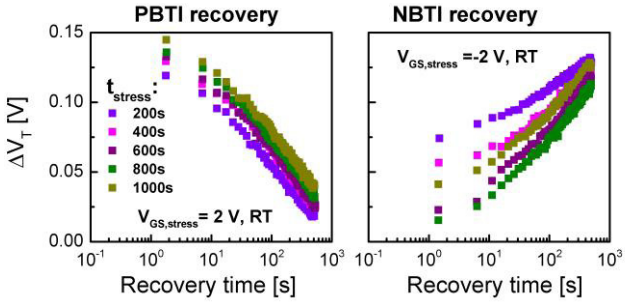

Fig. 11. Time evolution of ΔV_T recovery after PBTI (left) and NBTI (right) stress experiments at RT ($V_{GS,stress} = \pm 2$ V) with different t_{stress} values.

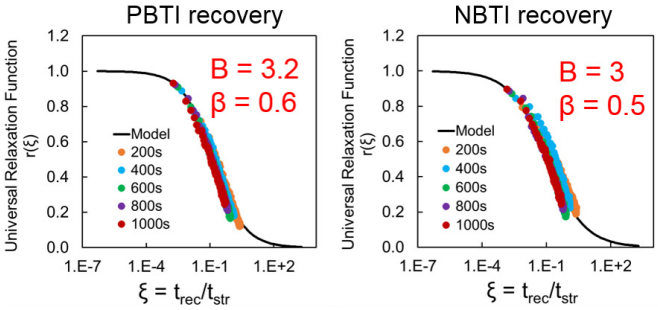

Fig. 12. Time evolution of ΔV_T recovery after PBTI (left) and NBTI (right) stress experiments at RT ($V_{GS,stress} = \pm 2$ V) with different t_{stress} values. Symbols: experimental values. Lines: model fitting results.

function [11], [24]

$$\Delta V_T(t_{stress}, t_{rec}) = \Delta V_T(t_{stress}, t_{rec} = 0) \times r(\xi) \quad (2)$$

with

$$r(\xi) = \frac{1}{1 + B\xi^{\beta}} \quad (3)$$

where t_{stress} is the stress time, t_{rec} is the recovery time, $\xi = t_{rec}/t_{stress}$ is the normalized recovery time, B is a prefactor, and β is a dispersion parameter. The model in (2) and (3) assumes no permanent degradation, which is the case in our experiments.

All recovery traces are fit with the model of (2) and (3) under the constraint that a single set of B and β values are used for all PBTI traces and NBTI traces, separately. Fig. 12 shows the model fitting result of the PBTI/NBTI recovery time function. Both PBTI and NBTI show a relatively well matched time evolution. $B = 3.2$ and $\beta = 0.6$ (PBTI) and $B = 3$ and $\beta = 0.5$ (NBTI) provide a good fit for all recovery data with different t_{stress} values. B values extracted here are close to those reported in the literature for GaN MIS-HEMT PBTI [11].

Fig. 13 compares the universal recovery function of PBTI versus NBTI. We observe a very similar relaxation behavior for positive and negative gate stress at RT. This suggests that both recovery processes reflect relaxation in a dispersive system. The slightly delayed relaxation after PBTI stress, with respect to NBTI relaxation, reflects the small energy barrier that electrons need to overcome during PBTI relaxation. This is not present during NBTI relaxation. These results are again

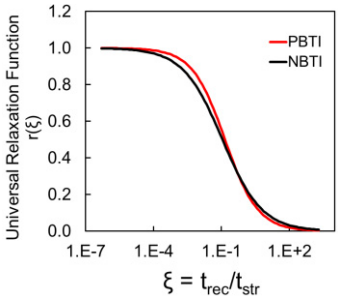

Fig. 13. PBTI and NBTI universal recovery function reveals similar recovery mechanism at RT.

consistent with our hypothesis of the same defect band being responsible for both mechanisms.

V. Conclusion

We have studied BTI in GaN MOSFETs under benign gate bias stress. V_T shift shows a symmetric continuum when $V_{GS,stress}$ is increased from -5 to 5 V at RT, and the shift is recoverable. Our findings suggest that electron trapping/detrapping in/from the same preexisting oxide traps is responsible for the observed V_T instability under benign gate bias stress.

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