Optimized Toroidal Inductors Versus Planar Spiral Inductors in Multilayered Technologies

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***Abstract*— This paper is aimed to compare the performance of toroidal inductors and planar spiral inductors in multilayered technologies, in terms of achievable inductance density. The optimization of planar toroidal inductors in multilayered substrates is investigated theoretically, and closed formulae are derived for their inductances as a function of geometrical parameters. The obtained model is validated by experimental results and electromagnetic simulation. From the comparison of the inductance of toroidal inductors and compact spiral inductors, a selection rule is proposed to choose the most suitable topology that leads to the most compact design.**

***Index Terms*— Inductance calculation, inductor design, inductor selection rules, magnetic passive components, toroidal inductor, toroidal inductor optimization.**

I. Introduction

TOROIDAL inductors and transformers in discrete form are widely used in low frequency power electronics applications. One prime example of such applications is power conversion. The increase in switching frequency allows greater compactness and better performance of power converters [1], [2]. Increasing the switching frequency means less demand for energy storage and consequently smaller values of passive components. However, it is not clear how the sizes of passive components scale down with increasing frequency, without degrading their overall performances. This fact is particularly important in the case of magnetic components, such as toroidal inductors and transformers, because of their relatively big sizes, far larger than the other parts in the converter system.

In the RF band of the electromagnetic (EM) spectrum, planar spiral inductors have been widely used in the design of radio frequency integrated circuits, intended to work in the GHz range and beyond [3], [4]. The main concern when using these passive components is area consumption. Scaling-down frequency from the GHz range means the need for higher values of inductance that can only be achieved by increasing the number of turns of the coils. This leads to an increase in losses and integration area, which makes their use less attractive.

According to this, at intermediate frequencies that are likely to become relevant for future power switching applications based on novel GaN power transistors, it is not clear which of these inductor designs, toroidal or planar spiral, is preferable. These intermediate frequencies would roughly correspond to very high frequency band, from tens of MHz to a few hundreds of MHz. However, there are not yet clear criteria on what inductor topology to choose for a given application. Contributing to the establishment of such criteria is one of the main objectives of this paper.

When comparing toroidal inductors with planar spiral inductors, we have to be sure that the best candidates for both the topologies are selected. For instance, square, hexagonal, octagonal, and circular planar spiral geometries have been studied in terms of related inductance [5]. Hollow inductor geometry [6] and tapered inductor geometry [7] have also been considered. If we focus on achieving the highest possible inductance density (i.e., achievable inductance over the volume required to implement the component), the compact planar spiral inductor would be the best candidate of its kind. However, it is not clear which would be one of the toroidal inductors. The optimization of the design of toroidal inductors has been considered previously [8]. In this seminal paper, the problem of achieving the highest inductance with the shorter length of wire is addressed. In this paper we deal with planar toroidal inductors fabricated using multilayered technologies. Wire length is no longer a concern. Now, metal strip, width and pitch, number or turns, and distance between via holes are the key geometrical parameters. Determining the optimum toroidal inductor geometry to achieve the highest possible inductance density is also a main objective of this paper.

This paper is an expanded version of [9]. A more in-depth analysis of the toroidal geometry as well as new experimental and simulation results are presented to reinforce the soundness and accuracy of this paper.

This paper is divided as follows. In Section II, the model of toroidal inductors in multilayered technologies is presented. Closed formulae for the inductance of the component as a function of geometrical parameters are derived from a theoretical analysis. As a result, an optimum inductor geometry is proposed to maximize the achievable inductance density. Section III of this paper briefly considers the comparison between toroidal and planar spiral inductor modeling. As a result, inductor selection rules as a function of geometrical

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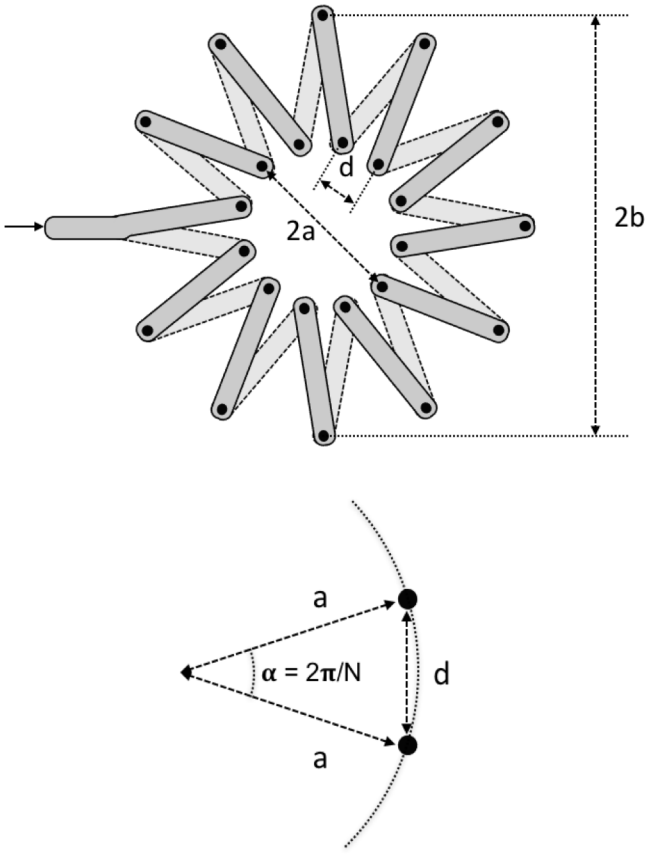

Fig. 1. Top: schematic of a toroidal inductor in multilayer technology. Bottom: relationship between main geometrical parameters.

parameters are derived and discussed. Section IV presents experimental data and EM simulation results for both inductor topologies. The obtained results validate the proposed toroidal inductor model, as well as the proposed inductors selection rules. In Section V, the application of selection rules to find optimum inductor designs for different standard multilayered technologies is discussed. Finally, Section VI concludes this paper.

II. Multilayer Toroidal Inductor Modeling

Fig. 1 shows an example of a toroidal inductor constructed using strips on the top and bottom surfaces of a multilayer substrate. Via holes through the substrate are used to close each turn. On the left-hand side, a via hole is removed to provide a feed point for current injection. Provided the number of turns is high enough (i.e., $N >> 1$), the inductance of this toroid is given as [10], [11]

$$L = \mu \frac{N^2 h}{2\pi} \ln\left(\frac{b}{a}\right) + L_o \tag{1}$$

where μ is the substrate permeability, N is the number of turns, h is the substrate thickness, a and b are the inner and outer radii, respectively, and L_o, is the inductance of the spur-shaped loop that remains when the substrate thickness h collapses to zero. To calculate L_o, the usual approximation consists in assuming that the spur-shaped loop behaves like an average circular loop [12]. Under this assumption, the inductance L_o is given as

$$L_o = \mu \frac{b+a}{2} \left[\ln\left(8\frac{b+a}{b-a}\right) - 2\right]. \tag{2}$$

The contribution of L_o to the overall inductance used to be small in comparison with the first term in (1) and usually can be neglected in a first approach.

Expression (1) can be rewritten in a more convenient way if we perform an in-depth analysis of the toroid geometry shown in Fig. 1. The most important parameter is the minimum distance between via holes d. For instance, given a number of turns N and the inner radius a of the toroid, it holds that

$$a = \frac{d}{2\sin\left(\frac{\pi}{N}\right)} \tag{3}$$

which can be approximated by

$$a \approx \frac{Nd}{2\pi}. \tag{4}$$

The error of the value given by (4) with respect to the exact value given by (3) is less than 5% when $N \geq 6$.

According to (4), the inner radius a increases as N. Taking into account that the upper limit of the inner radius a is the outer radius b, then the maximum number of turns of the toroid, $N_{\max}$ can also be related to the design parameter d according to the following expression:

$$b \approx \frac{N_{\max} d}{2\pi}. \tag{5}$$

In (5), we also assume $N_{\max} \geq 6$. Combining (4) and (5) the relationship between a, b, N, and $N_{\max}$ can be found as

$$R = \frac{a}{b} \approx \frac{N}{N_{\max}}. \tag{6}$$

Therefore R is either the ratio between the number of turns and the maximum number of turns, or the ratio between the inner and outer radii of the toroid.

Replacing (4), (5), and (6) into (1) we finally obtain the following expression for the inductance:

$$L = \mu \frac{V}{d^2} R^2 \ln\left(\frac{1}{R^2}\right) + L_o \tag{7}$$

where V is the total volume occupied by the toroid, which is equal to

$$V = \pi b^2 h. \tag{8}$$

If we neglect the effect of L_o the inductance given by (7) shows a maximum value $L_{\max}$ given as

$$L_{\max} = \mu \frac{V}{d^2 e} \tag{9}$$

where e is Euler's number. The inductance maximum is achieved for an optimum value of the ratio R given as

$$R_{\text{opt}} = \frac{1}{\sqrt{e}} = 0.6065\ldots. \tag{10}$$

Fig. 2 shows the inductance according to (7) normalized to its maximum $L_{\max}$ as a function of R. The influence of L_o is removed. The insets in the plot are schematic views of the inductor geometries corresponding to different values of R.

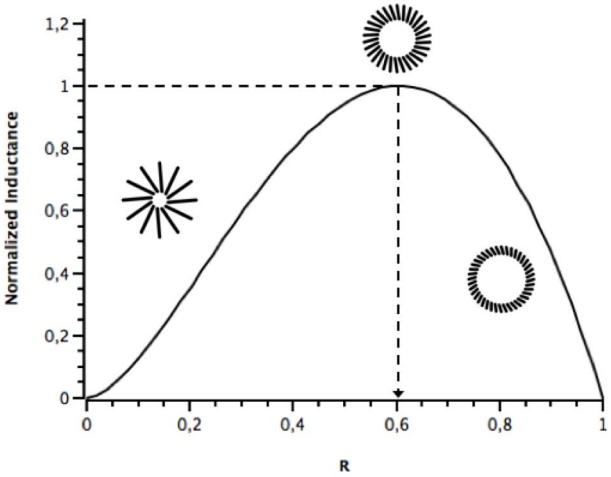

Fig. 2. Normalized inductance plot of a toroidal inductor as a function of the geometrical ratio R. Insets: layout views of the inductors for different values of R.

Note that values of $R > R_{\max}$ lead to inductor geometries with a big empty area in the center. On the contrary, values of $R < R_{\max}$ lead to inductor geometries with empty space in the periphery. In both the cases, the consequence is a decrease of the inductance with respect to the maximum.

According to this, for a given size (i.e., volume) of the toroidal inductor, the equivalent inductance achieves its maximum value when the inner radius a is about 60%–61% of the external radius b, regardless of the number of turns or metal strip width.

III. Toroidal Versus Planar Spiral Modeling

To point out the advantages or disadvantages of using multilayer toroidal inductors, it is mandatory to compare their performances with those of planar spiral inductors. Planar spiral inductors of different shapes (i.e., circular, octagonal, or square) have been used for decades in integrated and/or multilayer technologies [3]–[6]. There is a vast literature available concerning the modeling of planar spiral inductors, including measurement fitting modeling, numerical simulations, and closed analytical formulae [13]. For the comparison we are going to use a proposed closed formula for planar spiral inductors that has shown to be rather accurate [5]. According to this paper, the inductance of planar spirals can be written as

$$L = \mu \frac{N^2 d_{\text{avg}} c_1}{2} \left[\ln\left(\frac{c_2}{\rho}\right) + c_3 \rho + c_4 \rho^2 \right]. \tag{11}$$

This formula can be applied to different spiral shapes, as long as the correct set of parameters c_1, c_2, c_3, and c_4, is selected. For comparison sake we will focus on the circular spiral case, which corresponds to $c_1 = 1$, $c_2 = 2.46$, $c_3 = 0$, and $c_4 = 0.2$. The schematic view of a circular planar spiral is depicted in Fig. 3. The rest of the parameters in (11), N, d_{avg}, and, ρ are also related to the inductor geometry. N identifies the number of turns of the spiral, and parameters d_{avg} and ρ are dependent on the inner d_i and outer d_o dimensions of the spiral, as follows:

$$d_{\text{avg}} = \frac{d_o + d_i}{2} \tag{12}$$

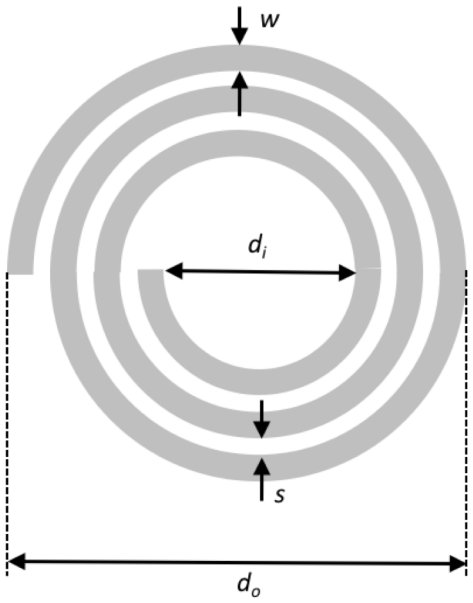

Fig. 3. Schematic of a circular planar spiral inductor.

and

$$\rho = \frac{d_o - d_i}{d_o + d_i}. \tag{13}$$

In [5], the parameter ρ is called the "*fill factor*" because it quantifies the coverage of the allowed area by the spiral. For instance, a compact spiral covering the whole allowed area would correspond to the case $\rho = 1$ or $d_i = 0$. From all circular spirals, the compact geometry has the highest inductance. For this inductor (11) can be rewritten as

$$L_{\max} = k \mu N^2 \frac{d_o}{2} \tag{14}$$

where $k = 0.55$.

Comparing Figs. 1 and 3, we can establish the following correspondences:

$$\begin{cases} d_o = 2b \\ d_i = 2a \\ w + s = d \\ Nd \approx b - a. \end{cases} \tag{15}$$

For comparison purposes, replacing (15) into (14) in the compact case (i.e., $d_i = 0$, or, $a = 0$) leads to a more convenient expression of the inductance

$$L_{\max} = k \mu \frac{Sb}{\pi d^2}. \tag{16}$$

The parameter S is the total area occupied by the spiral, which is given as

$$S = \pi b^2. \tag{17}$$

Let us now compare the inductance of the compact spiral, given by (16) and (17), with the maximum inductance of a toroid, given by (8) and (9). There is a different behavior of the inductances with respect to the external radius b. In the case of the spiral, the inductance is proportional to b^3. On the contrary, for the toroid the inductance is proportional to b^2. Accordingly,

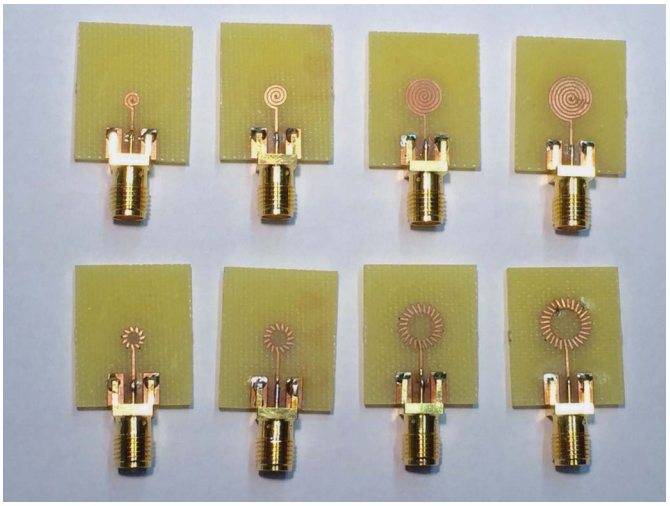

Fig. 4. Top: prototype examples of PCB spiral. Bottom: optimum toroidal inductors.

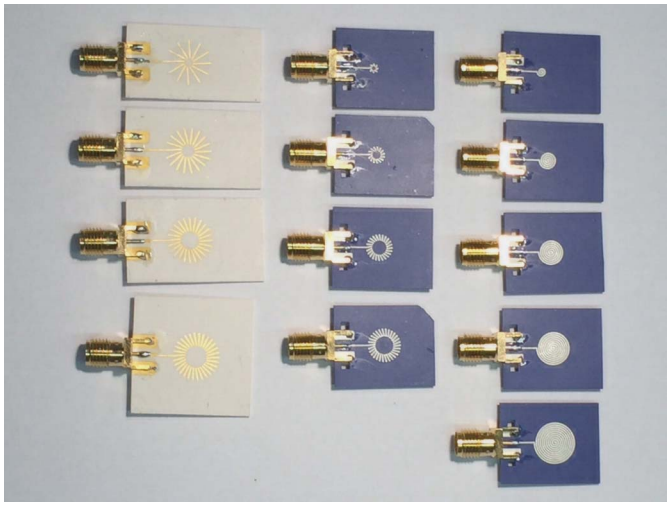

Fig. 5. Example of LTCC inductor prototypes. Left (first column): using Themex ceramics technology. Right (two next columns): using Heraeus technology.

for small values of b, a higher inductance density is expected for the toroidal topology than for the spiral topology, and vice versa. To determining the crossing point between these two behaviors we have calculated the ratio between both the inductances. It is easy to find that

$$\frac{L_{\max-\text{spiral}}}{L_{\max-\text{toroidal}}} = k\frac{e}{\pi}\frac{b}{h} \tag{18}$$

where b/h is the aspect ratio of the inductors cross section.

The crossing point at an inductance ratio equal to unity determines a threshold for the aspect ratio, which is equal to

$$\frac{L_{\max-\text{spiral}}}{L_{\max-\text{toroidal}}} = 1 \Longrightarrow \left.\frac{b}{h}\right|_{th} = e\frac{\pi}{k} = 2.1. \tag{19}$$

Consequently, when $b/h < 2.1$, then the toroid outperforms the circular planar spiral in terms of achievable inductance. On the contrary, when $b/h > 2.1$, then the circular planar spiral outperforms toroid. This result stablishes a general selection rule that must be validated experimentally.

IV. Experimental and EM Simulation Results

The set of samples studied in this paper consist of toroidal and planar spiral inductors fabricated using the standard FR4 printed circuit board (PCB) technology and low temperature cofired ceramic (LTCC) technology. A design of experiments, varying geometrical parameters, has been performed to obtain all the required inductors prototypes to validate all aspects of the previous theoretical study.

A. Sample Preparation

Fig. 4 shows examples of the obtained PCB inductors. Fig. 5 shows inductor prototypes fabricated using two LTCC technologies, from Themex Ceramix (white) and Heraeus (blue). In the case of toroidal inductors, the most important design parameter is the minimum distance between adjacent via holes d, which is equal to 600 μm for PCB inductors and 500 μm for LTCC inductors. The width of the metal traces w is equal to 450 and 300 μm, respectively. The minimum metal-to-metal spacing s is equal to 150 μm using PCB and 200 μm using LTCC. In the case of spiral inductors, the most important design parameter is the pitch, which is equal to $p = w + s$. For comparison purposes, w and s are kept constant all over the spiral, and equal to their minimum values, so that $p = d$. The via hole diameter is equal to 300 μm, using PCB technology, and 150 μm, using LTCC technology. To study the effect of the substrate thickness h, three equal sets of PCB toroidal inductors have been fabricated. The first one corresponds to a substrate thickness $h = 1.57$ mm and the second to $h = 0.83$ mm. To account for the case corresponding to $h \approx 0$, the third set of samples has been obtained by merging the top and bottom layers of the toroid on the top surface of the PCB. This design is depicted in Fig. 6. On the left-hand side of the figure, there is a toroid performed using a 1.57 mm thick PCB substrate. On the right-hand side we can see the same inductor when the substrate thickness is $h \approx 0$. The result is a spur-shaped loop that will also contribute to the overall inductance. Only one via hole is kept to connect the right extreme of the loop with the ground line on the bottom layer.

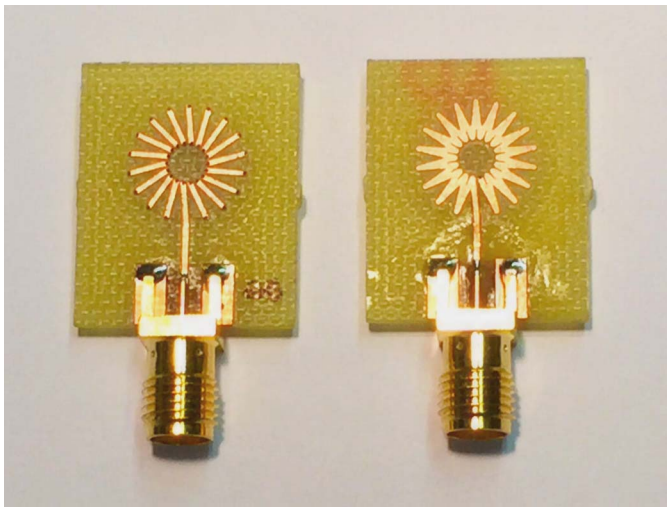

Fig. 6. PCB single-winding toroidal inductor. Left: using a substrate thickness $h = 1.57$ mm. Right: same inductor corresponding to the limit $h \approx 0$.

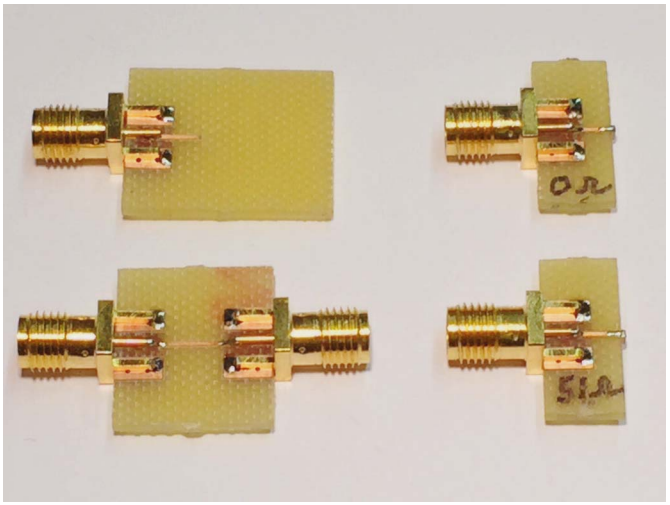

Fig. 7. PCB custom calibration kit for de-embedding SMA connector and pad effects from the inductor measurements. Clockwise from top-left: open, short, broadband load, and thru.

Fig. 7 shows one of the custom calibration kits that have been fabricated to de-embed the effects of the SMA connector and pads from the inductor measurements. Clockwise from the top-left corner of the figure, the custom kit consists of open, short, broadband load, and thru. Short and load standards have been fabricated by connecting a surface mount device (SMD) resistor on the edge of the PCB board. A 0 Ω resistor is used for the short, and a 51 Ω resistor for the broadband load. SMD 0603 and SMD 0402 resistors have been used with the 1.57 mm thick and the 0.83 mm thick PCB substrates, respectively.

B. Measurement and Simulation Setups

S parameters have been measured for the whole set of PCB and LTCC inductors and for the custom calibration kits using E5071B Vector Network Analyzer (VNA) from Keysight Technologies (formerly Agilent Technologies).

Prior to the measurements the VNA is precalibrated using an N4431-60003 electronic calibration module, also from Keysight Technologies. Then the S parameters of the inductor samples and the standards of the custom calibration kit are measured from 300 kHz to 1 GHz. The de-embedding of the SMA connector and pads is performed using Advanced Design System from Keysight Technologies. This design environment is also used for further analysis of the data.

Fig. 8 shows an example of inductor measurements. In the figure the equivalent inductance and the quality factor of a 24 turns LTCC toroidal inductor are plotted as a function of frequency. Raw data before de-embedding of SMA connector and pads (thin red line) and data after de-embedding (thick black line) are shown together on the same graph. The inset of the figure depicts the footprint view photograph of the inductor. The SMA connector and pads introduce a parasitic series inductance and parallel capacitance. The removal of the parasitic series inductance after de-embedding is responsible for a decrease Δ_L, of the equivalent inductance of about 7 nH. The removal of the parasitic parallel capacitance leads to an

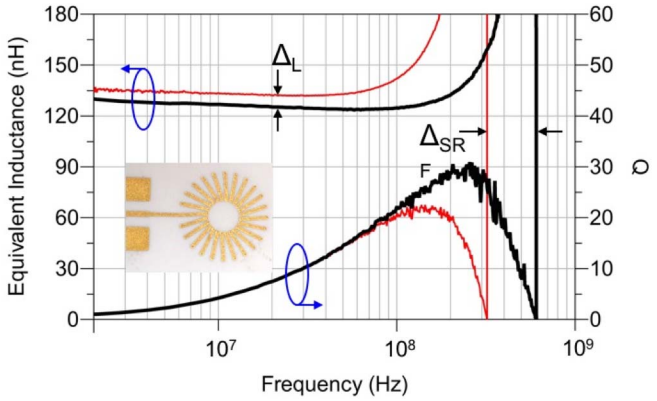

Fig. 8. Equivalent inductance and quality factor as a function of frequency for an LTCC toroidal inductor. Thin red line: raw data before de-embedding of SMA connector and pad effects from the measurements. Thick black line: data after de-embedding.

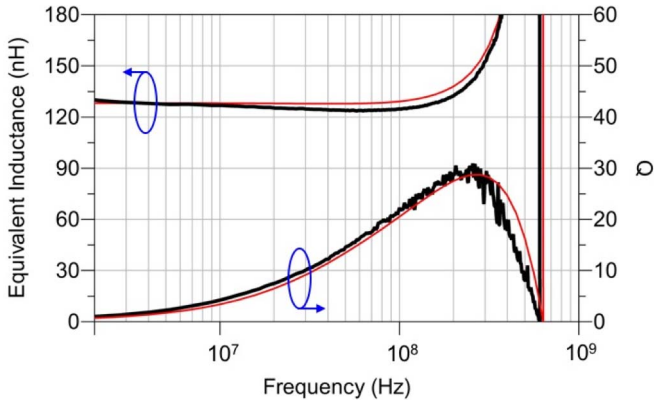

Fig. 9. Equivalent inductance and quality factor as a function of frequency for an LTCC toroidal inductor. Thick black line: data after de-embedding of SMA connector and pad effects from the measurements. Thin red line: momentum simulation.

increase Δ_{SRF}, of the self-resonant frequency (SRF) of about 300 MHz. The maximum quality factor also increases, from about 22–30, but this is just a consequence of the increase in SRF.

EMs have been performed using momentum planar solver from Keysight Technologies. To account for magnetically induced losses on the metal traces [7] and other parasitic effects, thick metal and edge mesh option has been used in all the simulations. Fig. 9 shows an example of the obtained results for the same LTCC inductor in Fig. 8. The equivalent inductance and quality factor are plotted as a function of frequency. The thick black line corresponds to experimental data after de-embedding of SMA connector and pads effects. The thin red line corresponds to the EM simulation results obtained using momentum planar solver. Note the good agreement between experiment and simulation, particularly at low frequency.

C. Toroidal Inductor Results

Fig. 10 shows the quasi-static inductance as a function of the number of turns N for a subset of PCB toroidal inductors studied in this paper. The external radius is $b = 4.7$ mm in all the cases. The internal radius a is given by (3).

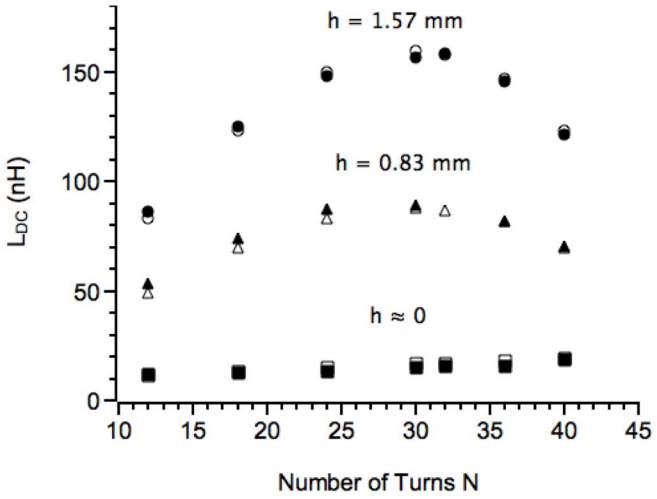

Fig. 10. Plots of the quasi-static inductance of PCB toroidal inductors as a function of the number of turns N. Solid symbols: experimental measurements. Outlined symbols: simulation results. Circles: results for substrate thickness $h = 1.57$ mm. Triangles: $h = 0.83$ mm. Squares: $h \approx 0$.

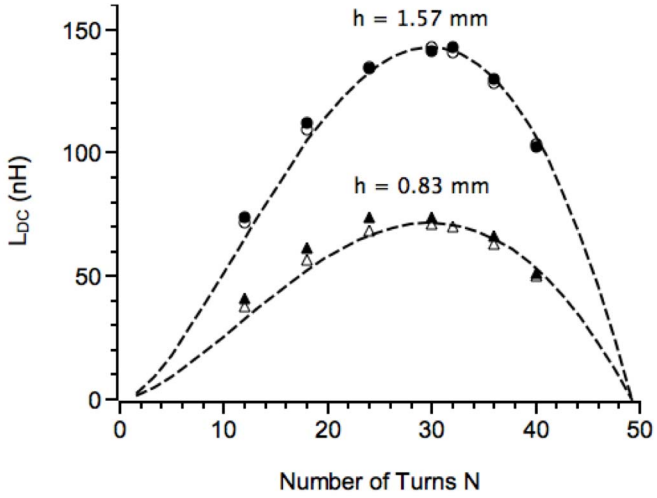

Fig. 11. Corrected values of the quasi-static inductance of PCB toroidal inductors after removal of the spur-shaped loop inductance L_o. Solid symbols: experimental measurements. Outlined symbols: simulation results. Circles and triangles: results for substrate thicknesses $h = 1.57$ mm and $h = 0.83$ mm, respectively. Dashed lines: theoretical curves given by (7) without considering the effect of L_o.

The number of turns is $N = 12$, 18, 24, 30, 32, 36, and 40. The experimental and simulation results for three substrate thicknesses h are plotted together in the same figure. Data obtained from experimental measurements are plotted using solid symbols. Outlined symbols are used for plotting data obtained from simulation.

In order to compare these results with the previous theoretical study carried out in Section II, we need to remove from the quasi-static inductance values the effect of L_o. This can be done by subtracting the quasi-static inductance values corresponding to $h \approx 0$ from the values corresponding to $h = 1.57$ mm and $h = 0.83$ mm. Fig. 11. shows the result. The experimental and EM simulation corrected data are plotted together with the theoretical curves given by (7) without considering the effect of L_o. It is important to remark the

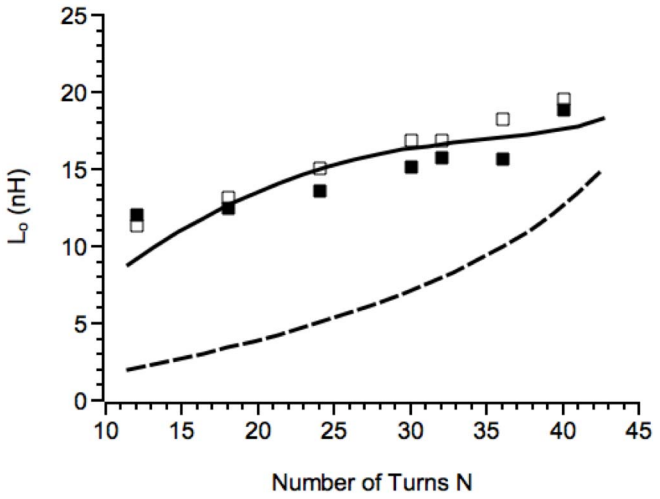

Fig. 12. Inductance L_o as a function of the number of turns of PCB toroidal inductors. Solid squares: experimental measurements. Outlined squares: simulation results. Dashed curve: values derived from the average circular loop model. Continuous line: values derived from the proposed corrected model.

good agreement between data and theory, particularly since there are no fitting parameters.

The expected values of L_o derived from (2) are plotted in Fig. 12 (dashed curve), together with experimental and simulated data (square symbols). It is clear from the figure that (2) underestimates the quasi-static loop inductance for all the values of the number of turns we have considered. According to this, the assumption that the spur-shaped loop behaves like an average circular loop is not valid, it is just a first approximation. Additional corrections are required to improve the accuracy of the model. To do so, we have to keep in mind that the main difference between the spur-shaped loop and the average circular loop is an extra length of the metal trace. Taking this into account, we propose a correction directly proportional to the extra length of the loop with respect to the average circle. It is important to note that the perimeter of the spur-shaped loop is not a linear function of the number of turns N. For a given value of the external radius b, the perimeter P of the loop is given as

$$P = 2N\sqrt{(b-a)^2 + \left(\frac{d}{2}\right)^2}. \tag{20}$$

Note that internal radius a is also a function of N, according to (3) or (4). The perimeter of the average circular loop P_o is simple given as

$$P_o = \pi(a+b). \tag{21}$$

The perimeter given by (20) is plotted together with the perimeter of the average circular loop given by (21) in Fig. 13. There is a big difference in perimeter $\Delta P = P - P_o$, for most values of the number of turns N. It initially increases as N increases, then it reaches a maximum, and finally it decreases as N continues to increase. Eventually, ΔP goes to zero for a maximum number of turns. To explain this behavior, we have to consider the ratio between radii a and b. For small values of N (i.e., $a << b$), any additional turn adds a spike to the

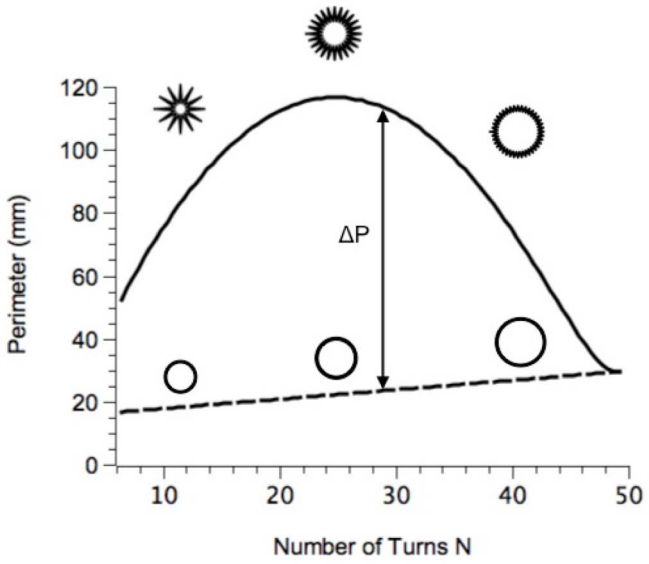

Fig. 13. Continuous line and dashed line: perimeters of the spur-shaped loop and average circular loop, respectively, as functions of the number of turns N. External radius $b = 4.7$ mm. Insets: schematic footprints of the loops for different values of N.

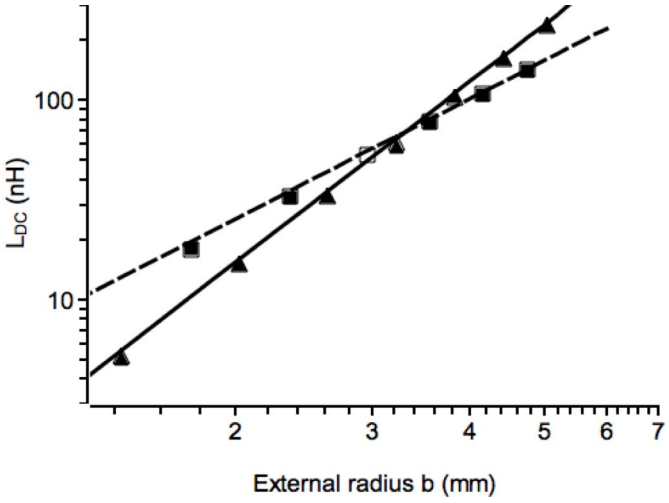

Fig. 14. Quasi-static inductance of PCB inductors as a function of the external radius b. Solid symbols: experimental measurements. Outlined symbols: simulation results. Squares: optimum toroidal inductor results corrected from L_o. Triangles: spiral inductor results. Dashed line: theoretical dependence given by (8) and (9). Continuous line: closed formula for circular spiral inductors given by (16) and (17) and derived from [5].

spur-shaped loop. The total increase in perimeter is about $2b$. On the contrary, the perimeter of the average circular loop weakly increases. For big values of N (i.e., $a \approx b$), any additional turn rounds the spur-shaped loop, decreasing its perimeter. At the end the spur-shaped loop becomes a circular loop of radius b, which is equal to the average circular loop. According to the discussion above, we propose the introduction of a correction term to calculate L_o directly proportional to ΔP as

$$L_o = \mu \frac{b+a}{2}\left[\ln\left(8\frac{b+a}{b-a}\right) - 2\right] + l\,\Delta P \qquad (22)$$

where the fitting parameter l is an inductance per unit length. The results given by (22) are shown as a continuous line in Fig. 12. A good fit of both the experimental and simulated results is observed using $l = 105$ pH/mm.

D. Toroidal Versus Spiral Results

Two sets of compact spiral inductors of different sizes have been designed and fabricated using PCB and LTCC technologies. These sets have been compared with two other sets of toroidal inductors having similar sizes and the optimum ratio R_{opt}, so that the dc equivalent inductance reaches its maximum. Some of the fabricated devices are shown in Figs. 4 (PCB) and 5 (LTCC, Heraeus samples in the middle and right columns). In Fig. 14, an example of the quasi-static inductance of PCB devices is plotted against the external radius b. Solid symbols correspond to experimental measurements. Outlined symbols correspond to simulation results. Squares correspond to optimum toroidal inductor results corrected from L_o and triangles correspond to spiral inductor results. The dashed curve is the theoretical dependence given by (8) and (9), which varies as b^2. The continuous curve corresponds to the closed formula for circular spiral inductors

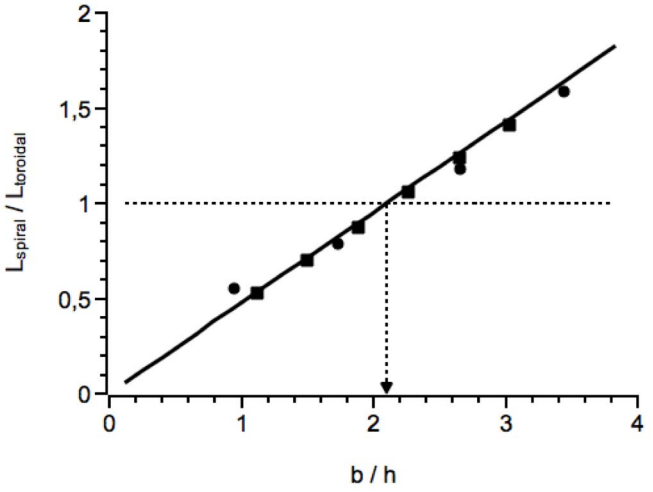

Fig. 15. Quasi-static inductance ratio of spiral and toroidal inductors as a function of the inductor aspect ratio b/h. Squares: data for PCB inductors. Circles: LTCC inductors. Continuous line: lineal behavior given by (18). Arrow: threshold value of 2.1 derived from theoretical analysis.

given by (16) and (17) and derived from [5], which is dependent on b^3. Good agreement is observed between experiments, simulations, and theory. As expected, we can clearly see a different behavior for both the inductor topologies. In this case, we can observe a cross point for an external radius b $\approx$ 3.3 mm. Below this value, the equivalent inductance of a toroidal inductor is bigger than that of a compact spiral of the same size, and vice versa.

Finally, Fig. 15. shows the ratio between the quasi-static inductance of spiral and optimum toroidal inductors as a function of the inductor aspect ratio b/h for both the PCB and LTCC technologies. To obtain the quasi-inductance ratios at the same value of b/h, data corresponding to the spiral inductors have been fit with a third-order polynomial of b,

and then interpolated. In the same figure the theoretical linear dependence given by (18) is also shown. Once again, good agreement is observed between measurements, simulations, and theory. As expected, below the threshold value of the ratio $b/h = 2.1$, the inductor topology of choice to achieve the highest inductance density is the toroid. Conversely, above the threshold spirals outperform toroidal counterparts.

V. Technology Effects on Inductor Selection Rules

The comparison in terms of achievable inductance of both the inductor designs (i.e., planar spiral inductor and toroidal inductor) reveals that the key parameter is the aspect ratio b/h. The outer radius b is a design parameter. It can be selected by the designer in order to scale the inductor geometry. On the contrary the substrate thickness h is a technological parameter. Usually, it is not accessible by the designer. According to this, from the point of view of inductor design, the different technologies should be classified by the substrate thickness. For instance, if we consider an integration technology consisting of a semiconductor bulk with thin intermetal dielectric layers on it, the aspect ratio for most components will be very large, and the natural choice for implementing inductors would be a planar spiral geometry. On the contrary, when using thick intermetal dielectrics or multilayered technologies like LTCC or even PCB the choice is not so clear. It is in this case that depending on the required inductance value the application of the selection rules reported in this paper will give us the optimum inductor design.

VI. Conclusion

In this paper a model of embedded toroidal inductors in multilayered technologies is proposed and validated by experimental data and simulation results. The model predicts the whole quasi-static inductance of the component. In addition to the inductance of the toroidal geometry, the proposed model also includes a new approach for modeling of the inductance of the spur-shaped loop, resulting when the substrate thickness trends to zero.

We can extract some general conclusion from our theoretical analysis and experimental and simulation results. The first is that it is possible to optimize the geometry of toroidal inductors to improve the maximum achievable inductance. The second is that the key parameter to decide whether to use a planar spiral inductor or a toroidal inductor is the aspect ratio b/h. Inductor selection rules have been derived and experimentally validated to obtain the optimum designs that maximize the inductance density. The application of the selection rules using different multilayered technologies has also been discussed. As far as we know, this is the first proposed procedure to decide whether to use planar spiral or toroidal inductor geometry, for a given requirement of inductance value and fabrication technology. Further work is under progress to compare other characteristic parameters of these structures, particularly the quality factor and the SRF, to establish additional selection rules.

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