Gate Bias and Geometry Dependence of Total-Ionizing-Dose Effects in InGaAs Quantum-Well MOSFETs

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***Abstract*— The effects of total-ionizing-dose irradiation are investigated in HfO_2/InGaAs quantum-well MOSFETs. Radiation-induced hole trapping is higher for irradiation under positive gate bias than under negative gate bias. Electrical stress-induced electron trapping compensates radiation-induced hole trapping during positive gate-bias irradiation. Stress-induced hole trapping adds to the effects of radiation-induced hole trapping under negative gate bias. Radiation-induced charge trapping increases with the channel length.**

***Index Terms*— III-V, InGaAs, MOSFETs, positive bias temperature instability (PBTI), total ionizing dose (TID).**

I. Introduction

SEVERAL III-V materials, due to their high electron mobility and high injection velocity, are promising channel candidates for future logic applications [1]. In particular, the InGaAs MOSFET is considered to be a leading candidate for the n-channel device for sub-10 nm CMOS technology nodes [2]. In addition to higher carrier mobility, the quantum-well architecture in these devices is advantageous for scalability [3], [4] and the favorable band alignment avoids carrier bottlenecks that limit the ability to realize the full benefits of the material in many other III-V based structures [5]. To operate in space environments, InGaAs MOSFETs must be able to withstand ionizing radiation.

Similar to III-V MESFETs/HEMTs, III-V MOSFETs are sensitive to single event effects due to charge enhancement effects [6], [7]. However, in contrast with the resistance against total-ionizing-dose (TID) effects of III-V MESFETs/HEMTs, III-V MOSFETs are vulnerable to TID effects [8], [9], [10]. Preliminary TID effects have been reported in InGaAs planar MOSFETs [8], gate-all-around MOSFETs [9], as well as AlGaN/GaN MOS-HEMTs [10]. All of these devices, though, use a thick Al_2O_3 oxide with an effective oxide thickness (EOT) of approximately 5 nm, which is too thick to be applied in the sub-10 nm node. In this paper, we investigate total-ionizing-dose (TID) effects in InGaAs quantum-well MOSFETs with a thin (physical thickness of 2.5 nm) HfO_2 gate dielectric, which is more relevant for future CMOS applications.

High densities of defect states at the high κ/semiconductor interface and in the high κ layer also can cause positive bias temperature instability, especially in InGaAs MOSFETs [11], [12], [13]. Hence, it is important to separate the TID response from effects produced by electrical bias in these structures. In this work, we evaluate the gate bias and geometry dependence of TID and bias-stress effects for InGaAs quantum-well MOSFETs with thin HfO_2 gate dielectrics. Irradiation and stress effects on threshold voltage are additive or partially offsetting, depending on gate bias. The magnitude of the changes in threshold voltage increases with channel length.

II. Experimental Setup

The devices considered here are self-aligned InGaAs quantum-well MOSFETs. The detailed fabrication process is described in [14]. Fig. 1(a) shows a schematic cross section of the device (not drawn to scale). A 0.4 μm thick $In_{0.52}Al_{0.48}As$ buffer layer is grown on a 600 μm thick semi-insulating InP substrate. A 5 nm thick $In_{0.7}Ga_{0.3}As$ channel is grown on top of the buffer layer, which is capped by an InP barrier layer [14]. A silicon delta doping layer (n-type) in the buffer just below the channel is incorporated during epitaxial growth to enhance the channel electron density. 2.5 nm HfO_2 (effective oxide thickness of $\sim$ 0.5 nm) is deposited by atomic layer deposition on top of the channel. The device is mesa isolated instead of using oxide isolation, which means that there should not be a leakage current increase caused by hole trapping in the field oxide. The vertical energy band alignment through the gate at $V_G = V_D = V_S = 0$ V is described in Fig. 1(b). The channel, the buffer, and the gate dielectric form a type-I heterostructure. Fig. 1(c) shows the measured capacitance from 300 kHz to 5 MHz. The capacitance equivalent thickness (CET) in these devices is approximately 1.7 nm. The dispersion in the capacitance-voltage characteristics in the sub-threshold region is due to interface traps [15].

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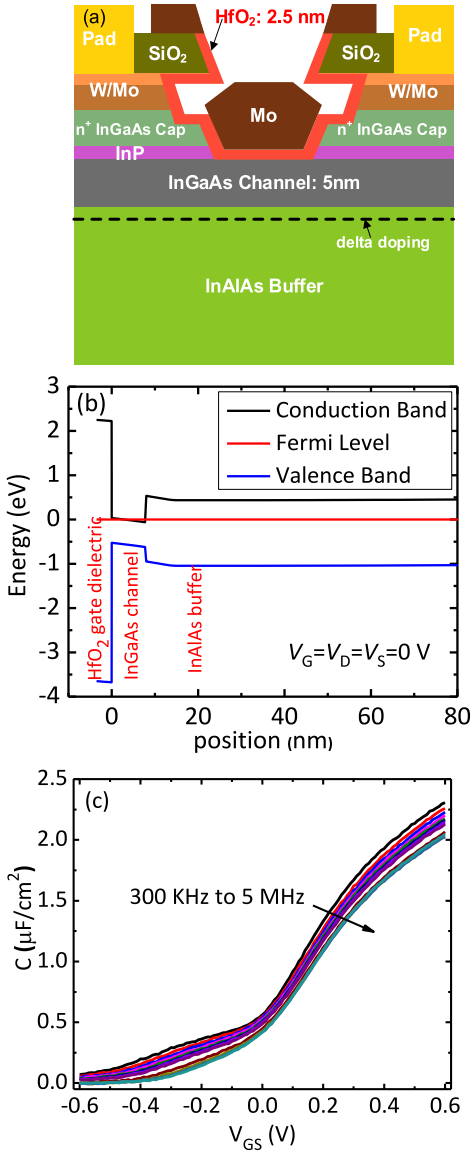

Fig. 1. (a) Schematic cross section of the device under test (not drawn to scale); (b) band diagram along a vertical cut line through the gate; (c) measured capacitance as a function of frequency from 300 kHz to 5 MHz. The arrow indicates the direction of increasing frequency. The tested device has a dimension of $W/L = 10\ \mu\text{m}/2\ \mu\text{m}$.

The irradiation is performed in a 10-keV ARACOR X-ray source at a dose rate of 31.5 krad(SiO_2)/min at room temperature. Irradiations and stresses were performed with gate voltages (V_{GS}) of +1.0 V or −1.0 V, with all the other terminals grounded. All the tested devices have an initial threshold voltage of approximately 0.1 V. There is a relatively high density of pre-existing traps in the gate oxide of these devices, which cause charge trapping due to electrical stress. To account for this, the electrical stress-induced degradation without irradiation is also measured at biases and times comparable to those used in the irradiation experiments. Current-voltage (I-V) characteristics are measured using an Agilent 4156 parameter analyzer. Devices with three different channel lengths are studied. At least three devices of each channel length are tested for each bias condition with and without exposure to X-ray irradiation. After irradiation, the

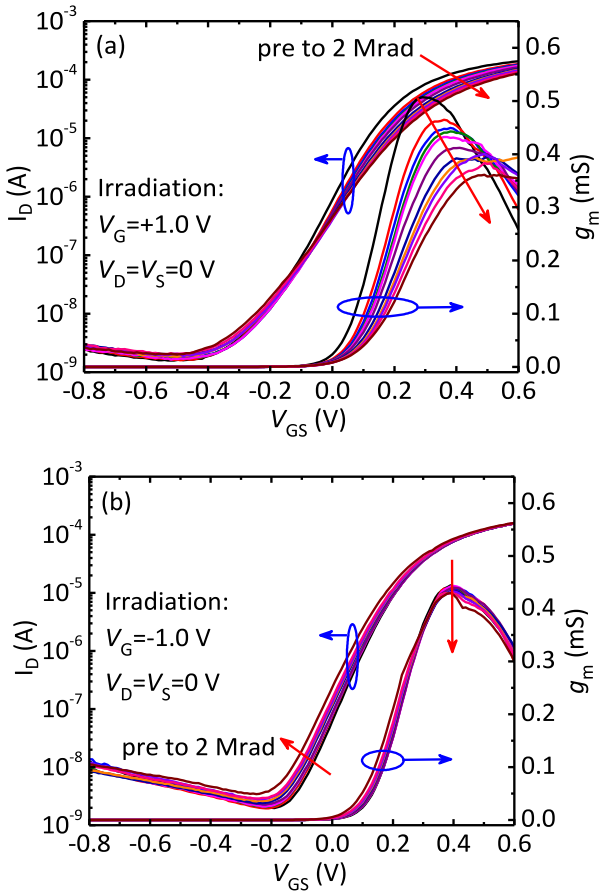

Fig. 2. I_D versus V_{GS} (left) and g_m versus V_{GS} (right) at different irradiation doses for a device with dimensions of $W/L = 10\ \mu\text{m}/2\ \mu\text{m}$ at (a) $V_{GS} = +1.0$ V and (b) $V_{GS} = -1.0$ V during irradiation. Measurements are made with $V_{DS} = 50$ mV. The red arrow indicates the direction of increasing dose. The initial interface trap density inferred from the subthreshold swing is $\sim 8 \times 10^{12}\ \text{cm}^{-2}\text{eV}^{-1}$.

devices are annealed with all terminals grounded at room temperature and I-V characteristics are re-measured after different annealing times.

III. Results and Discussion

Figs. 2 (a) and (b) show I_D (drain current) vs. V_{GS} and g_m (transconductance) vs. V_{GS} measured with $V_{DS} = 50$ mV as a function of dose for devices biased at $V_{GS} = +1.0$ V and $V_{GS} = -1.0$ V, respectively, during irradiation. The threshold voltage shifts positively for $V_{GS} = +1.0$ V, indicating net electron trapping during positive-bias irradiation. But for $V_{GS} = -1.0$ V, the threshold voltage shifts negatively, suggesting net hole trapping. For both conditions, the devices have an excellent ON/OFF ratio, above 10^4 after a total dose of 2 Mrad(SiO_2), indicating excellent gate control. Due to variations among devices, the leakage currents are at different levels for different devices. The leakage current mechanisms are illustrated in [16].

Fig. 3 shows the subthreshold swing (SS) and normalized peak transconductance, extracted from Fig. 2, as a function of total dose and anneal time for $V_{GS} = +1.0$ V and $V_{GS} = -1.0$ V irradiation bias. The average SS increases approximately 40 mV/decade at $V_{GS} = +1.0$ V, corresponding

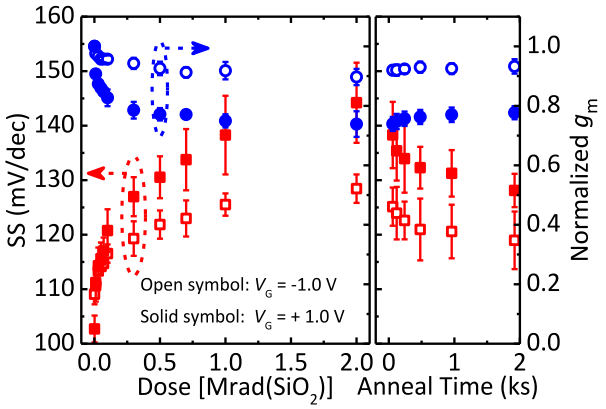

Fig. 3. Subthreshold swing (left) and normalized peak transconductance (right) as a function of irradiation dose and annealing time. The normalization is based on the pre-irradiation peak transconductance. The error bars represent standard deviations among different devices tested. Measurements are made with $V_{DS} = 50$ mV. All the tested devices have dimensions of $W/L = 10\ \mu$m/2 μm. The red squares correspond to subthreshold swing, and the blue circles represent the peak transconductance.

to the generation of 8.3×10^{12} cm^{-2}eV^{-1} interface traps, if interface traps distributed uniformly in energy are solely responsible for the change in SS [17]. The SS increase at $V_{GS} = -1.0$ V is half that of positive-bias irradiation. Similarly, peak-$g_{\rm m}$ degradation at $V_{GS} = -1.0$ V (10%) is less than half of $V_{GS} = +1.0$ V (30%). That the peak-g_m degradation correlates well with the increase in subthreshold swing increase suggests there are interface and/or near interface oxide (border) traps generated during irradiation [11], [12]. The partial recovery in SS and peak-g_m during annealing is likely related to electron/hole detrapping from border traps [18]. Some of the remaining degradation may be due to interface traps, but a significant percentage may also be due to border traps.

The degradation under the two bias conditions in Figs. 2 is quite different. At $V_{GS} = +1.0$ V, the ON current (at V_{GS} - $V_{TH} = 0.5$ V) decreases by 26% after 2 Mrad(SiO$_2$) exposure, and the subthreshold current increases 6% (at $V_{GS} = -0.2$ V). However, for $V_{GS} = -1.0$ V, the ON current decreases 4% and the subthreshold current increases by 2x. These differences occur because more radiation-induced interface traps are created in devices irradiated under positive bias in these HfO_2 dielectric devices than for ones irradiated under negative bias, as typically observed also for SiO_2 dielectrics [19]. The resulting charge scatters carriers efficiently [20]–[23].

To separate the pure TID response from the combined response, the bias-induced degradation was separately measured at biases and times comparable to those used during irradiation. Fig. 4 (a) and (b) show the threshold voltage shift as a function of equivalent dose for (1) TID irradiation, (2) bias only, and (3) the pure TID response, adjusted for charge trapping due to the simultaneous bias-stress at $V_{GS} = +1.0$ V and $V_{GS} = -1.0$ V, respectively. The adjustment is made by subtracting (2) bias only results from (1) TID irradiation results. For the bias-only condition at $V_{GS} = +1.0$ V, there is a positive threshold-voltage shift of about 200 mV, indicating an areal density of 2.5×10^{12} cm^{-2} trapped

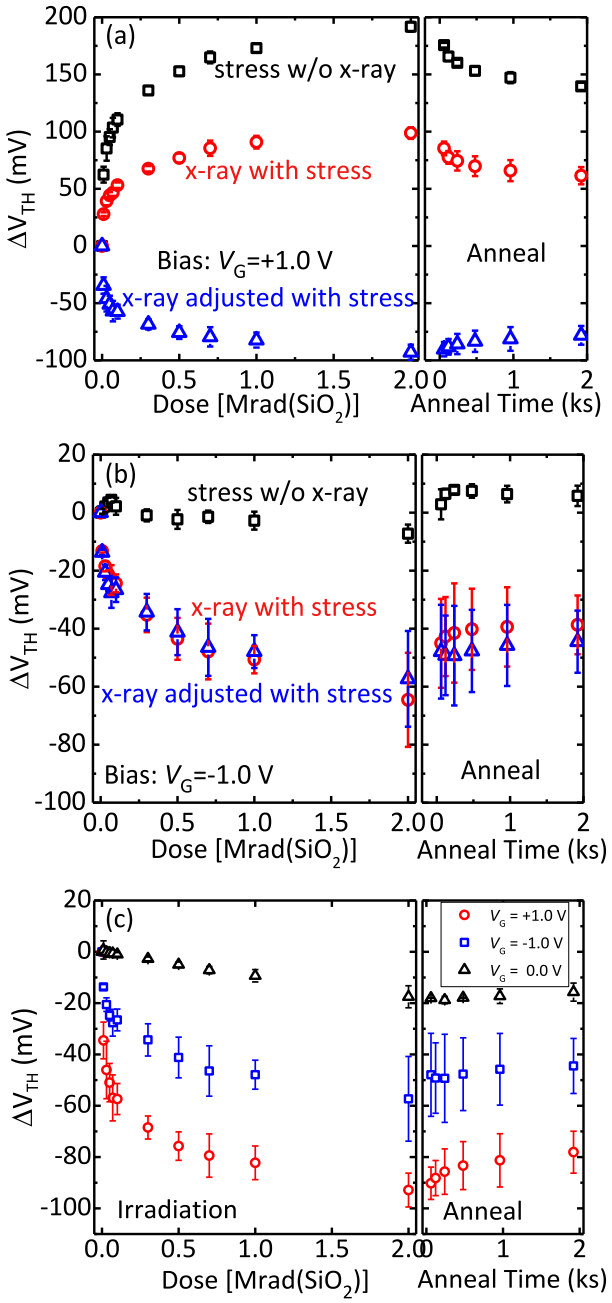

Fig. 4. Threshold voltage as a function of irradiation dose and annealing time for irradiation, bias only, and bias-stress-adjusted irradiation conditions for (a) $V_{GS} = +1.0$ V and (b) $V_{GS} = -1.0$ V during irradiation; (c) threshold voltage shift as a function of dose and annealing time for bias-stress-adjusted irradiation at two bias conditions. The adjusted curves reflect the biased X-ray response, after subtracting the stress-alone induced shifts. Results for 0 V irradiation are also shown in (c), and show smaller shifts. The error bars represent the standard deviations among different devices tested. Measurements are made with $V_{DS} = 50$ mV. All tested devices have dimensions of $W/L = 10\ \mu$m/2 μm.

electrons when projected to the interface. These trapped charges cause Coulomb scattering to channel carriers and decrease the carrier mobility, as discussed above. However, for $V_{GS} = -1.0$ V, there is a negligible negative threshold voltage shift (less than -10 mV) due to bias only. This suggests that InGaAs MOSFETs are more sensitive to positive bias stress than negative bias stress.

After subtracting the bias-alone induced threshold-voltage shift from the biased-irradiation induced threshold-voltage shift in Fig. 4(a), there is a negative threshold voltage shift of about 100 mV at $V_{GS} = +1.0$ V, which corresponds to an areal density of 1.3×10^{12} cm^{-2} trapped holes when projected to the interface. That net electron trapping is observed shows that less TID-induced hole trapping occurs than bias-induced electron trapping under the selected irradiation and bias conditions, consistent with the response of some Si-gate devices with HfO_2 gate dielectrics [24]. Hence, the combined positive-bias response of the devices biased at $V_{GS} = +1.0$ V during irradiation is dominated by electron trapping due to the applied bias alone, i.e., positive-bias instability [11]. Similar analysis shows that the threshold voltage shift is approximately -60 mV for the $V_{GS} = -1.0$ V gate-bias irradiation in Fig. 4(b), corresponding to 7.5×10^{11} cm^{-2} hole trapping in the HfO_2. The threshold voltage shifts under both bias conditions are larger than silicon devices with similar gate dielectric [24]. This is related to the high density of interface defects between the high κ dielectric and InGaAs, such as Ga or As dangling bonds, as well as Ga-Ga or As-As like-atom bonds, which leads to enhanced hole and electron trapping [25].

Fig. 4(c) shows the pure TID-induced threshold-voltage shift at irradiation bias of $V_{GS} = +1.0$ V, $V_{GS} = -1.0$ V, and $V_{GS} = 0$ V. These results show that the threshold voltage shift due to irradiation, after correcting for bias-stress effects, is greater under positive gate bias during irradiation than negative gate bias. This result is similar to what is observed in Si MOSFETs with HfO_2 gate oxides [26], and contrary to that in InGaAs gate-all-around MOSFETs [9]. Radiation-induced threshold voltage shifts under positive and negative bias are larger than under zero bias. This is due to the smaller electric field in the gate oxide under zero bias, which leads to smaller hole yield [19].

TCAD simulations show that the electric fields in the HfO_2 at $V_{GS} = +1.0$ V and $V_{GS} = -1.0$ V are approximately 0.8 MV/cm and -0.8 MV/cm, respectively. Hence, the charge yield in both bias conditions should be approximately equal, which suggests that the charge yield cannot explain this bias dependence. One plausible explanation for the difference in threshold voltage shift under the two bias conditions is that the trapped hole centroid at $V_{GS} = +1.0$ V is closer to the HfO_2/InGaAs interface than at $V_{GS} = -1.0$ V, due to the electric field polarity difference between the two bias conditions, as illustrated in Fig. 5. The closer to the interface the charge centroid, the charge would cause larger threshold voltage shift. This bias dependence is similar to what is typically observed for charge trapping in SiO_2, when trapped-oxide charge densities are similarly high [19].

Fig. 6 (a) shows the transfer characteristics before irradiation and after 2 Mrad(SiO_2) exposure for devices with different gate lengths. The device is biased with $V_{GS} = +1.0$ V during irradiation. Devices with different gate lengths have similar irradiation response, namely positive threshold-voltage shift, negligible leakage-current increase, and ON-current degradation. After 2 Mrad(SiO_2) exposure, the devices still have ON/OFF ratios over 10^5, even for

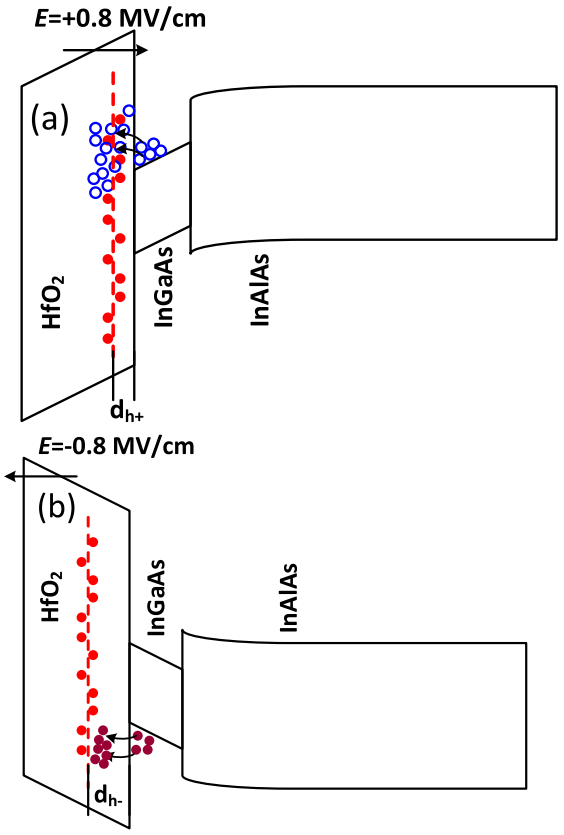

Fig. 5. Schematic illustration of charge trapping during biased irradiation at (a) $V_{GS} = +1.0$ V and (b) $V_{GS} = -1.0$ V. The blue open circle represents electrical stress-induced electron trapping; the red solid circle represents radiation induced hole trapping; and the dark solid red circle represents electrical stress-induced hole trapping. The red dashed line in the figure represents the trapped-hole centroid. The labels d_{h+} and d_{h-} represents the distance between the trapped-hole centroid and the HfO_2/InGaAs interface at $V_{GS} = +1.0$ V and $V_{GS} = -1.0$ V, respectively. $d_{h-} > d_{h+}$.

the devices with $L_G = 80$ nm. The bias-stress-adjusted TID response as a function of dose and annealing time for different gate lengths are shown in Fig. 6(b) and (c) under irradiation bias of $V_{GS} = +1.0$ V and $V_{GS} = -1.0$ V, respectively. The results indicate that larger threshold-voltage shifts are observed for devices with longer channels, for both positive and negative gate bias during irradiation. This suggests there is more hole trapping for the longer devices than the shorter devices. No significant effects of channel length are observed for the bias-induced shifts.

A typical cause of length and width variation in TID response is electric field variation in the gate dielectric as a function of channel length, which can strongly influence the amount of hole trapping [27], [28]. However, TCAD simulations show that the electric field in the HfO_2 differs by less than 1% among all these devices and gate lengths. Therefore, electric field variations cannot explain the large TID-induced threshold voltage shift difference at different gate lengths.

Another possibility is that the mechanical strain in the gate oxide may vary with gate length, which in turn can impact the hole trapping in the oxide significantly. This has been evaluated for SiO_2/Si devices [29]–[32], but not for devices

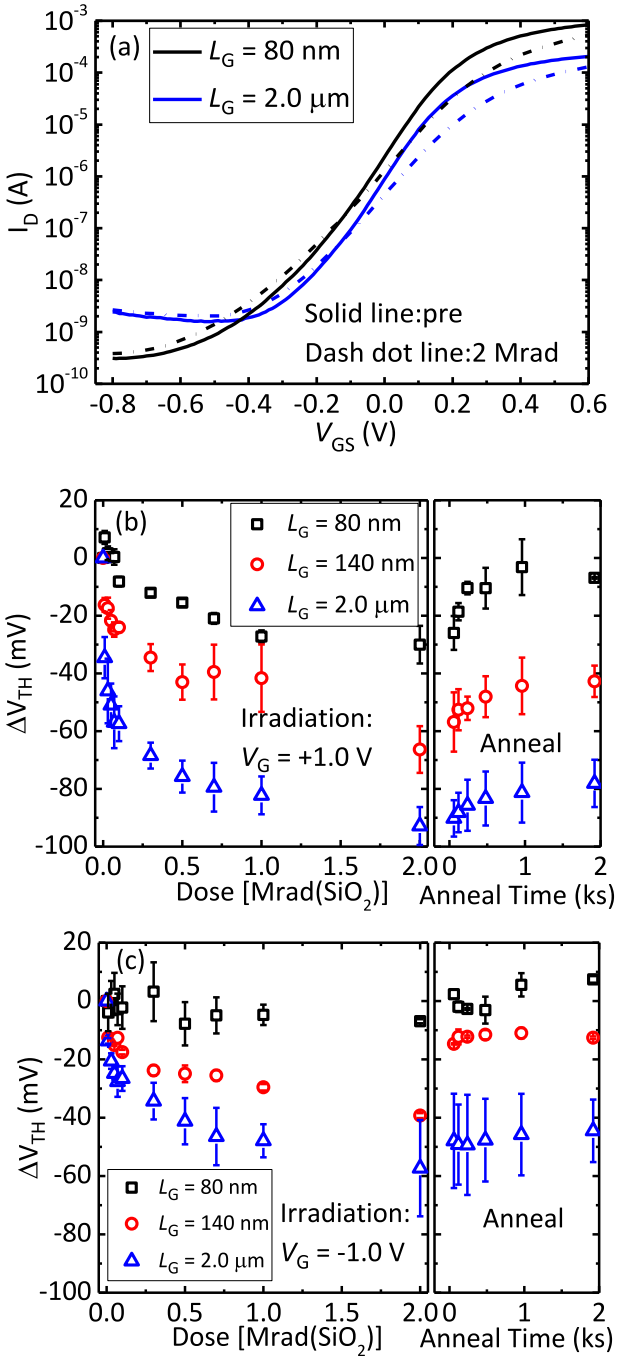

Fig. 6. (a) I_D versus V_{GS} before and after 2 Mrad(SiO_2) irradiation for devices with different gate lengths. During irradiation, $V_{GS} = +1.0$ V. The bias-stress-adjusted TID-induced threshold voltage shift is shown as a function of dose and anneal time for different gate lengths for bias at (b) $V_{GS} = +1.0$ V, and (c) $V_{GS} = -1.0$ V. The error bars represent standard deviations among different devices tested. Measurements are made with $V_{DS} = 50$ mV.

with high-K gate stacks. In previous work, it has been shown that radiation-induced hole trapping tends to decrease if the interfacial Si tensile stress decreases. As a result, the radiation-induced hole trapping is larger for narrow width [27], [29] and thick gate metal devices [30], due to more compressive stress. This is consistent with the trends we observe, but more work is required to evaluate the effects of stress on charge trapping in devices with high-κ gate stacks.

IV. Conclusions

The gate bias and geometry dependence of TID effects on InGaAs quantum-well MOSFETs with thin HfO_2 gate oxide have been evaluated. Positive gate bias during irradiation leads primarily to bias-stress-induced electron trapping that exceeds radiation-induced hole trapping, leading to a net positive threshold-voltage shift under the conditions of this study. Negative gate bias during irradiation results in additive hole trapping from irradiation and bias-stress. The shift produced by the irradiation alone is negative and larger with positive gate bias than that observed under negative gate bias. In addition, the bias-stress-adjusted radiation-induced hole trapping increases with the channel length for both positive and negative bias irradiation. These results provide early insight into the mechanisms and magnitude of the combined bias-stress and TID responses of InGaAs quantum-well MOSFETs with thin HfO_2 gate oxides. Improvements to oxide/semiconductor interface quality are required before these devices are suitable for insertion into commercial-grade CMOS technologies.

References

[1] J. A. del Alamo, "Nanometre-scale electronics with III–V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, Nov. 2011.

[2] M. Radosavljevic *et al.*, "Electrostatics improvement in 3-D tri-gate over ultra-thin body planar InGaAs quantum well field effect transistors with high-K gate dielectric and scaled gate-to-drain/gate-to-source separation," in *Proc. IEEE Int. Electron Device Meeting (IEDM)*, Dec. 2011, pp. 765–768.

[3] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Impact of intrinsic channel scaling on InGaAs quantum-well MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3470–3476, Nov. 2015.

[4] R.-H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: From bulk to SOI to bulk," *IEEE Trans. Electron Devices*, vol. 39, no. 7, pp. 1704–1710, Jul. 1992.

[5] M. Rodwell *et al.*, "III–V FET channel designs for high current densities and thin inversion layers," in *Proc. DRC*, Jun. 2010, pp. 149–152.

[6] K. Ni *et al.*, "Single-event transient response of InGaAs MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3550–3556, Dec. 2014.

[7] K. Ni *et al.*, "Charge collection mechanisms in GaAs MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 2752–2759, Dec. 2015.

[8] X. Sun *et al.*, "Total ionizing dose radiation effects in Al_2O_3-gated ultra-thin body $In_{0.7}Ga_{0.3}As$ MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 1, pp. 402–407, Feb. 2013.

[9] S. Ren *et al.*, "Total ionizing dose effects in extremely scaled ultra-thin channel nanowire gate-all-around InGaAs MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 2888–2893, Dec. 2015.

[10] X. Sun *et al.*, "Total-ionizing-dose radiation effects in AlGaN/GaN HEMTs and MOS-HEMTs," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4074–4079, Dec. 2013.

[11] S. Deora *et al.*, "Positive bias instability and recovery in InGaAs channel nMOSFETs," *IEEE Trans. Device Mater. Reliab.*, vol. 13, no. 4, pp. 507–514, Dec. 2013.

[12] M.-F. Li, G. Jiao, Y. Hu, Y. Xuan, D. Huang, and P. D. Ye, "Reliability of high-mobility InGaAs channel n-MOSFETs under BTI stress," *IEEE Trans. Device Mater. Reliab.*, vol. 13, no. 4, pp. 515–523, Dec. 2013.

[13] Z. Ji *et al.*, "An investigation on border traps in III–V MOSFETs with an $In_{0.53}Ga_{0.47}As$ channel," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3633–3639, Nov. 2015.

[14] J. Lin, Z. Xin, Y. Tao, D. A. Antoniadis, and J. A. del Alamo, "A new self-aligned quantum-well MOSFET architecture fabricated by a scalable tight-pitch process," in *Proc. IEEE Int. Electron Device Meeting (IEDM)*, Dec. 2013, pp. 421–424.

[15] K. Martens *et al.*, "On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 547–556, Feb. 2008.

[16] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Physics and mitigation of excess OFF-state current in InGaAs quantum-well MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1448–1455, May 2015.

[17] J. R. Schwank, P. S. Winokur, P. J. McWhorter, F. W. Sexton, P. V. Dressendorfer, and D. C. Turpin, "Physical mechanisms contributing to device 'rebound,"' *IEEE Trans. Nucl. Sci.*, vol. NS-31, pp. 1434–1438, Dec. 1984.

[18] D. M. Fleetwood, "Fast and slow border traps in MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 3, pp. 779–786, Jun. 1996.

[19] D. M. Fleetwood, "Total ionizing dose effects in MOS and low-dose-rate sensitive linear-bipolar devices," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1706–1730, Jun. 2013.

[20] P. Nagaiah *et al.*, "Mobility and remote scattering in buried InGaAs quantum well channels with high κ gate oxide," *J. Vac. Sci. Technol. B*, vol. 28, pp. C3H5–C3H9, May 2010.

[21] A. M. Sonnet *et al.*, "Remote phonon and surface roughness limited universal electron mobility of $In_{0.53}Ga_{0.47}As$ surface channel MOSFETs," *Microelectron. Eng.*, vol. 88, pp. 1083–1086, 2011.

[22] F. Lime *et al.*, "Carrier mobility in advanced CMOS devices with metal gate and HfO_2 gate dielectric," *Solid-State Electron.*, vol. 47, no. 10, pp. 1617–1621, Oct. 2003.

[23] M. A. Negara *et al.*, "Analysis of electron mobility in HfO_2/TiN gate metal-oxide-semiconductor field effect transistors: The influence of HfO_2 thickness, temperature, and oxide charge," *J. Appl. Phys.*, vol. 105, no. 2, p. 024510, 2009.

[24] S. K. Dixit *et al.*, "Radiation induced charge trapping in ultrathin HfO_2-based MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 1883–1890, Dec. 2007.

[25] J. Robertson, Y. Guo, and L. Lin, "Defect state passivation at III–V oxide interfaces for complementary metal-oxide-semiconductor devices," *J. Appl. Phys.*, vol. 117, no. 11, p. 112806, Mar. 2015.

[26] X. J. Zhou, D. M. Fleetwood, J. A. Felix, E. P. Gusev, and C. D'Emic, "Bias-temperature instabilities and radiation effects in MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2231–2238, Dec. 2005.

[27] F. Faccio and G. Cervelli, "Radiation-induced edge effects in deep submicron CMOS transistors," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2413–2420, Dec. 2005.

[28] F. El-Mamouni *et al.*, "Fin-width dependence of ioniz-ing radiation-induced subthreshold-swing degradation in 100-nm gate-length finFETs," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3250–3255, Dec. 2009.

[29] M. R. Chin and T. P. Ma, "Gate-width dependence of radiation-induced interface traps in metal/SiO_2/Si devices," *Appl. Phys. Lett.*, vol. 42, no. 10, pp. 883–885, 1983.

[30] V. Zekeriya and T. P. Ma, "Dependence of radiation-induced interface traps on gate Al thickness in metal/SiO_2/Si structures," *J. Appl. Phys.*, vol. 56, no. 4, pp. 1017–1020, 1984.

[31] V. Zekeriya and T. P. Ma, "Dependence of X-ray generation of interface traps on gate metal induced interfacial stress in MOS structures," *IEEE Trans. Nucl. Sci.*, vol. NS-31, no. 6, pp. 1261–1266, Dec. 1984.

[32] K. Kasama, F. Toyokawa, M. Tsukiji, M. Sakamoto, and K. Kobayashi, "Mechanical stress dependence of radiation effects in MOS structures," *IEEE Trans. Nucl. Sci.*, vol. NS-33, no. 6, pp. 1210–1215, Dec. 1986.