OFF-state TDDB in High-Voltage GaN MIS-HEMTs

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***Abstract*—We have investigated time-dependent dielectric breakdown (TDDB) in high-voltage AlGaN/GaN Metal-Insulator-Semiconductor High Electron Mobility Transistors (MIS-HEMTs) biased in the OFF state. This is an important reliability concern that has been overlooked. Towards this goal, we have developed a novel methodology using ultraviolet light that allows us to separate the permanent effects of dielectric degradation from the transient behavior due to trapping after high voltage stress. This new approach reveals unmistakable evidence of TDDB at the drain end of the gate in the OFF state. This mechanism must be accounted for in device lifetime estimation models. Furthermore, trapping emerges as a significant complication in the study of OFF-state TDDB. If uncontrolled, trapping effects can lead to a dramatic overestimation of device breakdown voltage.**

***Index Terms*—dielectric reliability, GaN, MIS-HEMT, OFF-state, TDDB**

I. Introduction

As demand for more energy-efficient electronics increases, GaN has emerged as a promising transistor material candidate for high-voltage power management applications. The AlGaN/GaN Metal-Insulator-Semiconductor High Electron Mobility Transistor (MIS-HEMT) constitutes the most suitable device structure for this application as it offers lower gate leakage than its HEMT counterpart. GaN has excellent material properties, but there are still many challenges to overcome before widespread commercial deployment [1]–[4]. Time-dependent dielectric breakdown (TDDB), a catastrophic condition arising after prolonged high-voltage gate stress [5], is a particularly important concern. Thus far, studies under positive gate bias stress have shown TDDB behavior similar to that of silicon CMOS systems [6]–[8].

In this work, we explore TDDB under OFF-state conditions: a negative gate bias is used to turn off the channel and a high positive bias is applied to the drain. This is the most common state of a power switching transistor in a power management circuit. In the OFF state, there is a high electric field across the gate dielectric at the gate edge on the drain side. Prolonged stress inevitably results in defect formation inside the gate dielectric and eventual dielectric breakdown. It is uncommon to think of TDDB under OFF-state conditions. Though there is limited work on this for GaN HEMTs [9], [10] this reliability concern in MIS-HEMTs has thus far been overlooked.

Here we show evidence of GaN MIS-HEMT failure after prolonged OFF-state stress through a TDDB mechanism. In order to study this, we present a new methodology based on UV light that separates pervasive trapping-related transient effects, such as current collapse and threshold voltage (V_T) shift, from permanent dielectric degradation, indicative of TDDB. We show that trapping effects during stress cause significant overestimation of device breakdown voltage under OFF-state stress conditions.

II. Breakdown Statistics and Initial Results

The devices studied in this work are industrially prototyped depletion-mode AlGaN/GaN MIS-HEMTs fabricated on 6-inch Si wafers. In an earlier study, we found that prolonged positive gate stress in these devices yields a breakdown behavior consistent with TDDB [7]. We also found evidence of progressive breakdown (PBD) prior to final hard breakdown [8] and further explored the temperature dependence of both [11]. In order to study TDDB in the OFF state, we focus on devices without field plates in which, under high-bias OFF-state conditions, a large electric field appears at the edge of the gate on the drain side. In actual high-voltage MIS-HEMTs, the electric field at this location can be mitigated by the use of field plates [12]. However, the electric field there remains relatively high and eventual dielectric failure is to be expected.

Fig. 1 shows the stress leakage evolution of a constant-voltage stress test in the OFF-state with $V_{DS,stress}$=118 V and $V_{GS,stress}=V_{T0}$-5 V (V_{T0} is the threshold voltage defined at I_D=1 μA on the virgin device). We observe multiple jumps in the gate current I_G (equal to the drain current I_D) before final hard breakdown occurs near 10^5 s. The source current is unaffected. The jumps in I_G=I_D (except for the last one) are reminiscent of soft dielectric breakdown in silicon MOSFETs [13] and also resemble dielectric breakdown after positive gate stress in these same devices [8]. "Hard breakdown" can occur either after a number of soft breakdown events, or for harsher stress conditions it can be the first breakdown event [14].

The inset of Fig. 1 shows time-to-breakdown distribution for a set of 14 devices. Hard breakdown is defined at the point when the device is no longer operational, which occurs when any of the terminal currents hits a compliance of 1 mA. In the figure, *F* is the cumulative failure of devices after a given stress time. The breakdown statistics do not follow a simple Weibull distribution, and the times-to-breakdown span many

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orders of magnitude. From these data, the physics of failure are unclear.

For greater understanding, we have performed stress experiments with periodic interruptions to enable a study of the evolution of device characteristics. This is sketched in the inset of Fig. 2. The rest of Fig. 2 shows the I_G current evolution for a constant-voltage stress experiment with $V_{DS,stress}$=94 V and $V_{GS,stress}$=V_{T0}-5 V. Here, the OFF-state stress is paused every 50 s and the device characteristics in the linear regime are measured, as shown in Fig. 3. The measured characteristics reveal an increase in OFF-state leakage that corresponds to the two large jumps in I_G observed in Fig. 2. There is also significant current collapse right after the application of stress.

To gain greater insight on the early stages of degradation, we have carried out OFF-state step-stress experiments (inset in Fig. 4). Each stress step lasted 100 s and I-V characterization was performed between steps. Fig. 4 shows the bias current evolution during stress. For low stress voltage, all the terminal currents remain below the noise floor of our system. For moderate stress, I_D=I_G exhibits a distinct shape: during stress the currents decrease as a result of trapping. Beyond $V_{DS,stress}$=90 V, there is evidence of *stress-induced leakage current* (SILC) [15] followed by a sudden and large jump and then a high-current plateau. Soon after, the device hits hard breakdown at 110 V. Throughout the entire experiment, I_G=I_D which suggests that the degradation is happening at the drain-side edge of the gate.

Fig. 5 shows the evolution of I-V subthreshold characteristics in the linear regime in between stress steps. Here, even for low values of $V_{DS,stress}$ we see large V_T shifts (first positive, then negative), a hysteretical behavior in the I-V sweeps and a progressive increase in current collapse. The hysteresis is indicated in Fig. 5 with red arrows where the I-V characteristics are first swept up, and then swept down. The high level of OFF-state leakage in the final I-V sweep in this graph corresponds to the plateau of high current in Fig. 4 as dielectric breakdown approaches.

It is well-known that high OFF-state bias causes an electric field peak at the gate corner on the drain side leading to severe trapping effects around this location [2]. We see evidence for

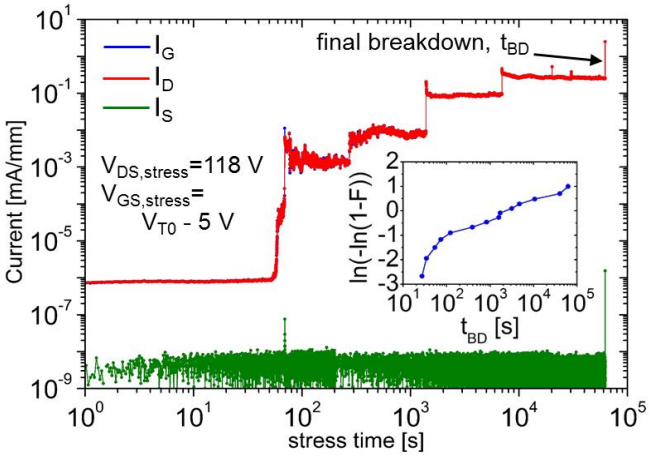

Fig. 1. Stress leakage evolution during a constant-voltage OFF-state stress experiment in the dark. Inset: Weibull plot of time-to-breakdown t_{BD} for OFF-state stress experiment. $V_{DS,stress}$=118 V. $V_{GS,stress}$=V_{T0}-5 V. F is defined as cumulative failure of devices at a given stress time.

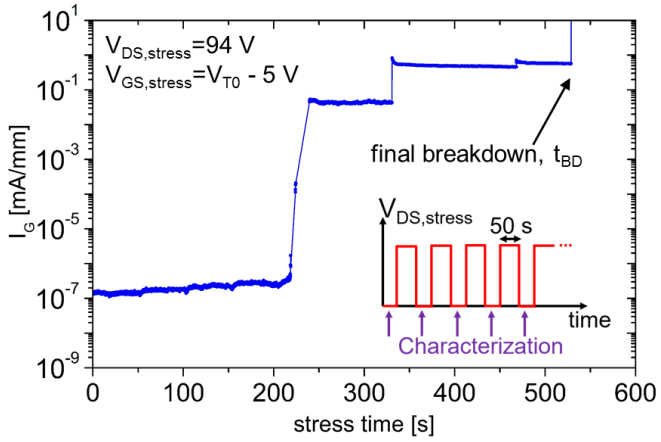

Fig. 2. Gate leakage evolution during a constant-voltage OFF-state stress experiment sketched in the inset. $V_{DS,stress}$=94 V. $V_{GS,stress}$=V_{T0}-5 V. Stress stopped and device characterized every 50 s.

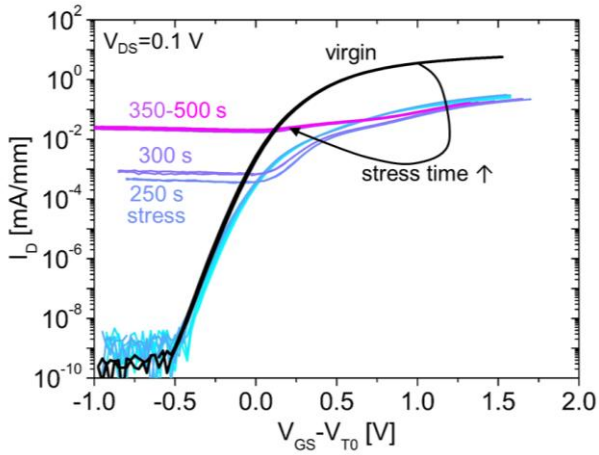

Fig. 3. Subthreshold I-V characteristics for the stress experiment in Fig. 2. V_{DS}=0.1 V. V_{GS} is normalized to the V_T of the virgin sweep, V_{T0}, defined at I_D=1 μA.

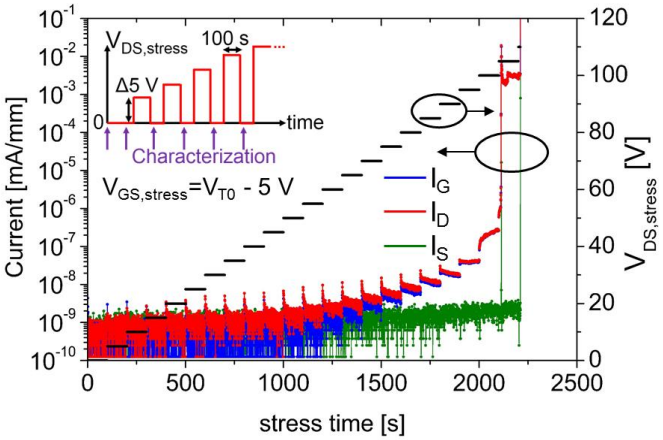

Fig. 4. Stress leakage evolution during an OFF-state step-stress experiment sketched in the inset. $V_{DS,stress}$ is increased in 5 V steps (right axis) until breakdown occurs. $V_{GS,stress}$=V_{T0}-5 V.

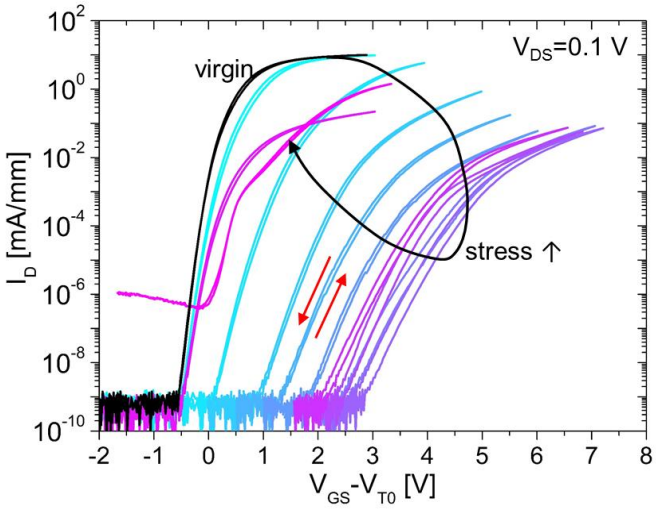

Fig. 5. Evolution of subthreshold I-V characteristics for the step-stress experiment in Fig. 4. V_{DS}=0.1 V. Hysteresis is visible and marked by red arrows where I-V characteristics are first swept up and then swept down.

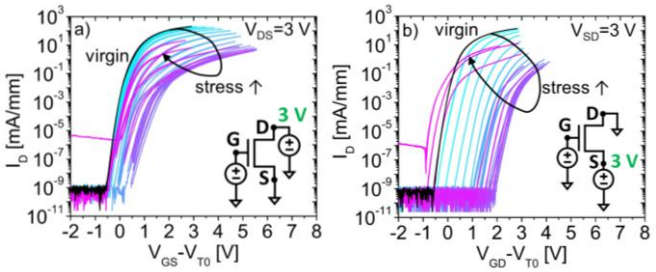

Fig. 6. a) Evolution of subthreshold characteristics in saturation with V_{DS}=3 V for the TDDB experiment of Fig. 4. b) Subthreshold characteristics with the role of source and drain swapped. V_{SD}=3 V.

this in Fig. 6 where the subthreshold I-V characteristics of the same device from Figs. 4 and 5 are measured under saturated conditions in the forward (Fig. 6a) and reverse (Fig. 6b) configurations (swapping source and drain). In saturation, V_T is set at the electron injection point (the source in the conventional configuration). Under regular conditions (Fig. 6a), V_T is relatively less affected by OFF-state stress. Under reverse conditions (Fig. 6b), V_T shows a similar behavior as in Fig. 5. This confirms that the prominent trapping that leads to V_T shifts and an increase in dispersion takes place at the drain end of the channel.

For additional insight, we have also performed C-V characterization between stress steps (Fig. 7). We see largely unchanged C-V characteristics during and after a typical step-stress experiment that reached breakdown. This suggests that most of the channel, towards the source side, is largely unaffected by the stress. To confirm this, in a separate device, we applied moderate $V_{DS,stress}$=40 V for 100 s and then measured first C-V and then I-V characteristics in quick succession. As shown in Fig. 8, there is minimum V_T shift of the C-V characteristics but an almost 1 V shift on the linear I-V characteristics. This is again consistent with trapping that is highly localized at one point in the channel.

All these experiments strongly suggest that under high OFF-state bias, TDDB takes place under the drain-side edge

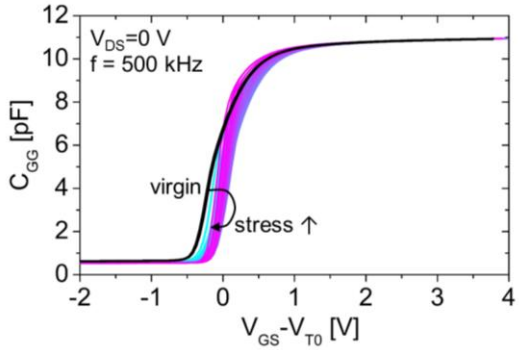

Fig. 7. Evolution of C-V characteristics at 500 kHz in between stress steps for an OFF-state step-stress experiment like that of Fig. 4. V_T shift comparable to Fig. 6a is observed. V_{DS}=0 V.

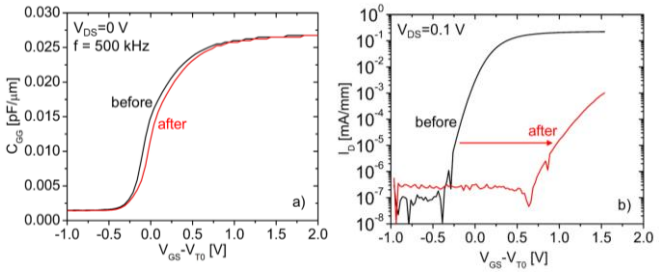

Fig. 8. a) C-V and b) I-V characteristics before and after stress measured in succession on the same device using bias tees. $V_{DS,stress}$=40 V for 100 s to induce current collapse and V_T shift. C-V is measured at 500 kHz with V_{DS}=0 V. I-V characteristics measured at V_{DS}=0.1 V.

of the gate. However, at that location, there is also severe trapping that masks the process. In order to tease out TDDB from the prominent trapping that is observed, we have devised a new methodology that is described next.

III. UV Light During Device Recovery and Stress

UV light has previously been shown to be effective in recovering current collapse effects in GaN MIS-HEMTs after OFF-state stress [2]. In our work, we first use UV light to separate transient effects from permanent degradation *after* OFF-state stress. A typical sequence is shown in Fig. 9. After each stress step, the device is grounded and illuminated with 3.5 eV UV light for 5 minutes and then characterized in the dark through I-V sweeps. This photon energy was chosen based on [2]. Fig. 10 shows subthreshold I-V characteristics during a typical experiment. The positive V_T shift has disappeared and current collapse is greatly mitigated. In fact, there is a negative V_T shift characteristic of NBTI [16], [17]. This shows the effectiveness of UV light in eliminating stress-induced trapping in the GaN and AlGaN layers. The subthreshold swing S in the inset of Fig. 10 shows no change throughout the experiment, indicating no interface states have been generated.

The linear I-V characteristics as well as the transconductance g_m and the V_T shift evolution are graphed in Fig. 11. There appears to be a two-stage behavior: first, g_m drops while V_T remains fairly stable, perhaps indicating residual current collapse, as seen in Fig. 11a. Subsequently V_T shifts negative and g_m increases slightly. This is characteristic of NBTI phenomenon due to oxide de-trapping [16], [17].

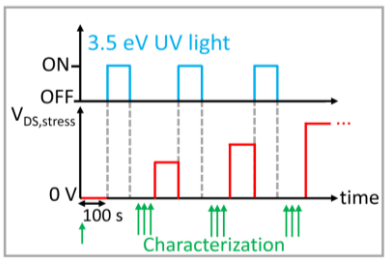

Fig. 9. Sketch of step-stress experiment with UV after stress. UV light is shone at 3.5 eV for 5 minutes after each stress step.

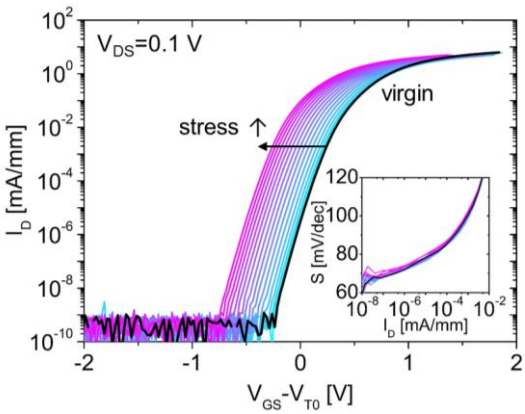

Fig.10. Subthreshold I-V characteristics for a step-stress experiment of Fig. 9. The V_T shift is only negative and there is little current collapse. V_{DS}=0.1 V.

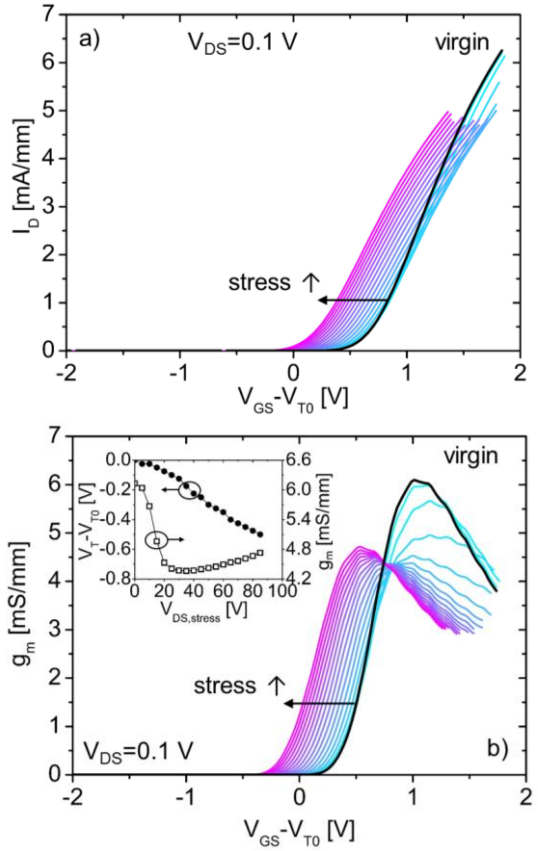

Fig.11 a) Linear I-V characteristics and b) gm characteristics for the step-stress experiment of Fig. 9. Peak g_m and V_T as a function of $V_{DS,stress}$ is shown in the inset. Except for an initial transient due to residual current collapse, g_m and V_T follow NBTI behavior.

We next use UV light to additionally mitigate trapping *during* electric stress (Fig. 12). The previous experiments show that UV is successful in recovering the effects of trapping after the stress is stopped. However, during stress, trapping still takes place and this is likely to affect the electric field across the gate dielectric that drives degradation. Trapping mitigation during stress is known to result in an increase in the electric field for the same applied bias [18]. This should accelerate dielectric degradation.

The evolution of the currents during stress in a typical experiment are shown in Fig. 13. The characteristic trapping signature, a reduction in I_G with time under constant voltage stress, has now disappeared. Instead, for moderate stress, we see leakage current increase during each stress period—a clear indication of SILC, well known to precede dielectric breakdown. In addition, hard breakdown occurs at a much lower voltage than in the dark ($V_{DS,stress}$=60 V in Fig. 13), just as expected [14].

These results strongly underline the impact trapping has in the field distribution in the OFF state. They also suggest that breakdown tests that ignore trapping have the potential to dramatically overestimate the device lifetime. This is confirmed in Fig. 14, showing the Weibull distribution for a set of devices stressed at constant voltage under UV, with the original distribution from the inset of Fig. 1 included for reference. Under UV, even with a 25% smaller $V_{DS,stress}$, the devices reach hard breakdown between 1 and 3 orders of magnitude faster than in the dark. We also see classic linear Weibull statistics with a much steeper slope of 1.2 compared

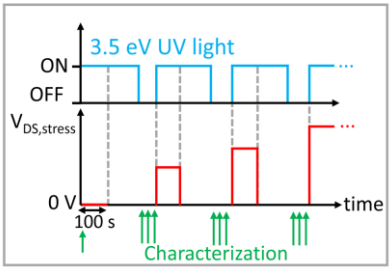

Fig. 12. Sketch of step-stress experiment with UV applied during and after stress. 3.5 eV UV light is shone during stress and for 5 minutes after each stress step.

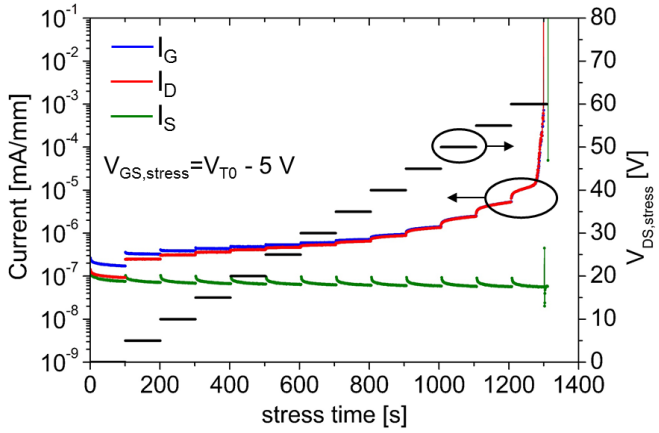

Fig. 13. Stress leakage evolution during an OFF-state step-stress experiment with UV light. $\Delta V_{DS,stress}$=5 V, $V_{GS,stress}$=V_{T0}-5 V.

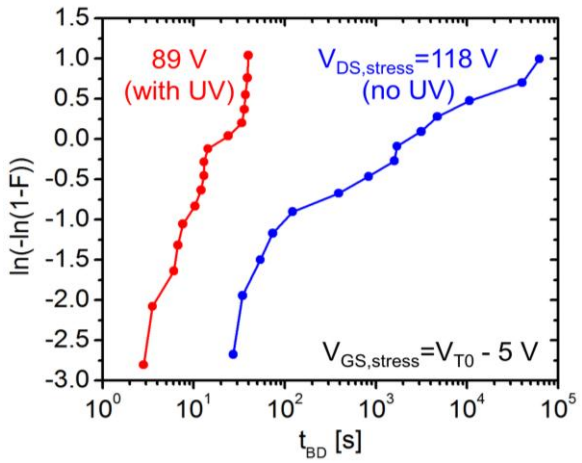

Fig. 14. Weibull plot of time-to-breakdown t_{BD} for OFF-state stress experiment with UV light, shown in red, and without UV light (from Fig. 1) shown in blue. $V_{DS,stress}$=89 V for UV data and 118 V for measurements in the dark. $V_{GS,stress}$= V_{T0}-5 V.

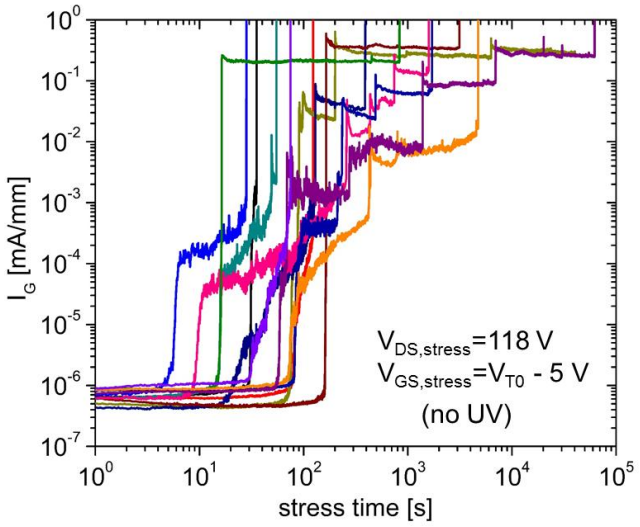

Fig. 15. Gate current I_G vs. stress time for the set of experiments in Fig. 14 in the dark. $V_{DS,stress}$=118 V, $V_{GS,stress}$=V_{T0}-5 V.

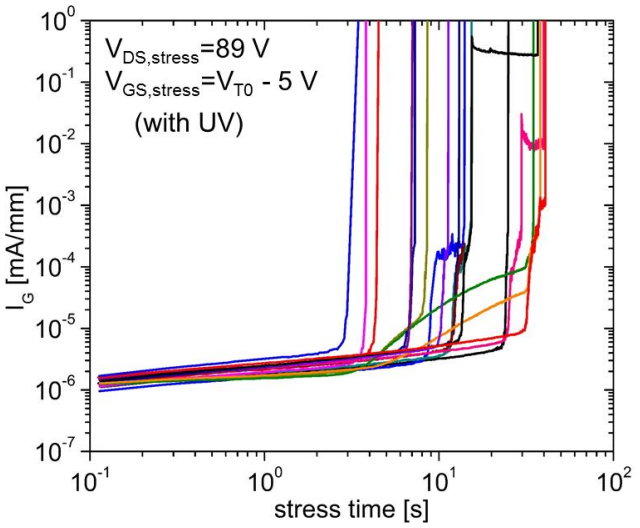

Fig. 16. Gate current I_G vs. stress time for the set of experiments in Fig. 14 under UV illumination. $V_{DS,stress}$=89 V, $V_{GS,stress}$=V_{T0}-5 V.

to 0.4 in the dark, suggesting that under UV exposure, we are now observing intrinsic TDDB behavior.

Figs. 15 and 16 show, respectively, the evolution of I_G for the TDDB experiments of Fig. 14 in the dark and under UV. In the dark (Fig. 15), multiple plateaus are observed before hard breakdown occurs. Under UV (Fig. 16), plateaus are more infrequent. This difference is another manifestation of the harsher stress conditions prevailing in the OFF state under UV. In Si devices, high stress voltage leads to "hard" breakdown characteristics (vs. "soft" breakdown at low voltage). To confirm this, Fig. 17 shows a TDDB experiment for lower $V_{DS,stress}$ under UV light where it is evident that a

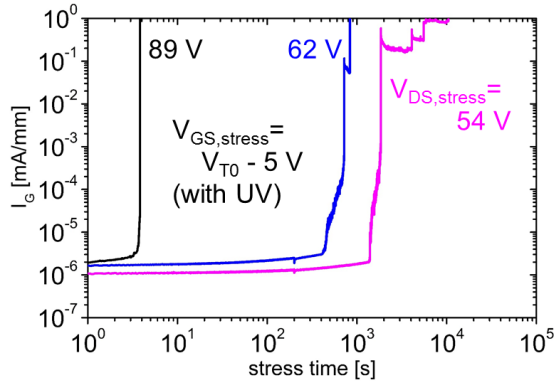

Fig. 17. Gate current I_G vs. stress time for a constant-voltage stress experiment with UV light at lower $V_{DS,stress}$ than in Fig. 16. One experiment from Fig. 16 shown for reference. $V_{GS,stress}$=V_{T0}-5 V.

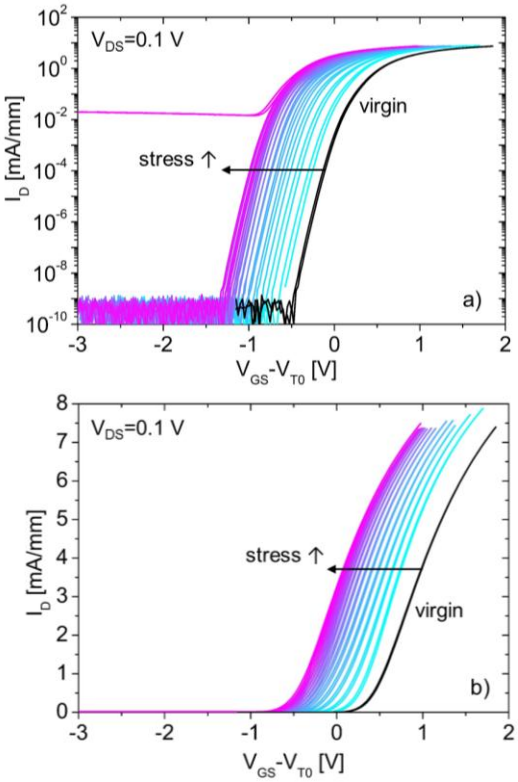

Fig. 18. Evolution of: a) subthreshold and b) linear I-V characteristics for a step-stress experiment of Fig. 13. Positive V_T shift has disappeared and there is substantially less current collapse. V_{DS}=0.1 V.

gentler stress condition results in multiple plateaus before final breakdown. A device stressed at $V_{DS,stress}$=89 V is shown for reference.

The evolution of device subthreshold I-V characteristics in the linear regime during a step-stress experiment with UV light are shown in Fig. 18. The results are largely similar to Fig. 10. This supports the notion that the addition of UV light during stress has not fundamentally changed the experiment but has merely prevented the trapping effects that reduce the electric field across the gate stack.

IV. Discussion

Our experiments constitute the first look at dielectric breakdown in GaN MIS-HEMTs under OFF-state stress conditions. We initially observe that in the dark, there is severe current collapse and prominent threshold voltage shifts that result from highly localized trapping at the drain-side edge of the gate corner.

In order to isolate the permanent degradation that results from TDDB, we must employ UV light. We establish first as a baseline the effect of UV light during a recovery stage and see that it completely mitigates current collapse and the positive V_T shift. In fact, the residual V_T shift that remains is characteristic of NBTI.

We can then additionally use UV light to eliminate trapping during stress. We find that this dramatically reduces the device breakdown voltage. This is because trapping effects cause a reduction of the applied electric field and this is mitigated through UV illumination. We can compare the I-V characteristics with those of the baseline experiment (where UV is only used during recovery) and find they are largely the same. This gives us confidence that the use of UV light during stress has not introduced new degradation behavior in the device.

In the future we will continue to use I-V as well as C-V measurements to further explore the physics of TDDB in GaN MIS-HEMTs. In order to develop accurate lifetime models, it is clear that much care must be taken to ensure that device lifetime does not become distorted by transient trapping-related degradation effects.

V. Conclusions

We have investigated OFF-state TDDB in GaN MIS-HEMTs and we have used UV light to disentangle trapping effects from permanent degradation due to dielectric breakdown. We find the impact of OFF-state stress largely localized to the drain-side edge of the gate. Without UV light, there is prominent current collapse and positive V_T shift. UV light almost completely eliminates current collapse and uncovers an underlying negative V_T shift characteristic of NBTI. In addition, with UV light during stress, the breakdown characteristics exhibit classic TDDB behavior with a breakdown voltage that is dramatically reduced. This highlights the importance of controlling for trapping effects when building models for lifetime prediction.

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