Nanoscale Mo Ohmic Contacts to III–V Fins

Alon Vardi, Wenjie Lu, Xin Zhao, and Jesús A. del Alamo, *Fellow, IEEE*

***Abstract*— A novel contact-first approach for III–V FinFETs and trigate MOSFETs is presented. In this process, the metal contact is sputtered on the as-grown semiconductor heterostructure, and the contact metal is used as a part of the fin dry-etch mask. We demonstrate this technique in Mo/n$^+$-InGaAs contact structures with fin widths in the range of 50 to 300 nm. We have measured contact resistance in the range of 5 to 20 $\Omega \cdot \mu$m. These results are in good agreement with the state-of-art contact resistance obtained on planar devices using similar technology. We further explore the possibility of enhancing the contacts by wrapping the metal over the fin sidewalls and found no significant improvement.**

***Index Terms*— Nano contacts, TLM, contact resistivity, III-V MOSFET, FinFETs.**

I. Introduction

III-V compound semiconductors are considered promising candidates to extend Moore's law beyond the limits of Si [1], [2]. III-V logic transistors are under investigation for designs with effective channel lengths smaller than 10 nm. In this regime, the transistors have to be of a three-dimensional nature with a fin or nanowire configuration [3]. In such devices, contact resistance is a great challenge. The contacts should have a length of about 10-15 nm while delivering a total source resistance of less than 50 $\Omega \cdot \mu$m [1], [4]. To meet this goal, the metal to semiconductor contact resistivity ρ_c needs to be lower than 0.5 $\Omega \cdot \mu$m^2. Low values of ρ_c for contacts on n$^+$-InGaAs between 0.4 and 3.2 $\Omega \cdot \mu$m^2 have been reported on planar contacts [5]–[9]. For such contact resistivity to be obtained, a high quality metal should be laid on a minimally processed semiconductor surface, ideally *in-situ* right after crystal growth [8], or *ex-situ* by thermal evaporation or sputtering very early in the process [9]. This represents a challenge for FinFET or Trigate MOSFETs in which a nanometer-scale fin needs to be defined. Addressing this important problem is the goal of this letter.

In this letter, we propose a new contact-first scheme to create refractory ohmic contacts to nm-scale etched III-V fins. In our approach, the metal contact serves as part of the mask that is used to define the fin etch. The proposed approach is demonstrated by fabricating Mo contacts on n$^+$-InGaAs heterostructures where we have extracted an average contact resistance of 8 $\Omega \cdot \mu$m.

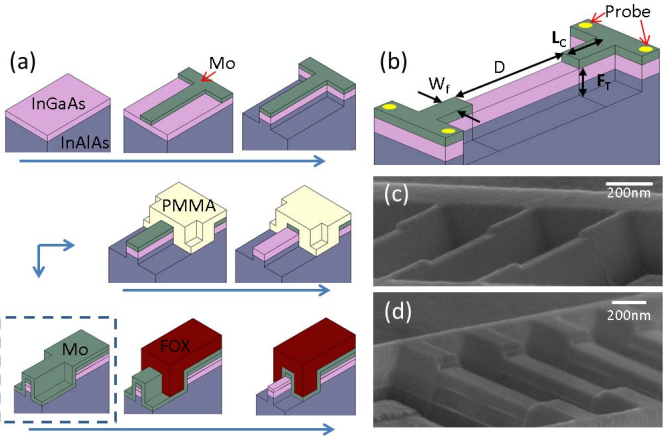

Fig. 1. (a) Schematic process flow of fin contacts with and without sidewall coverage. (b) Schematics of final test structure and device parameter definition. (c) and (d) SEM images of processed devices without and with a sidewall contact, respectively.

II. Fabrication Process

The sample used in these experiments consists of 20 nm $In_{0.53}Ga_{0.47}As$ n$^+$-doped to 10^{19} cm^{-3} on top of an undoped $InP/In_{0.53}Ga_{0.47}As$ (2/40 nm) heterostructure grown on $In_{0.52}Al_{0.48}As$ buffer layer on an InP substrate. Fig. 1 (a) shows a schematic of the process flow. It begins with sputtering of 30 nm of Mo followed by 2 nm of Al_2O_3 by ALD and 100 nm of spun-on hydrogen silsesquioxane (HSQ). Al_2O_3 is used to reduce the Mo undercut during the etch process and improve the HSQ adhesion. The thickness of the metal is selected so that the HSQ can survive the entire fin etching process while obtaining fins heights in the range $F_T \leq 250$ nm. The thickness of the Al_2O_3 is chosen so that it can be completely removed during the subsequent removal of HSQ in TMAH.

The fin pattern is then created by e-beam lithography. The Mo layer is etched using highly anisotropic reactive ion etching (RIE) based on a SF_6/O_2 plasma [9]. This is followed by fin-etch which is accomplished by a novel inductively coupled plasma (ICP) etching process utilizing $SiCl_4/BCl_3/Ar$ chemistry [10]. After fin etching, a window in a PMMA layer is patterned to reveal the fin and the Mo on top. Through this window, the Mo on the top surface is dry etched (using again SF_6/O_2 chemistry) to form a slit along the fin. Subsequent to PMMA removal, the process is finished by evaporating and lifting off Ti/Au (10/200 nm) pads.

Due to the high selectivity of SF_6 to III-V semiconductors, during Mo etch and once the Mo is completely removed,

Manuscript received November 23, 2014; accepted December 22, 2014. Date of publication December 25, 2014; date of current version January 23, 2015. This work was supported in part by the National Science Foundation (NSF) Award 0939514 (E3S STC), in part by the Donner Endowed Chair at MIT, and in part by an MIT-Technion Fellowship. The review of this letter was arranged by Editor M. Passlack.

The authors are with Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: alonva@mit.edu).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2014.2386311

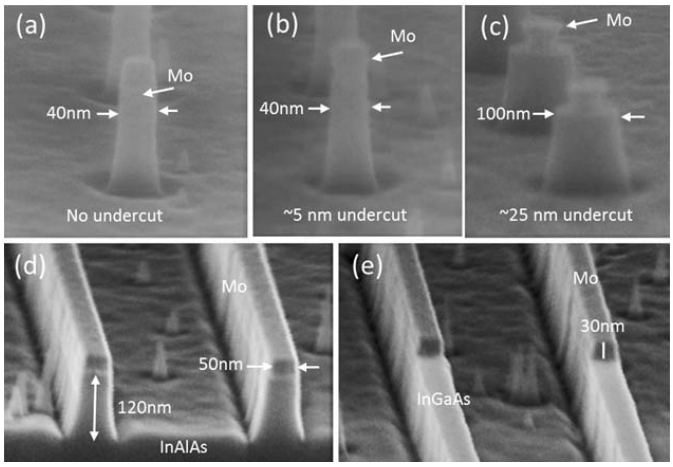

Fig. 2. Fin-etch process window using Mo/Al_2O_3 as mask: (a-c) metal etching time splits: 90, 100 and 120 sec, respectively. Same III-V etching conditions for 70 sec (d-e). Fin test structures (d) before and (e) after Mo slit opening.

the semiconductor/metal boundary under the mask is attacked sideways and an inverted undercut starts to form in the metal. This is shown in Fig. 2 (a-c), where different Mo etching times and a constant III-V etch time were used to pattern InGaAs posts. If on the other hand, the Mo is not fully removed, severe micro masking appears on the semiconductor surface during III-V etch due to the high selectivity of the $SiCl_4/BCl_3/Ar$ chemistry to Mo. With proper calibration of Mo etch time, the metal profile is vertical and the undercut is minimal, however, weak micro masking still appears during fin etch. For this letter, minimizing the undercut is of higher priority with the reduction of micro masking requiring further research. Figs. 2 (d) and (e) show 50 nm wide fins right after fin etch and after Mo slit opening, respectively, as obtained through an optimized process.

To obtain a wrapped-around contact (WAC), additional 30 nm of Mo is sputtered over the fin before slit patterning, as shown in Fig. 1 in the dashed rectangle. In this process flow, slit patterning is performed by e-beam exposed flowable oxide (FOX). Our sputtering system yields a ~1:2 Mo thickness ratio between the sidewalls and the top surface of the fin. Consequently, in the WAC process, there is a total of 60 nm of Mo on top of the fin and ~15 nm on the sidewalls. Therefore, the Mo slit opening requires twice the etching time (Fig. 1 (d)) as in the top-contact process. Since the thickness of the Mo on the sidewalls is only 1/4 of the total thickness on top of the fins, the etching time in SF_6 that is required to open the slit is enough to completely remove the Mo from the sidewalls and no additional isotropic etching step is required. This was confirmed by scanning electron microscope (SEM) inspection and through a separate experiment where the results using isotropic (CF_4/O_2) and anisotropic etch to pattern the slit were compared and found equivalent.

III. Results

The test structure used in this letter is a four-probe nano transmission line method (TLM), sketched in Fig. 1 (b), that is designed to measure the resistance of small contacts [11].

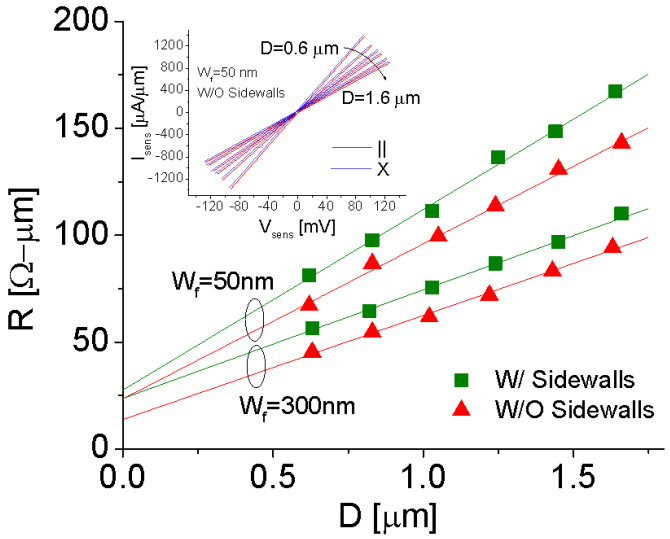

Fig. 3. TLM resistance vs. measured contact distance on structures with and without sidewall contacts for two different fin widths. Inset: typical TLM I-V characteristics in cross and parallel configurations.

The positions of the four probes are marked by yellow circles. To ensure that the measured resistance is associated with the fin contact (of length L_c in Fig. 1 (b)), we measured and averaged the four possible measurement configurations (two parallel and two diagonal). This is valid, as long as the access regions and the metal routing leading to the fins are wider than the transfer length estimated at <200 nm. In addition, the metal sheet resistance, R_{shm}, must be much smaller than that of the semiconductor, R_{sh}. In our case, $R_{shm} = 5\Omega/\square$ (for 30 nm thick Mo), R_{sh} = 40-50 Ohm/□ and the metal routings are >500 nm wide. The inset of Fig. 3 verifies that the diagonal and parallel current-voltage characteristics of the nano-TLM structure are within 1% of each other.

To simplify contact resistance extraction and reduce the sensitivity of the results to slit misalignment in the fin, we kept L_c larger than the transfer length (L_c = 200-500 nm). Under these conditions, the contact resistance is insensitive to the exact value of L_c and the fin contact resistance (R_c) can be extracted directly from TLM data extrapolation.

Fig. 3 graphs TLM resistance vs. physical contact distance, D, as obtained by SEM inspection, for fins with F_T = 100 nm. The graph shows normalized data for structures with and without sidewall contacts with W_f of 50 and 300 nm. In all structures, the data is normalized to W_f. It is clear that the narrower fin exhibits higher values of R_{sh} and width-normalized R_c suggesting improper fin width scaling (R_{sh} and normalized R_c should not depend on W_f). In addition, the structures with sidewall contacts yield a higher contact resistance than those without. Since in the WAC structures, the sidewall contact periphery was not taken into account in the normalization, the increased contact resistance shown in Fig. 3 for these devices is underestimated.

A summary of contact resistance and semiconductor sheet resistance measurements for different fin widths is shown in Figs. 4 (a) and (b). These graphs include additional data sets obtained on structures with taller fins (F_T = 200 nm) but the same n+ cap thickness (20 nm). All together, these graphs

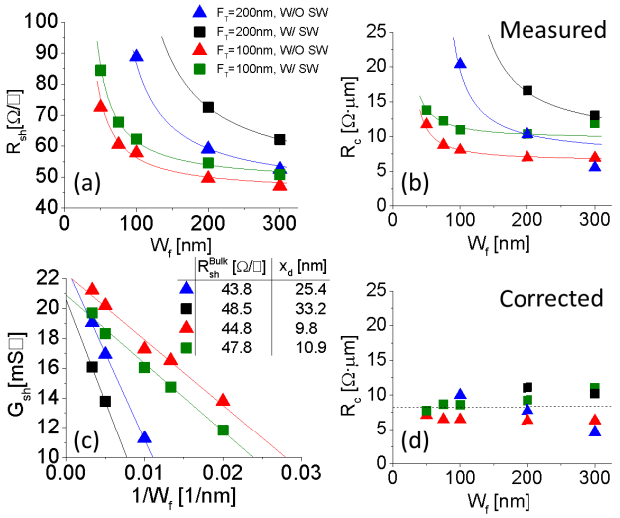

Fig. 4. Sheet resistance (a) and contact resistance (b) as obtained from TLM measurements on structures with different fin height, with and without sidewall contacts. (c) Semiconductor sheet conductivity vs. $1/W_f$ for dead zone estimation. (d) Contact resistance corrected by effective electrical fin width.

collect data from 100 unique devices. A consistent trend emerges. In all data sets, R_{sh} and R_c increase as the fin width is decreased. In taller fins, the width dependence becomes more acute. This behavior could arise from the existence of a "dead zone" that does not contribute to transport and that is associated with the fin sidewalls. Such a dead zone could originate in a depletion region associated with Fermi level pinning at the fin sidewall surface as well as plasma damage during RIE.

A simple model can be constructed if we associate a width, x_d, for the "dead zone" that is associated with each sidewall. In this case, the measured sheet conductivity is given by:

$$\frac{1}{R_{sh}^{m}} = \frac{1}{R_{sh}^{Bulk}}\left(1 - \frac{2x_d}{W_f}\right)$$

where R_{sh}^{m} and R_{sh}^{Bulk} are the measured and bulk sheet conductivity, respectively. This equation suggests that $G_{sh}^{m} \equiv 1/R_{sh}^{m}$ should be proportional to $1/W_f$.

Indeed this dependence is clearly observed in our experiments, as shown in Fig. 4c. From this, we can extract R_{sh}^{Bulk} and x_d. These values are given in the figure inset. The obtained bulk sheet resistance is slightly larger for structures with sidewall contacts. This could be attributed to the longer dry etching required for slit opening as a result of the thicker metal. The inset of Fig. 4c also shows that the dead zone is wider for structures with taller fins. This indicates that the dead zone is at least partially associated with the III-V etching time. In fact, a worse case estimate for the depletion region thickness at the sidewalls is ~ 5 nm. This suggests that sidewall damage is rather likely and that this problem could be partially mitigated by physically removing the dead zone using digital etch [11] and proper annealing.

Given the strong indications that the dead zone partially originates in plasma damage during fin etching, it is reasonable to expect similar damage under the contacts rendering these areas electrically inactive. A more appropriate estimation of the contact resistance should then correct for the dead zone width. Fig. 4 (d) shows the corrected contact resistance for the different process splits. The dead zone correction eliminates the fin width dependence giving credibility to our hypothesis.

The uncorrected contact resistance that we measure spans between 5 and 20 Ω-μm. The average contact resistance after dead-zone correction is $8.0 \pm 1.8\Omega$-μm, corresponding to a transfer length of 200 nm and a contact resistivity of 1.3 Ω-μm^2. These results are somehow higher than those obtained in planar contacts using a similar technology [12]. Nevertheless, our results are promising and represent an order of magnitude improvement with respect to fin-contact resistance obtained in the Ni-InGaAs system [13]. Further research will be dedicated to reducing the contact resistance and minimizing the dead zone trough digital etching, sidewall passivation, thermal annealing and optimization of the InAs cap composition.

IV. Conclusion

We demonstrate a novel contact-first approach for III-V fins in which the contact metal is used as part of the fin-etch mask. We have obtained electrically active contact resistance of around 8 Ω-μm on 50-300 nm wide fins. These results approach the state of the art on similar planar structures and bode well for the prospect of sub-10 nm III-V FinFETs and Trigate MOSFETs.

Acknowledgments

Device fabrication was carried out at the Microsystems Technology Laboratories and the Electron Beam Lithography Facility at MIT.

References

[1] J. A. del Alamo, "Nanometre-scale electronics with III–V compound semiconductors," *Nature*, vol. 479, pp. 317–323, Nov. 2011.
[2] M. Heyns and W. Tsai, "Ultimate scaling of CMOS logic devices with Ge and III–V materials," *MRS Bull.*, vol. 34, no. 7, pp. 485–492, 2009.
[3] H. Riel *et al.*, "III–V compound semiconductor transistors—From planar to nanowire structures," *MRS Bull.*, vol. 39, no. 8, pp. 668–677, 2014.
[4] (2011). *The International Technology Roadmap for Semiconductors*. [Online]. Available: http://www.itrs.net
[5] J. C. Lin, S. Y. Yu, and S. E. Mohney, "Characterization of low-resistance Ohmic contacts to *n*- and *p*-type InGaAs," *J. Appl. Phys.*, vol. 114, no. 4, pp. 044504-1–044504-8, Jul. 2013.
[6] R. Dormaier and S. E. Mohney, "Factors controlling the resistance of Ohmic contacts to *n*-InGaAs," *J. Vac. Sci. Technol. B*, vol. 30, no. 3, pp. 031209-1–031209-10, 2012.
[7] A. Baraskar *et al.*, "Ex situ Ohmic contacts to n-InGaAs," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 28, no. 4, pp. C517–C519, Jul. 2010.
[8] U. Singisetti *et al.*, "Ultralow resistance *in situ* Ohmic contacts to InGaAs/InP," *Appl. Phys. Lett.*, vol. 93, no. 18, pp. 183502-1–183502-3, 2008.
[9] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Sub-30 nm InAs quantum-well MOSFETs with self-aligned metal contacts and sub-1 nm EOT HfO_2 insulator," in *Proc. IEEE IEDM*, Dec. 2012, pp. 32.1.1–32.1.4.
[10] X. Zhao and J. A. del Alamo, "Nanometer-scale vertical-sidewall reactive ion etching of InGaAs for 3-D III–V MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 521–523, May 2014.
[11] J. Lin *et al.*, "A novel digital etch technique for deeply scaled III–V MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 440–442, Apr. 2014.
[12] W. Lu *et al.*, "A test structure to characterize nano-scale Ohmic contacts in III–V MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 178–180, Feb. 2014.
[13] X. Zhang *et al.*, "Multiple-gate $In_{0.53}Ga_{0.47}As$ channel n-MOSFETs with self-aligned Ni-InGaAs contacts," *ECS Trans.*, vol. 45, no. 4, pp. 209–216, 2012.