III-V MOSFETs for Future CMOS

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***Abstract* — In the last few years, as Si electronics faces mounting difficulties to maintain its historical scaling path, transistors based on III-V compound semiconductors have emerged as a credible alternative. To get to this point, fundamental technical problems had to be solved. Nevertheless, there are still many challenges that need to be addressed before the first non-Si CMOS technology becomes a reality. This paper reviews recent progress as well as challenges of III-V electronics for future logic applications.**

***Index Terms* — III-V, InGaAs, CMOS, QW-MOSFET.**

I. Introduction

The increasing difficulty of Si to support the historical rate of progress of CMOS scaling known as Moore's Law has prompted the search for alternative channel materials with enhanced transport characteristics. The difficulties of Si can be appreciated in Fig. 1 which plots the current density of n- and p-channel Si MOSFETs as a function of year of introduction. Current density matters because the capacitance per unit area of transistors scales up as the devices are reduced in size and parasitics become more prominent. Maintaining performance then demands continued improvements in current density. Fig. 1 indicates that the rate of progress has stagnated in the last few years. The strong impact of strain on p-channel MOSFET performance has partially alleviated the problem, but this benefit is also seen to saturate. Further progress seems difficult based on Si alone.

At the heart of Si's difficulties is the need to reduce the operating voltage as transistor density increases but the power density budget remains unchanged. Progress is going to require new semiconductors and device concepts that deliver higher current density at a lower voltage. Among possible candidates, InGaAs has recently emerged as a leading contender for n-channel MOSFETs while InGaSb is attractive for p-channel MOSFETs [1,2]. The rational for this is seen in Fig. 2 which graphs electron (red) and hole (blue) inversion-layer and quantum-well mobility of selected semiconductors as a function of their actual lattice constant [1]. For electrons, InGaAs stands out with mobilities that easily exceed 10,000 cm^2/V.s. at room temperature. For holes, compressively strained InGaSb and Ge (the arrows represent increasing compressive biaxial strain) are promising.

While the first InGaAs MOSFETs were demonstrated over 30 years ago, only recently significant progress has taken place. The dramatically different historical evolution of InGaAs MOSFETs and HEMTs is evident in Fig. 3 [3]. There is a striking transconductance gap between the two types of devices that lasted for over 25 years. It is only in the last decade that InGaAs MOSFETs have finally emerged as a viable transistor architecture. In fact, in the last year, the g_m of an InGaAs MOSFET has come to match that of the best InGaAs HEMT [4].

The remarkable recent progress of InGaAs MOSFETs stems from the finding that high-permittivity oxides formed by Atomic-Layer Deposition (ALD) yield an unpinned Fermi-level interface [5]. This is particularly significant because ALD is an ex-situ technique already well established in Si manufacturing [3].

This paper provides an overview of recent progress in III-V MOSFETs with emphasis on InGaAs-based devices.

II. Recent Progress on InGaAs MOSFETs

Fig. 4 shows the evolution of MOSFET design in its quest for reduced footprint and enhanced transistor density. The challenge of transistor scaling is balancing performance at reduced voltage (i.e. current density) and short-channel effects. Footprint scaling demands scaling of all dimensions including the gate length. In order to mitigate short-channel effects, enhanced gate control is required. This has dictated an evolution from the bulk planar MOSFET to an ultra-thin body MOSFET and eventually to multi-gate structures such as the FinFET, Tri-gate MOSFET and the Gate-All-Around Nanowire MOSFET. All these device structures have been demonstrated in the InGaAs system [2].

Fig. 5 shows a conceptual cross-section of a self-aligned Quantum-Well (QW) InGaAs MOSFET [4]. This device represents the state of the art among planar MOSFETs. The fabrication flow features CMOS-compatible materials and processes with extensive use of RIE. This is the device that at the time of this writing holds the g_m record with a value of 3.1 mS/μm at a V_{ds}=0.5 V. A TEM cross-section of a 20 nm gate length device is shown in Fig. 6. This process achieves very tight self-alignment as evident in the 15 nm gate-to-contact distance that is demonstrated.

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A recent gate-length and channel thickness scaling study of this device structure has revealed that the planar QW-MOSFET is essentially at the limit of scaling at a gate length of about 50 nm. This is illustrated in the evolution of the subthreshold swing in Fig. 7 [4].

Other self-aligned MOSFET architectures have been successfully demonstrated. A raised selectively-grown source and drain design has recently yielded excellent results [6]. Self-aligned ion-implanted schemes [7] and self-aligned Ni-InGaAs contact approaches [8] are also promising. The scaling potential of these alternative designs is unlikely to be very different from those in [4].

Planar MOSFETs, though unable to meet the scaling goals, constitute an excellent platform for process development and device physics exploration. A recent example is the identification of the physics behind excess off-state current in tight-pitch InGaAs QW-MOSFETs [9]. As Fig. 8 shows, this excess off-state current is strongly gate length dependent making it highly problematic in nanoscale devices. Recent analysis has revealed that this current is due to band-to-band tunneling (BTBT) at the drain-end of the channel amplified by a parasitic lateral bipolar transistor formed by the channel (floating base), the source (emitter) and drain (collector) of the MOSFET. The bipolar gain can easily approach ~10^3 making even a small BTBT current a great concern. Mitigating this phenomenon is a key goal for future scaled devices.

Improved scalability requires 3D device designs. InGaAs Tri-gate MOSFETs have been demonstrated with fins formed by either RIE [10] or selective growth [11]. They have shown improved scalability though performance is still lacking.

The ultimate scalable MOSFET design is the nanowire architecture. In particular, the vertical nanowire (VNW) MOSFET is attractive because with a vertical current flow, footprint scaling and gate length scaling are uncoupled. This promises high transistor density with acceptable short-channel effects. VNW-MOSFETs also offer a plausible path for Si integration since selective epitaxial growth on templated Si substrates is relatively well established [2]. Still, RIE offers an expeditious approach to investigating VNW-MOSFET design and physics (Fig. 9). VNW InGaAs MOSFETs by RIE have been demonstrated (Fig. 10). Single-NW devices with diameter in the 30 nm range show well behaved electrical characteristics though they also reveal vulnerability to even a few interface states or trapping centers (Fig. 11).

III. Conclusions

Impressive recent III-V MOSFET progress gives hope for Moore's law to go beyond the point where Si can reach. Vertical Nanowire MOSFETs are the ultimate scalable MOSFET structure. Recent demonstrations of self-aligned planar and VNW-MOSFETs give credibility to the use of III-Vs in sub-10 nm CMOS nodes.

Acknowledgments

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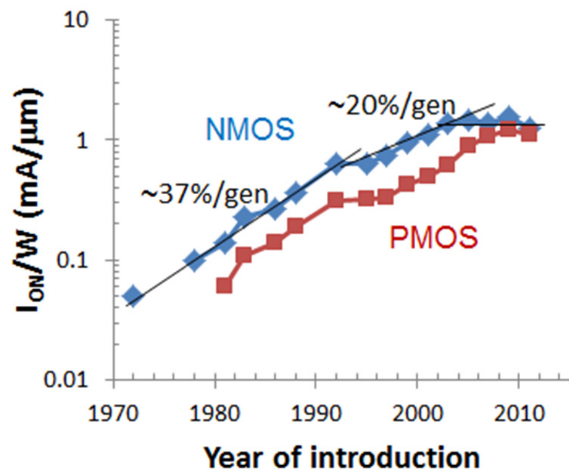

Fig. 1. ON-current (I_{on}) scaling trend of NMOS and PMOS transistors *vs.* year of introduction of CMOS technology.

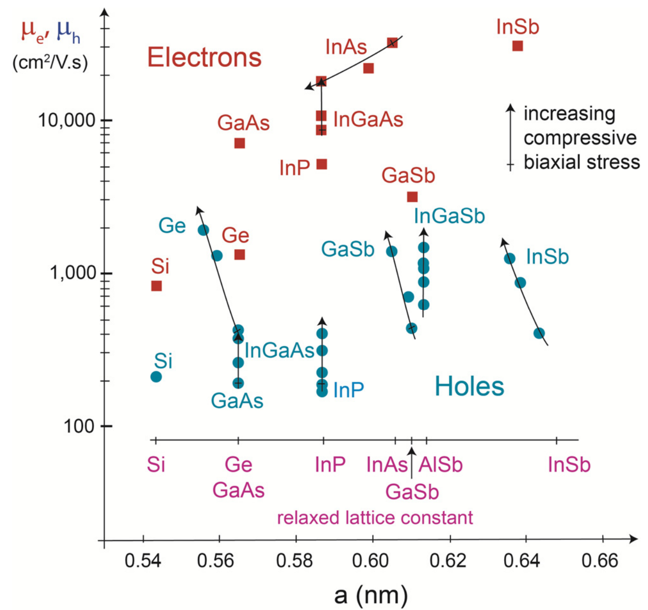

Fig. 2. Electron and hole mobility of Si, Ge and III–V compound semiconductors. The highest room-temperature mobility of electrons (red) and holes (blue) in inversion layers and quantum wells is shown as a function of the actual semiconductor lattice constant. The mobilities are reported for any sheet carrier concentration. For relaxed layers under no strain, the lattice constant is its natural one, as shown on the scale. For pseudomorphic layers, which are perfectly strained on a substrate with a different lattice constant, the lattice constant is that of the substrate. The impact of biaxial strain is indicated by an arrow representing increasing compressive biaxial strain.

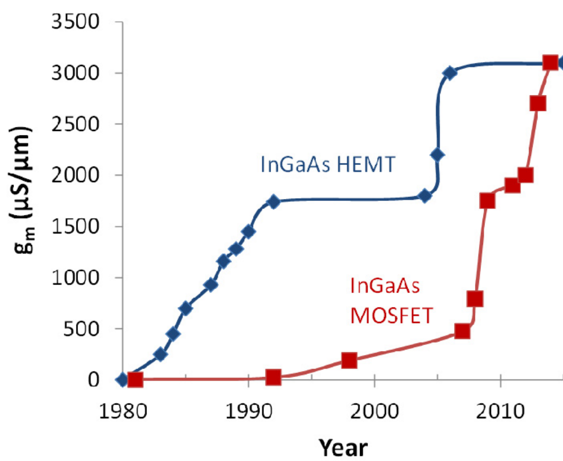

Fig. 3. Transconductance comparison of inversion-type InGaAs MOSFETs and HEMTs (with InAs composition between 0 and 1) *vs.* year.

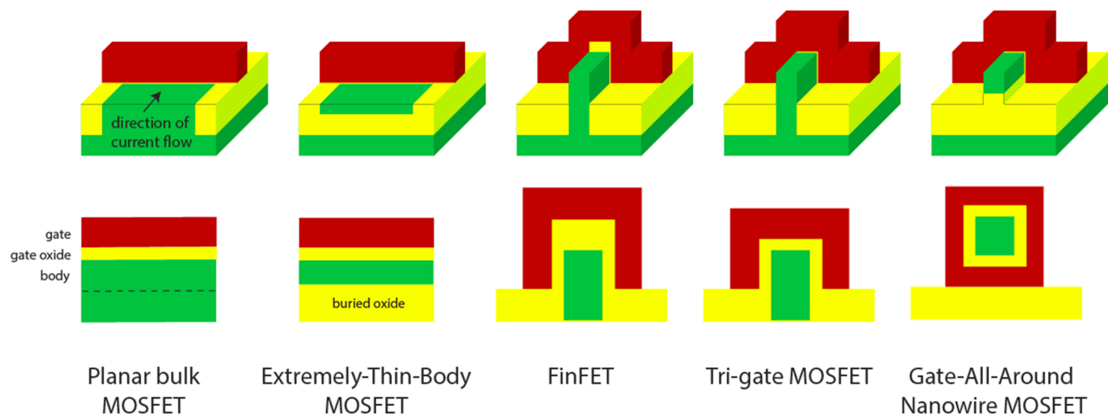

Fig. 4. 3D schematic (top) and cross-sectional schematic (bottom) of MOSFET structures with increasing electrostatic gate control. In Planar bulk and Extremely-Thin-Body MOSFETs, channel charge is electrostatically controlled by gating from the device surface. In FinFETs, gate action takes places from two sides in a fin-shaped channel. In Tri-gate MOSFETs, the gate wraps around three sides. The "Gate-All-Around" nanowire MOSFET has a thin nanowire channel that is wrapped in its entire periphery by the gate.

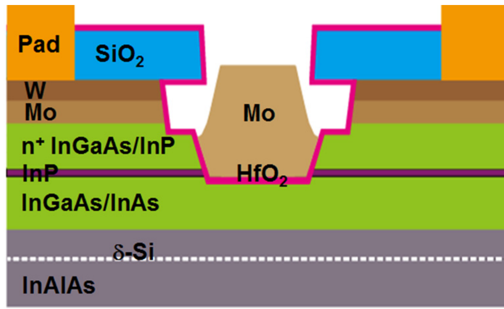

Fig. 5. Cross-sectional schematic of a self-aligned thin-body InGaAs QW-MOSFET [4].

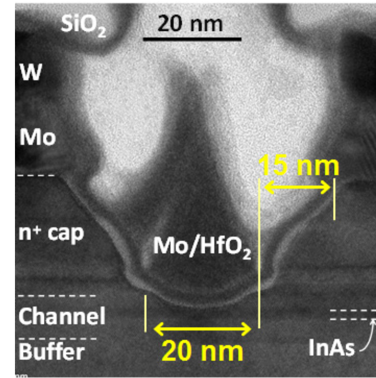

Fig. 6. Cross-sectional TEM image of a self-aligned InGaAs QW-MOSFET with L_g=20 nm. The length of the access region between the edge of the channel and the edge of the ohmic contact is L_{access}=15 nm [4].

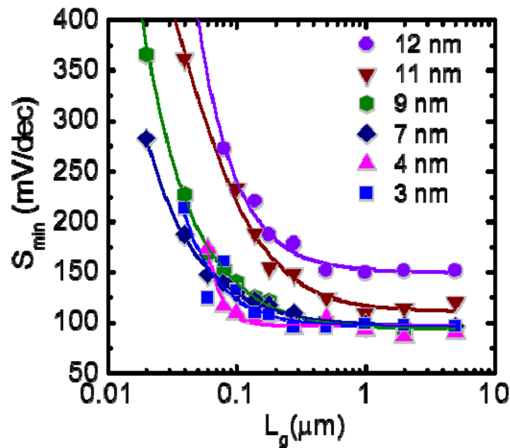

Fig. 7. Minimum subthreshold swing (S_{min}) of InGaAs QW-MOSFETs as a function of gate length (L_g) for channel thickness (t_c) from 3 nm to 12 nm. This planar QW-MOSFET structure is at the limit of scaling around L_g=50 nm [4].

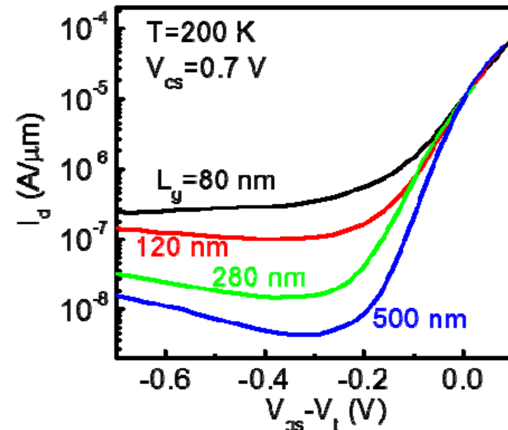

Fig. 8. Subthreshold I_d *vs.* V_{gs}-V_t characteristics of InGaAs QW-MOSFETs for gate lengths between 80 and 500 nm, measured at V_{ds}=0.7 V and at 200 K [9].

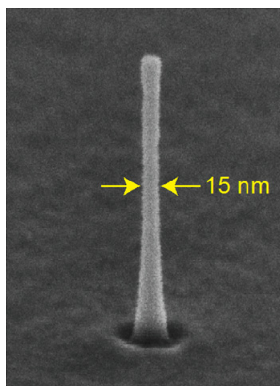

Fig. 9. 15-nm-diameter InGaAs nanowire with aspect ratio over 15 and steep sidewall. The nanowire is fabricated by an optimized RIE process [12].

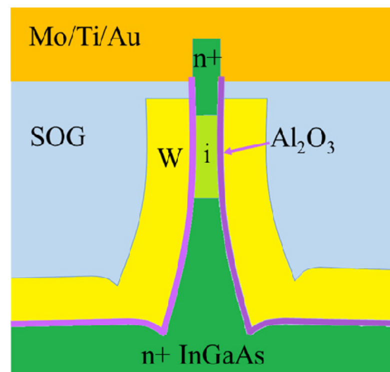

Fig. 10. Schematic of an InGaAs vertical NW-MOSFET fabricated by a top-down approach [12].

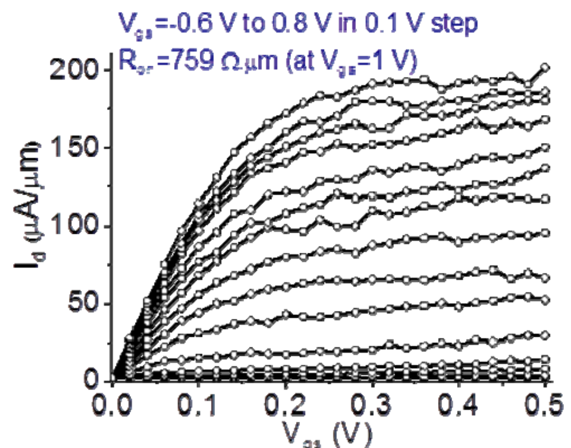

Fig. 11. Output characteristics of a 30-nm-diameter InGaAs single NW-MOSFET [12].