

A Test Structure to Characterize Nano-Scale Ohmic Contacts in III-V MOSFETs

Wenjie Lu, Alex Guo, Alon Vardi, and Jesús A. del Alamo, *Fellow, IEEE*

Abstract—We propose and demonstrate a novel test structure to characterize the electrical properties of nano-scale metal–semiconductor contacts. The structure is in essence a two-port transmission line model (TLM) with contacts in the nanometer regime. Unlike the conventional TLM, two types of Kelvin measurements are possible. When performed on devices with different contact spacing, this allows the extraction of the contact resistance, the semiconductor sheet resistance, and the metal sheet resistance. For this, a 2-D distributed resistive network model has been developed. We demonstrate this technique in Mo/n⁺-InGaAs contacts with contact lengths from 19 to 450 nm where we have measured an average contact resistivity of $0.69 \pm 0.3 \Omega \cdot \mu\text{m}^2$. For relatively long contacts (>110 nm), this corresponds to an extremely small contact resistance of $6.6 \pm 1.6 \Omega \cdot \mu\text{m}$.

Index Terms—Nano contacts, TLM, contact resistivity, III-V MOSFET.

I. INTRODUCTION

THE III-V MOSFET is one of the most promising technologies to extend Moore’s law beyond the limits of Si [1], [2]. In these devices, contact resistance remains a great challenge. At the insertion point, III-V logic transistors must have contacts in the 10–15 nm length range while delivering a total source resistance of $50 \Omega \cdot \mu\text{m}$ [1], [3]. To meet this goal, the metal to semiconductor contact resistivity ρ_c needs to be lower than $0.5 \Omega \cdot \mu\text{m}^2$. Low values of ρ_c for contacts on n⁺-InGaAs between 0.4 and $3.2 \Omega \cdot \mu\text{m}^2$ have been reported [4]–[7]. Currently, the contact resistance in lateral devices is mostly extracted using a TLM structure [8] or a four-terminal Kelvin test structure [9]. In a TLM, the contacts are very large, they are separated by a distance in the scale of microns and the metal resistance is neglected. However, when dealing with nano-scale contacts for future CMOS, we need a more accurate test structure capable of extracting extremely small values of contact resistance on very small contacts where the metal resistance can be significant. Addressing this need is the goal of this letter.

In this letter, we propose a new two-port TLM structure with nano-scale contacts separated by nanometer-range distances.

Manuscript received November 13, 2013; revised December 11, 2013; accepted December 13, 2013. Date of publication January 9, 2014; date of current version January 23, 2014. This work was supported in part by the Focus Center for Materials, Structures and Devices, in part by SRC, and in part by Intel Corporation. The review of this letter was arranged by Editor M. Passlack.

The authors are with the Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: wenjie@mit.edu).

Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LED.2013.2295328

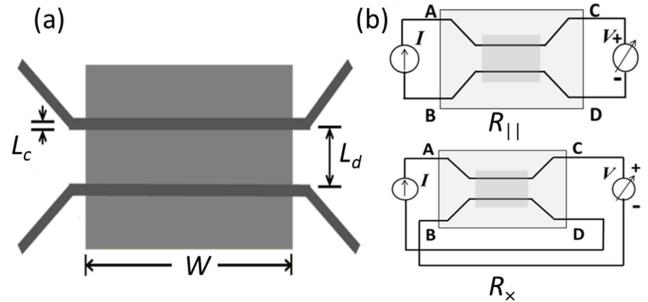


Fig. 1. (a) Schematic top-down view of a single nano-TLM test structure. (b) Two Kelvin measurement schemes used to characterize the nano-TLM test structure.

We model the structure through a 2D distributed circuit network. The model allows the simultaneous extraction of the contact resistance, R_c , the semiconductor sheet resistance, R_{sh} , and the metal sheet resistance, R_{shm} . The proposed approach is demonstrated by fabricating Mo nano-contacts on n⁺-InGaAs heterostructures where we have extracted an average contact resistivity as low as $0.69 \Omega \cdot \mu\text{m}^2$. This matches the state-of-the-art in this metal/semiconductor system [4]–[7]. The proposed test structure and model is not limited to III-V MOSFETs and can be used to analyze nano-scale contacts in any material system.

II. NANO-TLM DESIGN AND MODELING

Fig. 1(a) shows a schematic of our proposed nano-TLM test structure. The shaded area indicates the active semiconductor region, on which there are two parallel thin metal contacts of length L_c , width W , separated by a distance L_d . A unique aspect of this structure is that the two nano-scale metal lines can be contacted at both ends separately. This enables the two Kelvin measurement schemes illustrated in Fig. 1(b). $R_{||}$, the parallel terminal resistance, is typical of the traditional TLM structure. This structure additionally allows the measurement of R_x the cross terminal resistance. The combination of $R_{||}$ and R_x enables accurate extractions of R_c , R_{sh} , and R_{shm} . In actual measurements, the forcing and sensing ports are interchanged so that four sets measurements per elemental test structure can be performed.

Fig. 2 shows a distributed circuit representation of the intrinsic structure of Fig. 1(a). Since Kelvin measurements eliminate the resistance of the extrinsic metal lines, pads and probes, these elements need not be modeled. However, unlike conventional TLMs in which the metal resistance in the

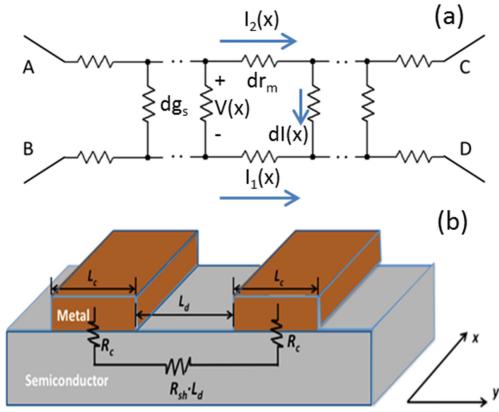


Fig. 2. (a) 2D distributed resistive circuit network of nano-TLM. (b) Cross-sectional view of a nano-TLM with equivalent circuit network.

intrinsic device is not modeled, here it is taken into account. In Fig. 2(a), dr_m is the elemental longitudinal resistance of the metal line given by:

$$dr_m = \frac{R_{shm}}{L_c} dx \quad (1)$$

dg_s is the elemental metal to metal conductance through the contacts and the semiconductor. Referring to the cross-sectional view of the nano-TLM structure of Fig. 2, dg_s can be expressed as:

$$dg_s = \frac{1}{R_{TLM}} dx \quad (2)$$

where R_{TLM} is given as in the conventional TLM [8] :

$$R_{TLM} = 2R_c + R_{sh} \cdot L_d \quad (3)$$

here R_c is the normalized contact resistance. An analysis of the distributed model of Fig. 2 yields the following expressions for the terminal resistances defined in Fig. 1(b):

$$R_{||} = \frac{R_{TLM}}{L_{Tx}} \csc h \left(\frac{W}{L_{Tx}} \right) \quad (4)$$

$$R_x = \frac{R_{TLM}}{2L_{Tx}} \left[\csc h \left(\frac{W}{L_{Tx}} \right) + \coth \left(\frac{W}{L_{Tx}} \right) \right] - \frac{R_{shm} W}{2L_c} \quad (5)$$

where L_{Tx} is the transfer length in the x direction:

$$L_{Tx} = \sqrt{\frac{L_c \cdot R_{TLM}}{2R_{shm}}} \quad (6)$$

As R_{shm} goes to zero, both (4) and (5) converge to R_{TLM}/W , which coincides with the classic normalized TLM result.

Fig. 3(a) shows model predictions for $R_{||}$ and R_x as a function of contact separation for different contact lengths. In long contacts, $R_{||}$ and R_x approach each other. In short contacts, however, R_x drops below $R_{||}$ due to the negative term in (5) which captures the voltage drop along the thin metal line.

The model provides guidance to test structure design for accurate extraction of the contact resistance. In general, one would like to have many test structures with identical L_c and different L_d . In particular, one needs: (1) a thick metal layer

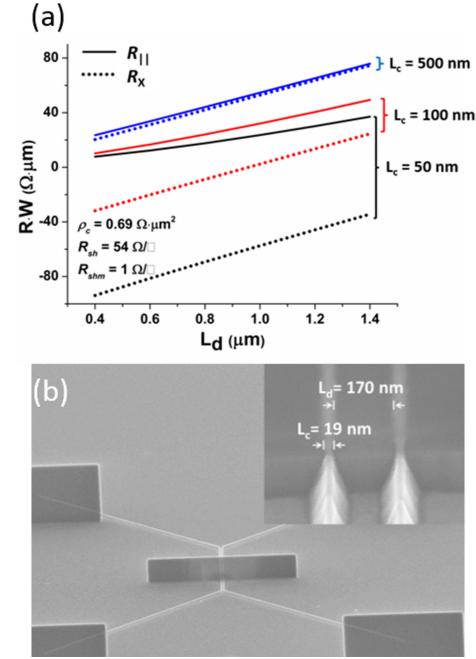


Fig. 3. (a) Modeled terminal resistances versus contact spacing for various contact lengths. (b) SEM image of fabricated Mo/n⁺-InGaAs nano-TLM structure. The inset shows a nano-TLM test structure with 19 nm long contact and 170 nm contact spacing.

to minimize R_{shm} , (2) small values of L_d to reduce the impact of R_{sh} , and (3) a small value of W to also mitigate the impact of R_{shm} . The model above suggests that W should be on the order of L_{Tx} which in our system is in the range of 1–4 μm . Reasonably small W also makes the mesa alignment easy. In our devices we have selected $W = 3 \mu\text{m}$.

III. EXPERIMENTS

We have demonstrated the proposed nano-TLM structure in the Mo/n⁺-In_{0.53}Ga_{0.47}As (20 nm thick, Si-doped, $N_D = 1 \times 10^{19} \text{ cm}^{-3}$) system. We first sputter 60 nm Mo onto the clean fresh semiconductor surface. This metal-first approach has been found to give outstanding contact resistance in InGaAs HEMTs and MOSFETs [10], [11]. The Mo nano-contacts are defined by E-beam lithography followed by RIE. The entire structure is then covered by CVD SiO₂ and the mesas are patterned and isolated by RIE. The depth of mesa etch is 130 nm, which is sufficient for current confinement since only the top 20 nm cap layer is conductive. After pad formation, the structure is annealed at 350 °C in N₂ for 1 min. We have fabricated test structures with contact lengths in the 19 to 450 nm range and contact spacings between 1.4 μm and below. Fig. 3(b) shows a test structure with 19 nm Mo contacts. All the relevant dimensions are measured by scanning electron microscope in the finished devices for accurate analysis.

In each elemental test structure, the four Kelvin measurements mentioned above are performed. The discrepancy in the two measurements of $R_{||}$ or R_x is less than 1%. From measurements of test structures with identical nominal L_c and different L_d (we call this a “set”), using a nonlinear least-square fitting program, we extract the values of R_c , R_{sh} and R_{shm} that minimize the error. For accurate extraction, $R_{||}$

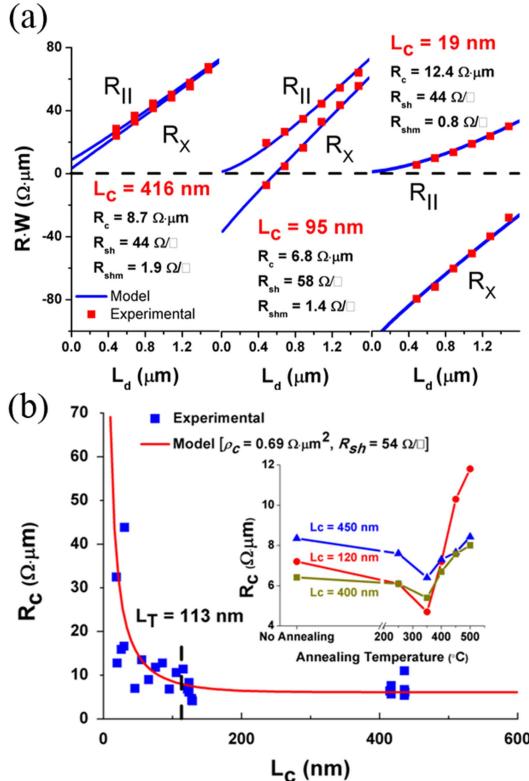


Fig. 4. (a) R_{\parallel} and R_X of nano-TLMs with average contact lengths of 416, 95, and 19 nm. (b) Contact resistance versus contact length for $\text{Mo}/\text{n}^+/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ contacts, with an average contact resistivity of $0.69 \pm 0.3 \Omega \cdot \mu\text{m}^2$. The inset shows the thermal stability of the Mo contacts.

and R_X are fitted simultaneously. Examples from three sets of test structures with $L_c = 416$, 95, and 19 nm are shown in Fig. 4(a). Even for relatively large 95 nm contacts, there is a remarkable split between the two measurement schemes, R_{\parallel} and R_X , and they split further for smaller contacts. Moreover, while R_{\parallel} is always positive, R_X can become negative for small contacts, consistent with the prediction of the model in Fig. 3(a).

Since we expect non-uniformities in test structure fabrication, we allow R_{sh} and R_{shm} to change from test structure set to set. The obtained values of R_{sh} and R_{shm} have average values of $54 \Omega/\square$ and $1.2 \Omega/\square$, and standard deviations of $4.3 \Omega/\square$ and $0.2 \Omega/\square$, respectively. To verify the accuracy of our extractions, we also obtained R_{sh} and R_{shm} from conventional TLMs and Van der Pauw structures elsewhere on the sample. The average discrepancy of R_{sh} and R_{shm} are 10% and 16% across the sample.

Fig. 4(b) shows the dependence of $\text{Mo}/\text{n}^+/\text{InGaAs}$ contact resistance on contact length obtained in 30 sets of test structures, a collective of 180 nano-TLM devices. For relatively long contacts, an extremely small average $R_c = 6.6 \pm 1.6 \Omega \cdot \mu\text{m}$ is achieved. R_c shoots up as the contact length becomes smaller than the transfer length in the y direction:

$$L_T \approx \sqrt{\rho_c / R_{sh}} \quad (7)$$

which is about 113 nm for this contact system, assuming that $R_{sh} \gg R_{shm}$. We have used the standard TLM model as in [8] to extract the contact resistivity, and we find

$\rho_c = 0.69 \pm 0.3 \Omega \cdot \mu\text{m}^2$ for all contact lengths. Fig. 4(b) shows that the simple model using the extracted ρ_c and R_{sh} provides a good match to the entire data set. In the extraction of ρ_c , we assume the semiconductor sheet resistance remains the same under the metal contact [12]. This value of ρ_c supersedes the one erroneously reported in [13] due to a flawed extraction. The inset of Fig. 4(b) also shows sequential measurements of R_c after N_2 annealing for 1 min at increasing temperature. These results suggest that Mo/InGaAs contacts are thermally stable up to at least 400 °C, in good agreement with [7], [11].

IV. CONCLUSION

We have proposed a new two-port TLM test structure to characterize nano-scale contacts. We demonstrate this concept in $\text{Mo}/\text{n}^+/\text{InGaAs}$ contacts with contact lengths in the 19–450 nm range. With the help of a 2D distributed resistive circuit network, we have extracted the contact resistance of contacts as short as 19 nm. Our entire data set is well described by a contact resistivity of $\rho_c = 0.69 \pm 0.3 \Omega \cdot \mu\text{m}^2$ which is close to the requirements for future nanometer-scale CMOS.

ACKNOWLEDGMENT

Device fabrication was carried out at the Microsystems Technology Laboratories and the Electron Beam Lithography Facility at MIT. The author would like to thank useful discussions with Prof. D. A. Antoniadis and J. Lin.

REFERENCES

- [1] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, pp. 317–323, Nov. 2011.
- [2] M. Heyns and W. Tsai, "Ultimate scaling of CMOS logic devices with Ge and III-V materials," *MRS Bull.*, vol. 34, pp. 485–492, 2009.
- [3] *The International Technology Roadmap for Semiconductors*. (2011) [Online]. Available: <http://www.itrs.net>
- [4] J. C. Lin, S. Y. Yu, and S. E. Mohney, "Characterization of low-resistance ohmic contacts to n- and p-type InGaAs," *J. Appl. Phys.*, vol. 114, pp. 044504-1–044504-8, Jul. 2013.
- [5] R. Dormaier and S. E. Mohney, "Factors controlling the resistance of ohmic contacts to n-InGaAs," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 30, no. 3, pp. 031209-1–031209-10, 2012.
- [6] A. Baraskar, M. A. Wistey, E. Lobisser, et al., "Ex-situ ohmic contacts to n-InGaAs prepared by atomic hydrogen cleaning," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 28, pp. C517–C519, Aug. 2010.
- [7] A. Baraskar, A. C. Gossard, and M. J. W. Rodwell, "Lower limits to metal-semiconductor contact resistance: Theoretical models and experimental data," *J. Appl. Phys.*, vol. 114, no. 15, pp. 154516-1–154516-9, 2013.
- [8] H. Murrmann and D. Widmann, "Current crowding on metal contacts to planar devices," *IEEE Trans. Electron Devices*, vol. 16, no. 12, pp. 1022–1024, Dec. 1969.
- [9] S. J. Proctor, L. W. Linholme, and J. A. Mazer, "Direct measurements of interfacial contact resistance, end contact resistance, and interfacial contact layer uniformity," *IEEE Trans. Electron Devices*, vol. 30, no. 11, pp. 1535–1542, Nov. 1983.
- [10] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Sub-30 nm InAs quantum-well MOSFETs with self-aligned metal contacts and sub-1 nm EOT HfO_2 insulator," in *Proc. IEEE IEDM*, Dec. 2012, pp. 32.1.1–32.1.4.
- [11] T. W. Kim, D. H. Kim, and J. A. del Alamo, "60 nm self-aligned-gate InGaAs HEMTs with record high-frequency characteristics," in *Proc. IEEE IEDM*, Dec. 2010, pp. 30.7.1–30.7.4.
- [12] G. K. Reeves and H. B. Harrison, "Obtaining the specific contact resistance from transmission line model measurements," *IEEE Electron Device Lett.*, vol. 3, no. 5, pp. 111–113, May 1982.
- [13] A. Guo and J. A. del Alamo, "Mo/ n^+ /InGaAs nanocontacts for future III-V MOSFETs," in *Proc. 40th ISCS*, Japan, May 2013, paper MoC4-5.