InGaAs MOSFET Electronics

J. A. del Alamo

Microsystems Technology Laboratories, MIT

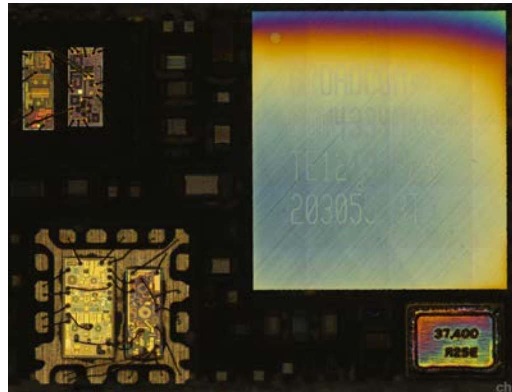
The 17th International Symposium
Physics of Semiconductors and Applications

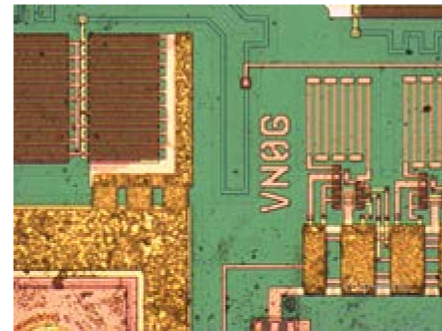
Jeju, Korea, December 7-11, 2014

Acknowledgements:

- D. Antoniadis, A. Guo, L. Guo, D.-H. Kim, T.-W. Kim, D. Jin, J. Lin, W. Lu, A. Vardi, N. Waldron, L. Xia
- Sponsors: Intel, FCRP-MSD, ARL, SRC, NSF, Sematech, Samsung
- Labs at MIT: MTL, NSL, SEBL

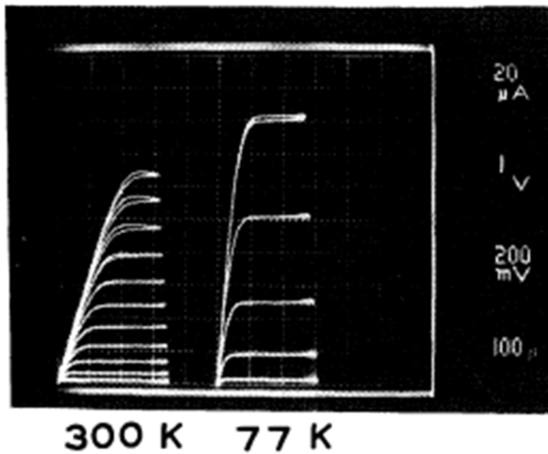
InGaAs electronics in your pocket!



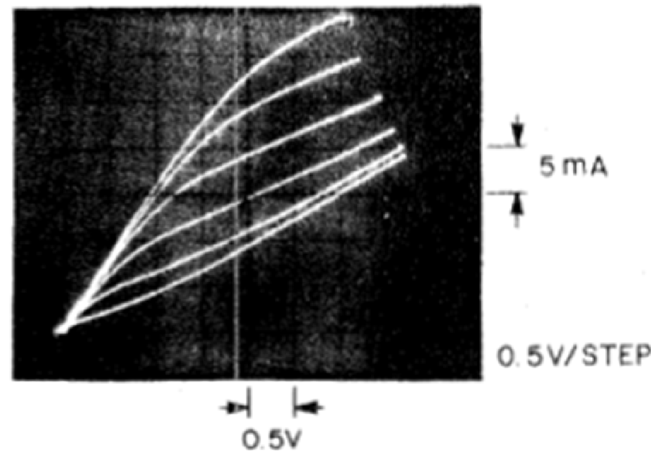


A bit of perspective…

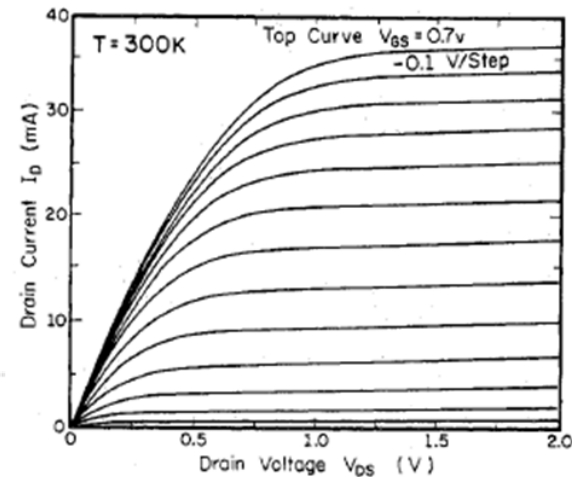
- Invention of AlGaAs/GaAs HEMT: Fujitsu Labs. 1980
- First InAlAs/InGaAs HEMT on InP: Bell Labs. 1982
- First AlGaAs/InGaAs Pseudomorphic HEMT: U. Illinois 1985
- Main attraction of InGaAs: RT μ_e = 6,000~30,000 cm^2/V.s



Mimura, JJAPL 1980

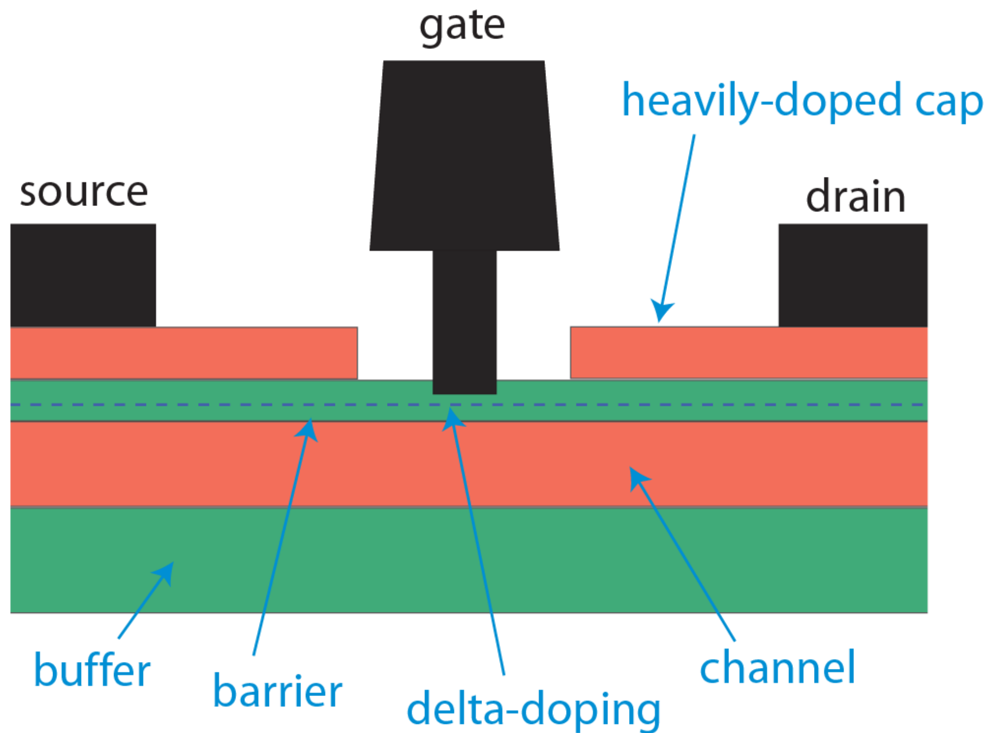


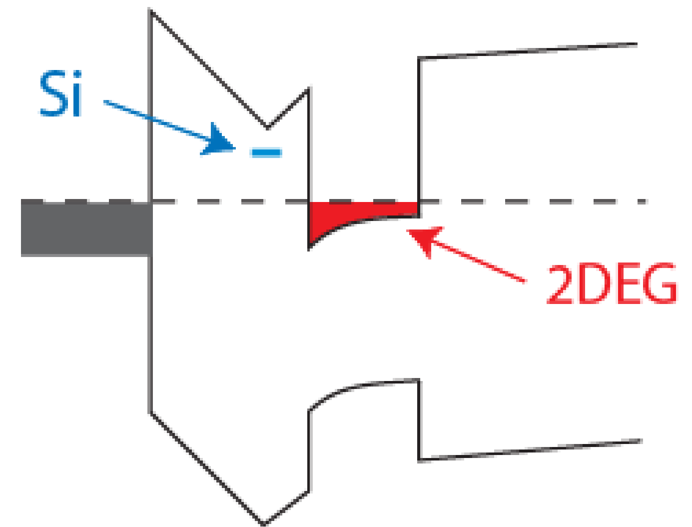
Chen, EDL 1982



Ketterson, EDL 1985

InGaAs High Electron Mobility Transistor (HEMT)

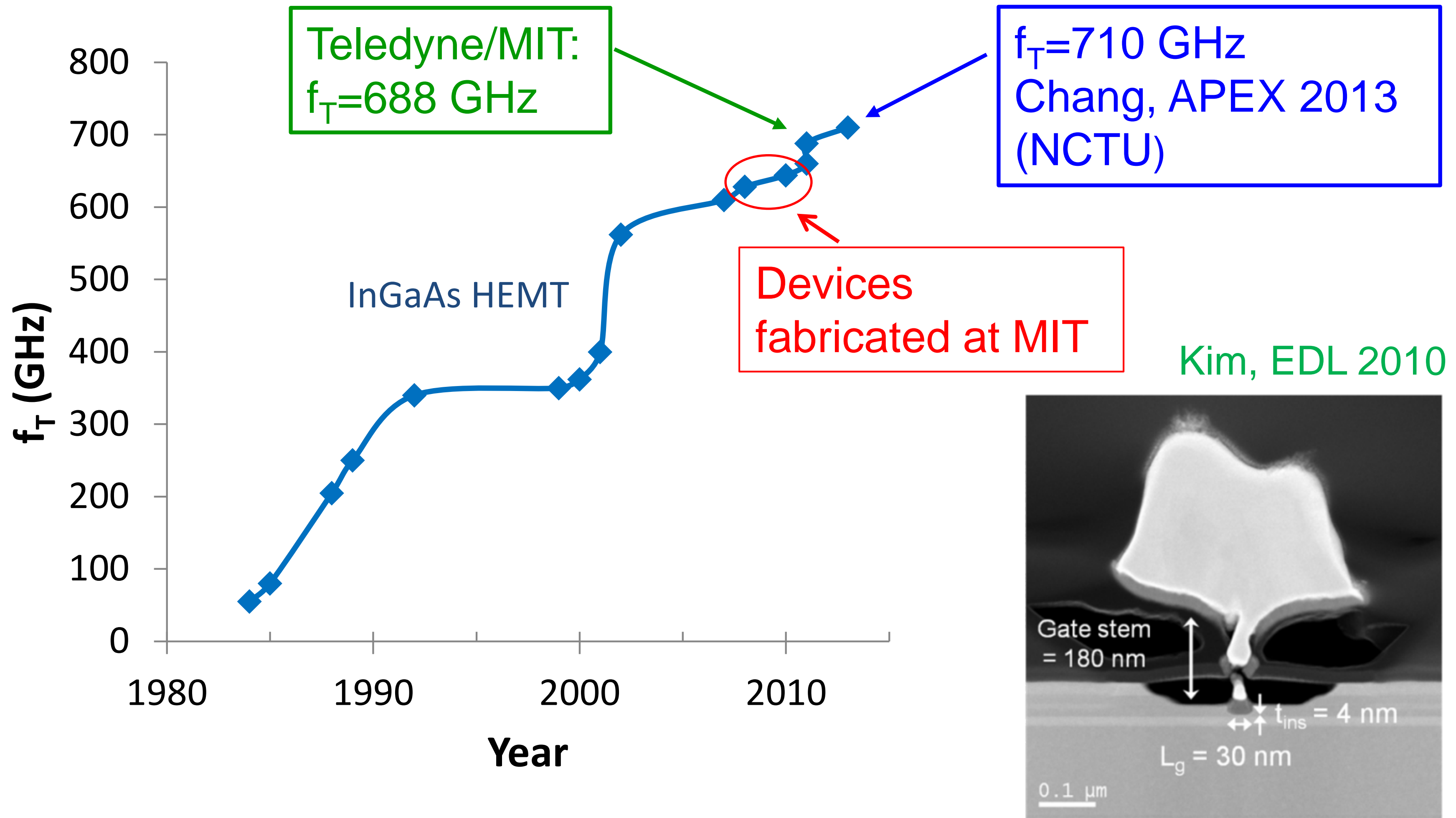




Modulation doping:

→ 2-Dimensional Electron Gas in narrow-bandgap channel

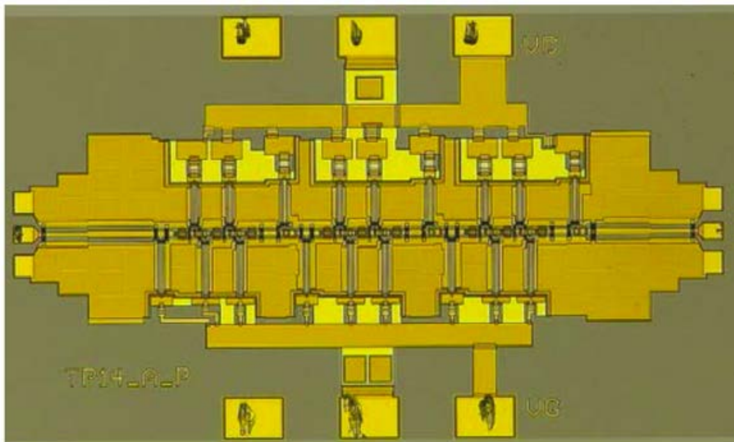
InGaAs HEMT: high-frequency record vs. time



Highest f_T of any FET on any material system

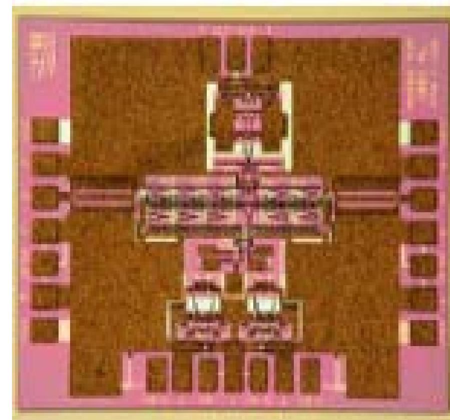
InGaAs HEMTs: circuit demonstrations

9-stage 850 GHz LNA

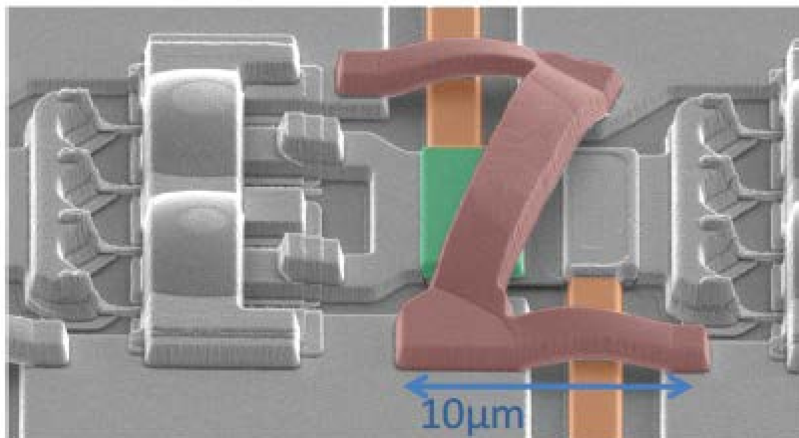


Deal, MTT-S 2014

80 Gb/s multiplexer IC

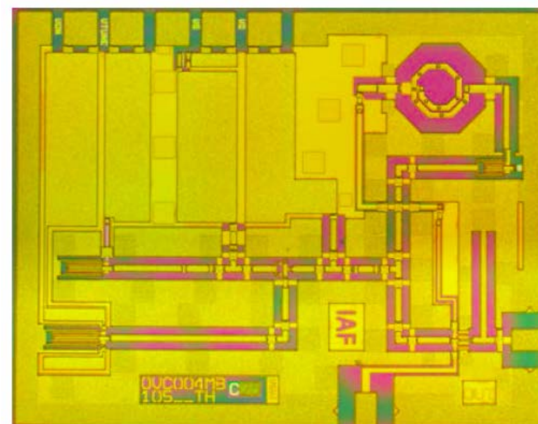


Wurfl, GAAS 2004



Sarkozy, IPRM 2013

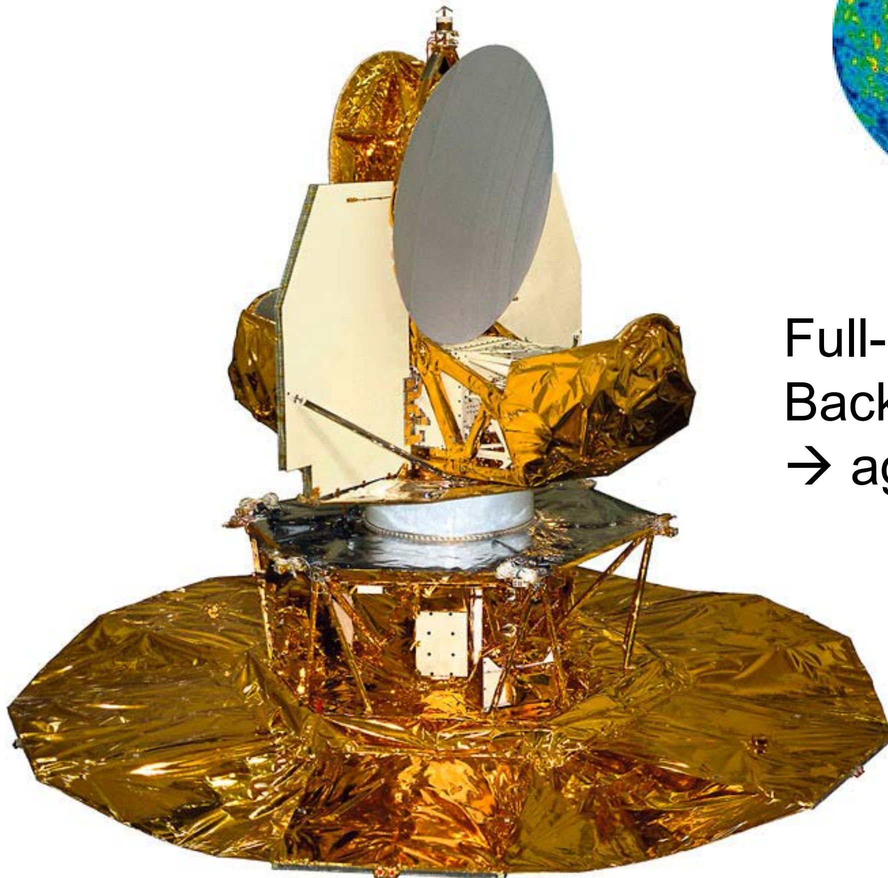
25 Gb/s wireless data at 113 GHz

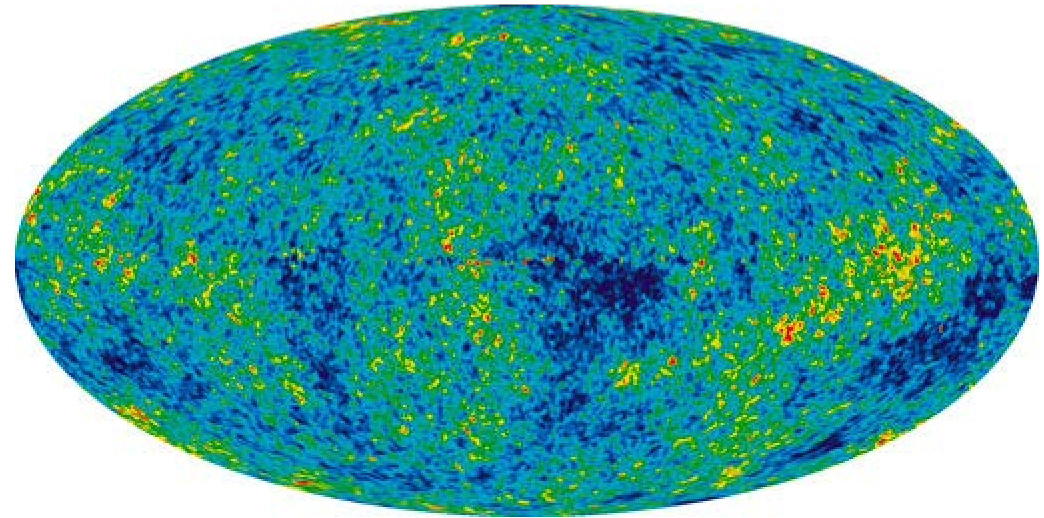


Thome, MTT-S 2014

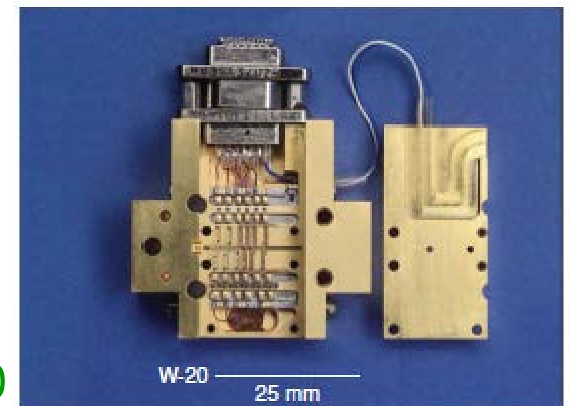
InGaAs HEMTs map infant universe

WMAP=*Wilkinson Microwave Anisotropy Probe*
Launched 2001





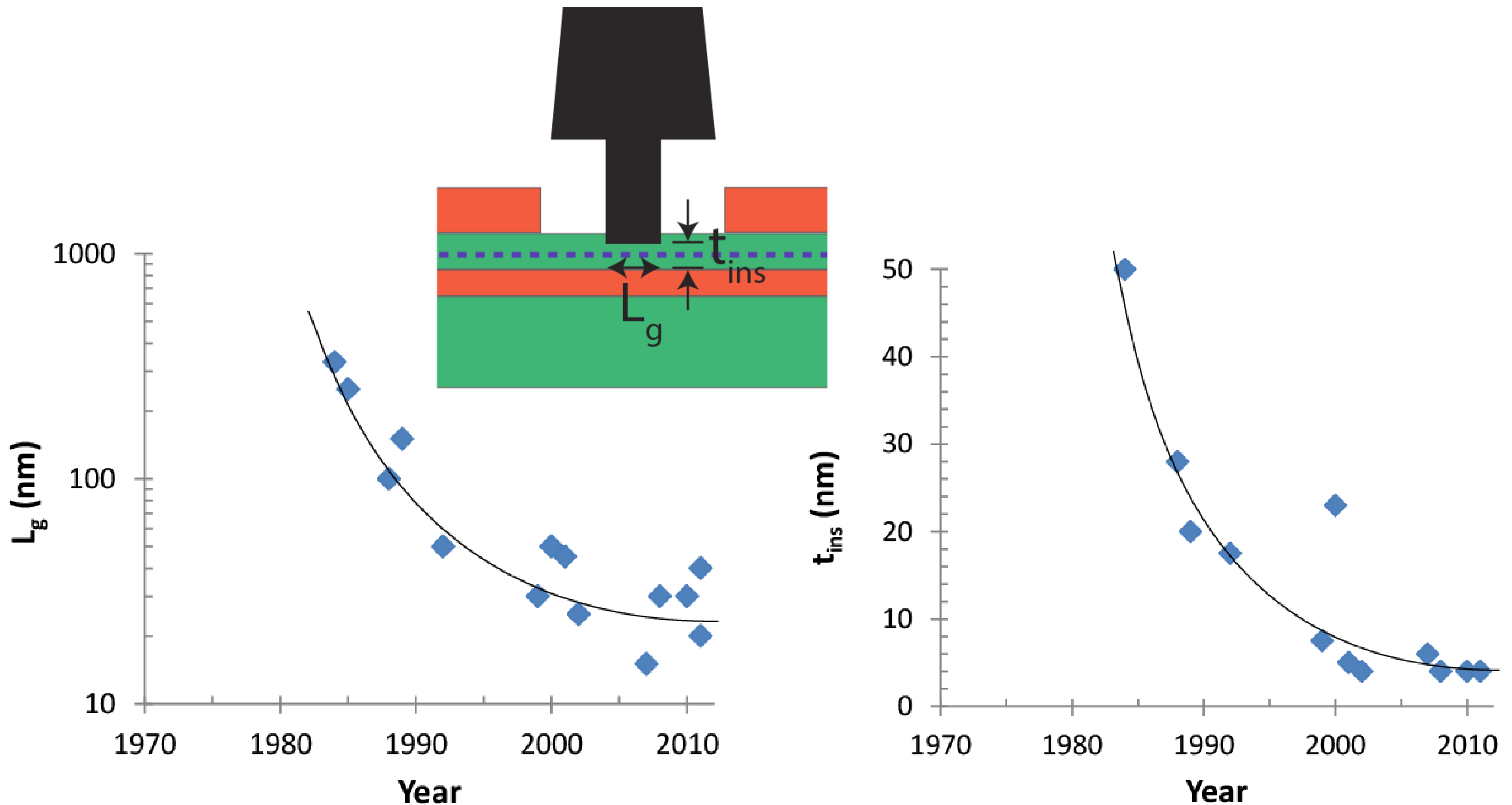
Full-sky map of Cosmic Microwave Background radiation (oldest light in Universe)
→ age of Universe: 13.73B years (±1%)



0.1 μm InGaAs HEMT LNA
Pospieszalski, MTT-S 2000

http://map.gsfc.nasa.gov/

Record f_T InGaAs HEMTs: megatrends



- Classic scaling trajectory: $L_g\downarrow$, $t_{ins}\downarrow$
- Recently: L_g, t_{ins} saturated → no more progress possible?

Limit to HEMT barrier scaling: gate leakage current

practical limit

InGaAs HEMTs

t_{ins} = 2 nm

t_{ins} = 4 nm

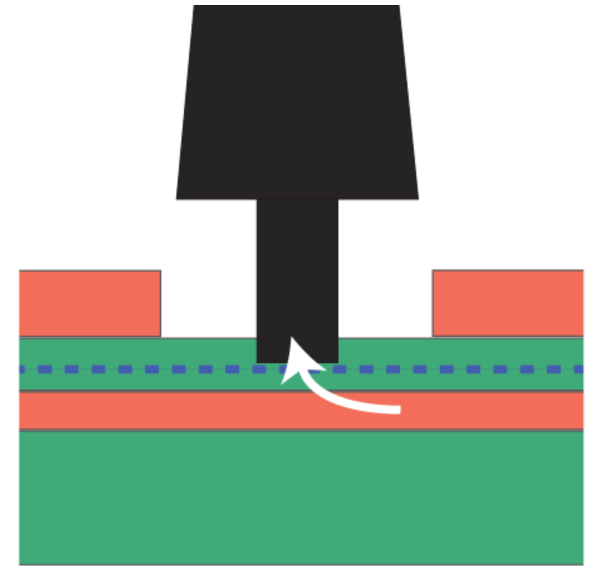
t_{ins} = 7 nm

t_{ins} = 10 nm

L_g=40 nm
V_{DS}=0.5 V

I_G [A/μm]: 10^{-4}, 10^{-6}, 10^{-8}, 10^{-10}, 10^{-12}, 10^{-14}

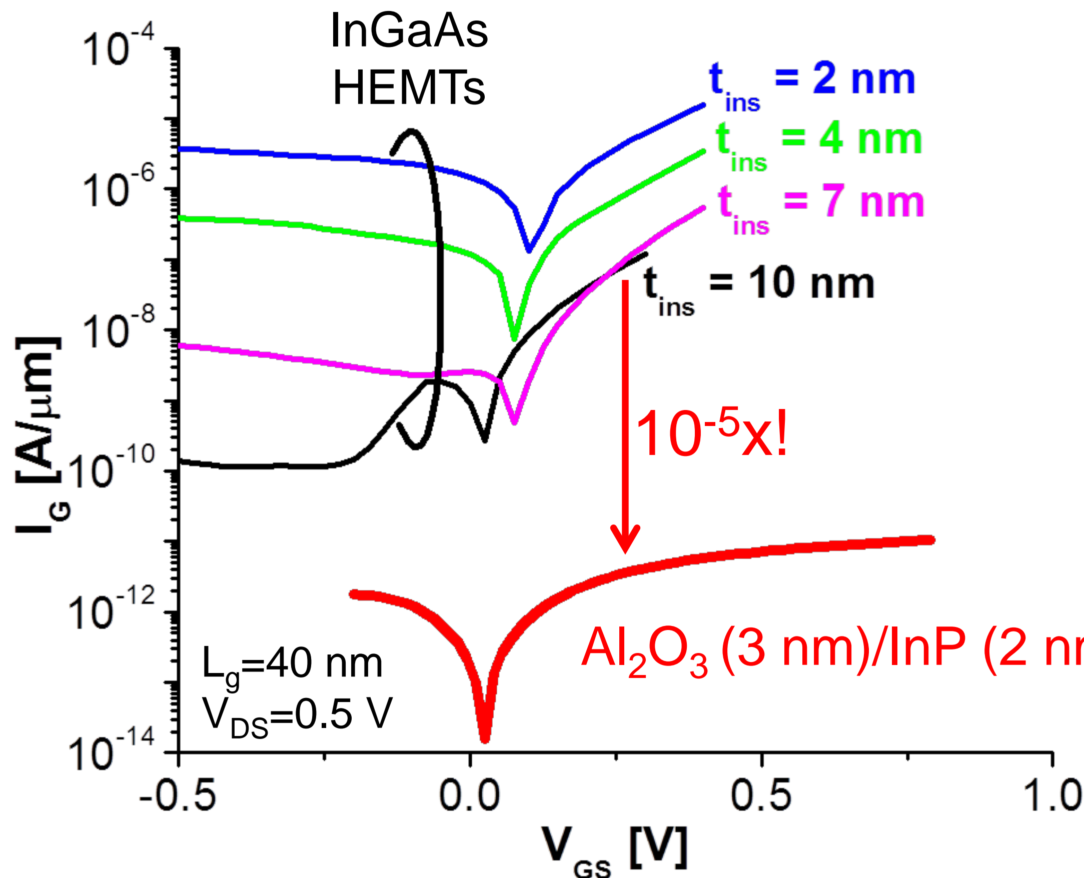
V_{GS} [V]: -0.5, 0.0, 0.5, 1.0

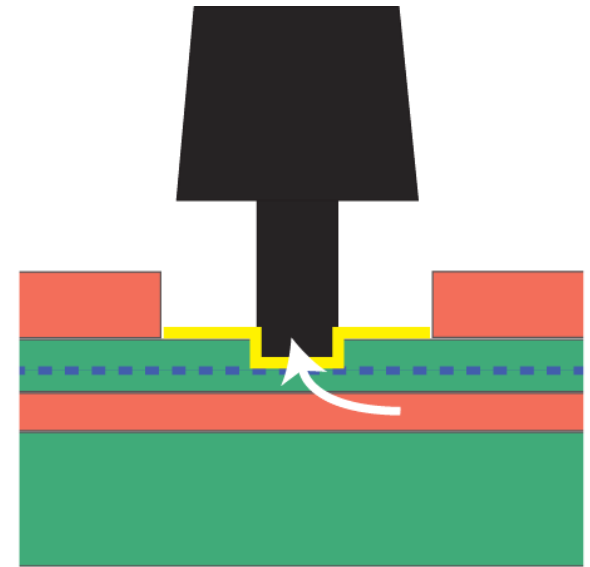


Kim, EDL 2013

At L_g=30-40 nm, modern HEMTs are at the limit of scaling!

Solution: introduce gate oxide!

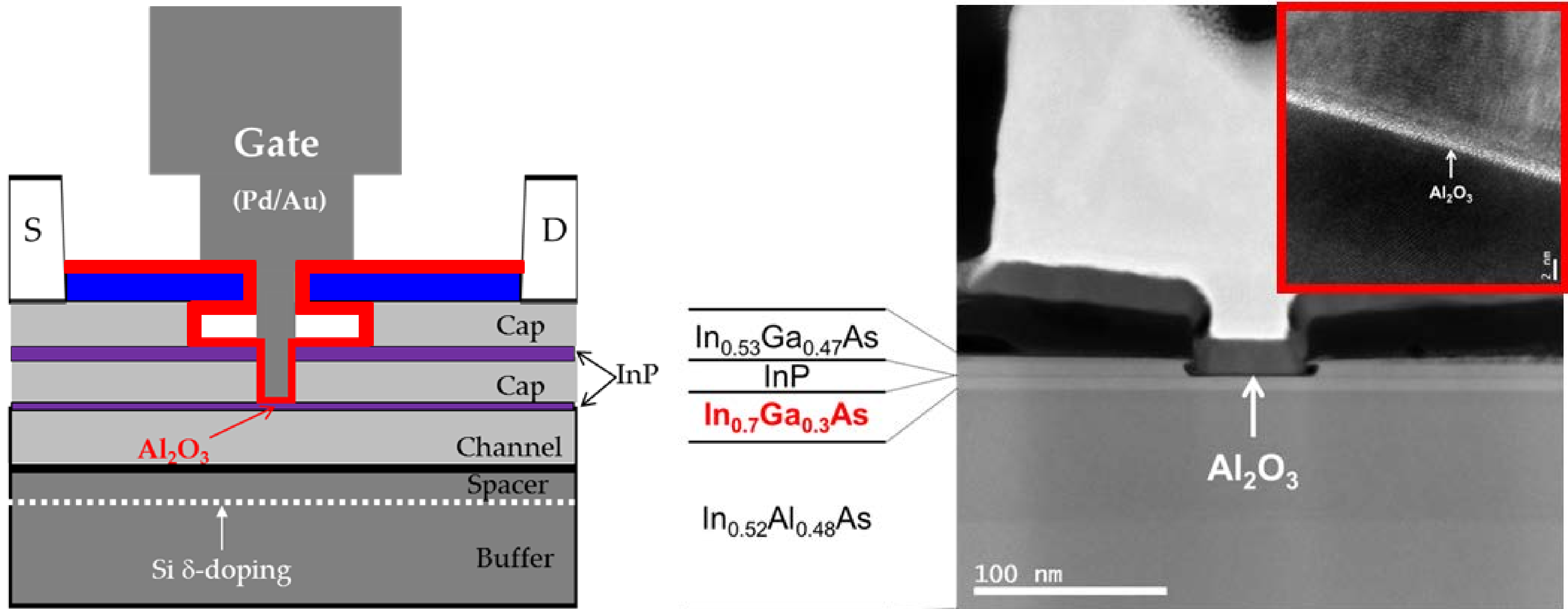




Kim, EDL 2013

Need high-K gate dielectric: **HEMT → MOSFET!**

InGaAs MOSFET with f_T=370 GHz

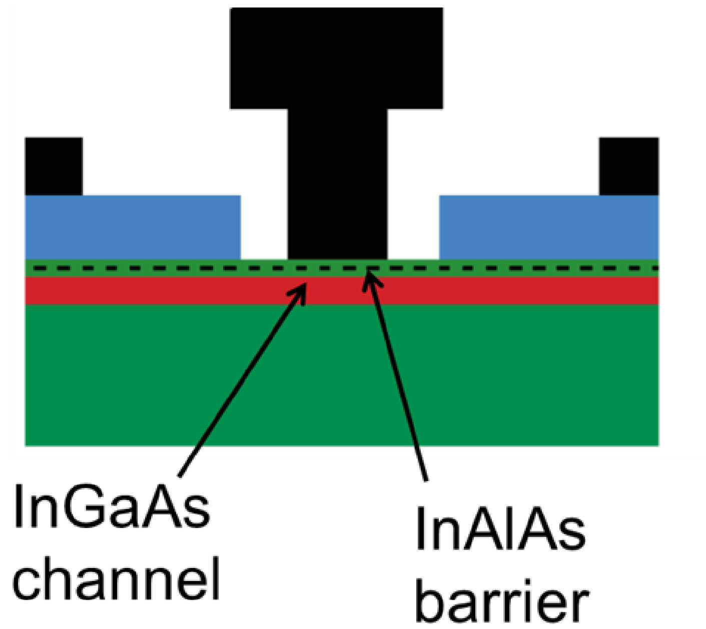


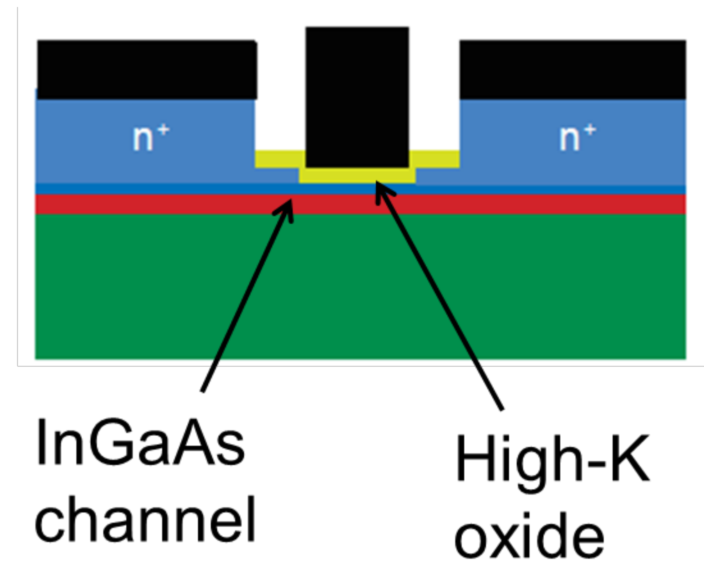
- Channel: 10 nm $In_{0.7}Ga_{0.3}As$
- Barrier: 1 nm InP + 2 nm Al_2O_3

- L_g = 60 nm
- f_T = 370 GHz
- g_m = 2 mS/μm

Kim, APL 2012

InGaAs HEMT vs. MOSFET

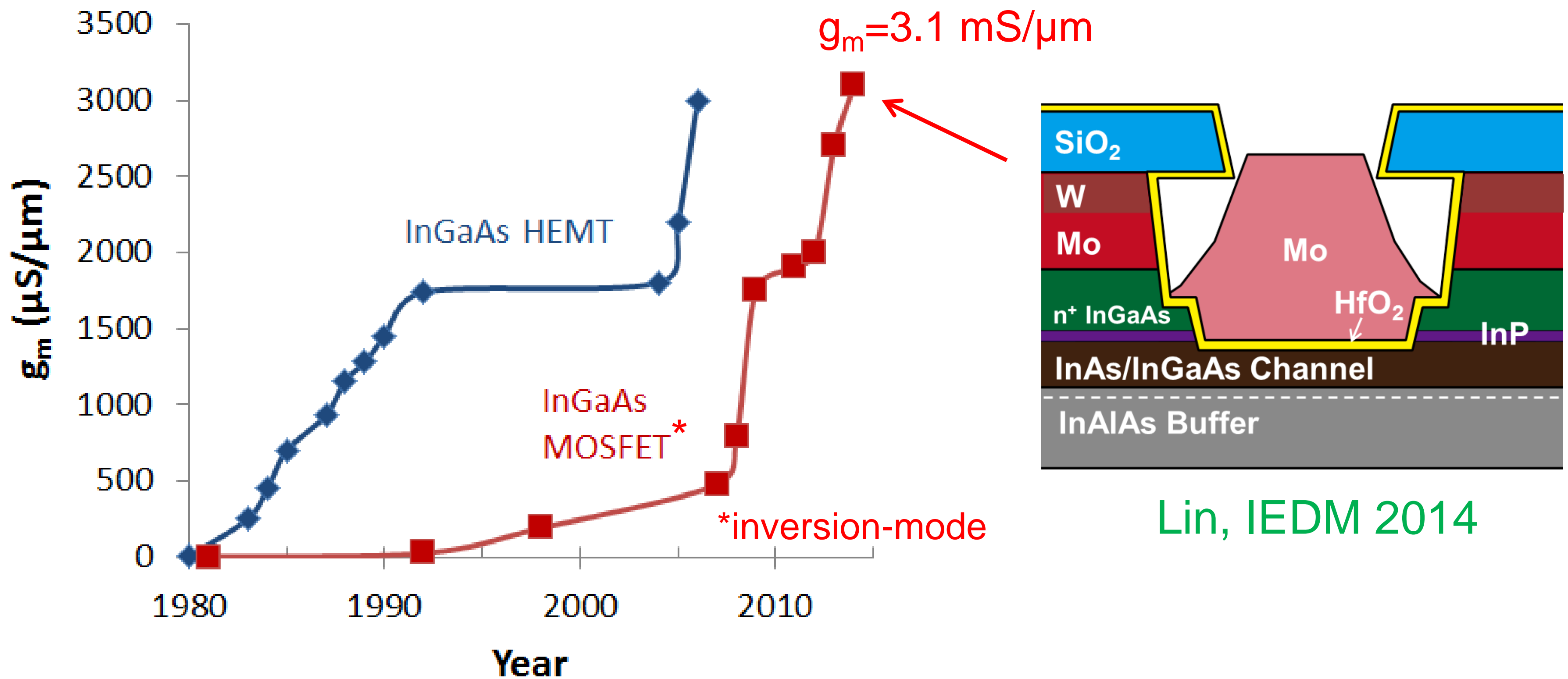




Since when can we make III-V MOSFETs?

Historical evolution: InGaAs MOSFETs vs. HEMTs

Transconductance (g_m):

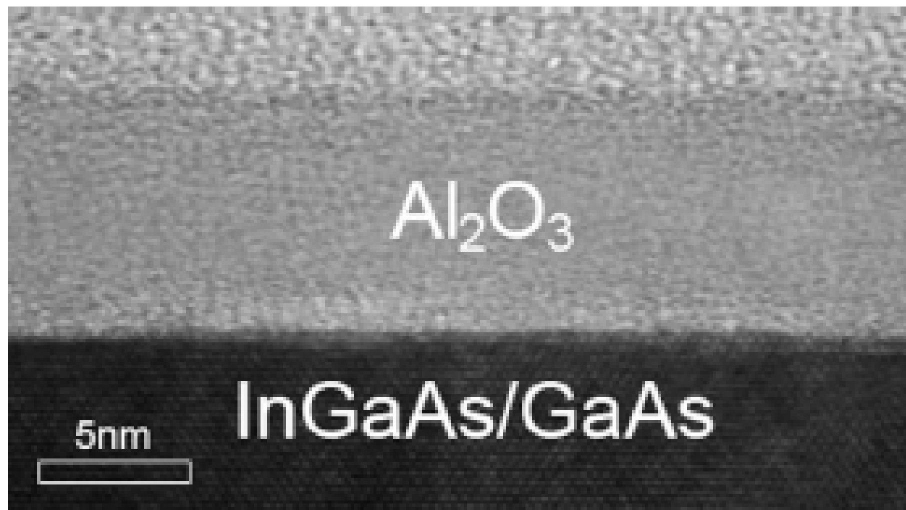


Recent progress due to improvement of oxide/III-V interface

What made the difference?
Atomic Layer Deposition (ALD) of oxide

ALD eliminates native oxides that pin Fermi level

→ "Self cleaning"

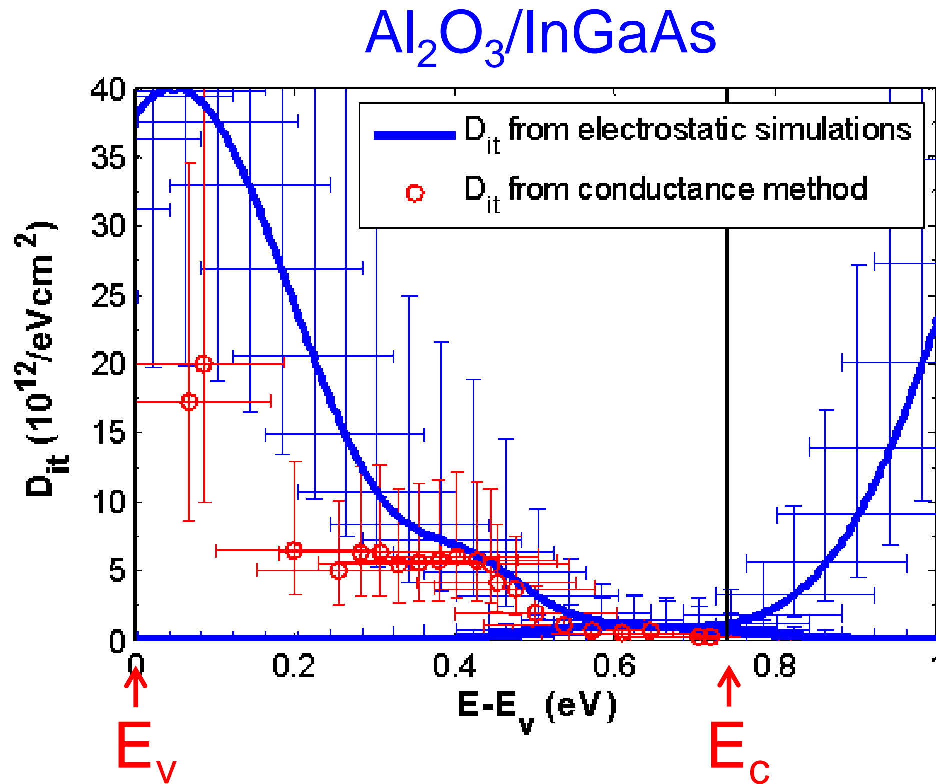


Huang, APL 2005

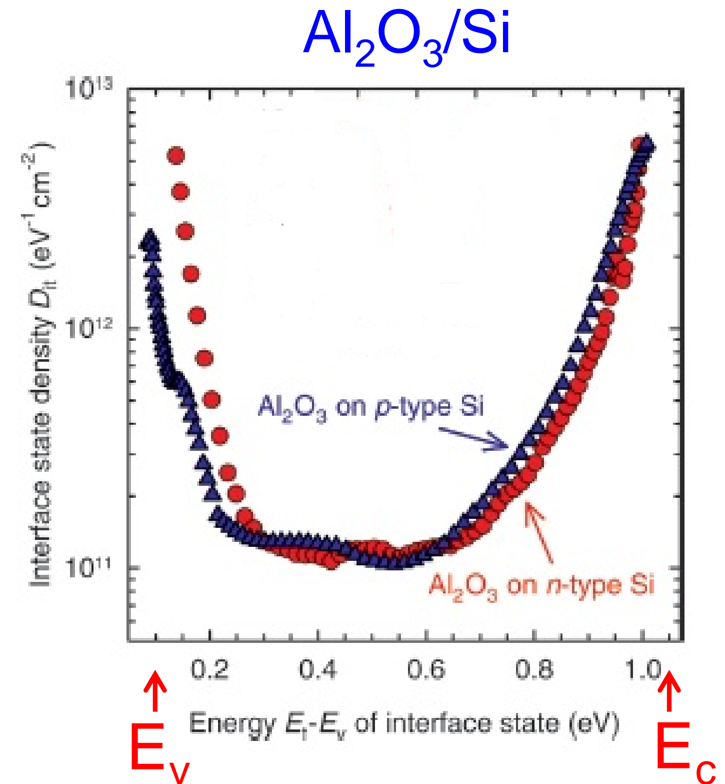
← Clean, smooth interface without native oxides

- First observed with Al_2O_3, then with other high-K dielectrics
- First seen in GaAs, then in other III-Vs

Interface quality: Al_2O_3/InGaAs vs. Al_2O_3/Si



Brammertz, APL 2009

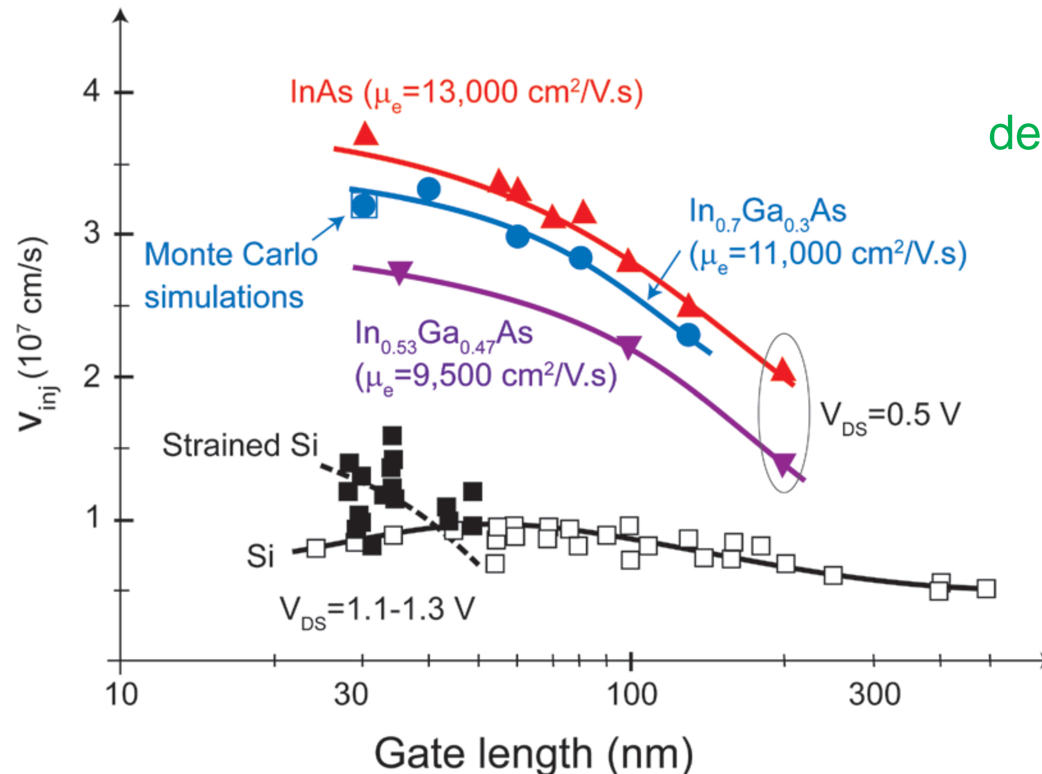


Werner, JAP 2011

Close to E_c, Al_2O_3/InGaAs comparable D_{it} to Al_2O_3/Si interface

Electron velocity: InGaAs vs. Si

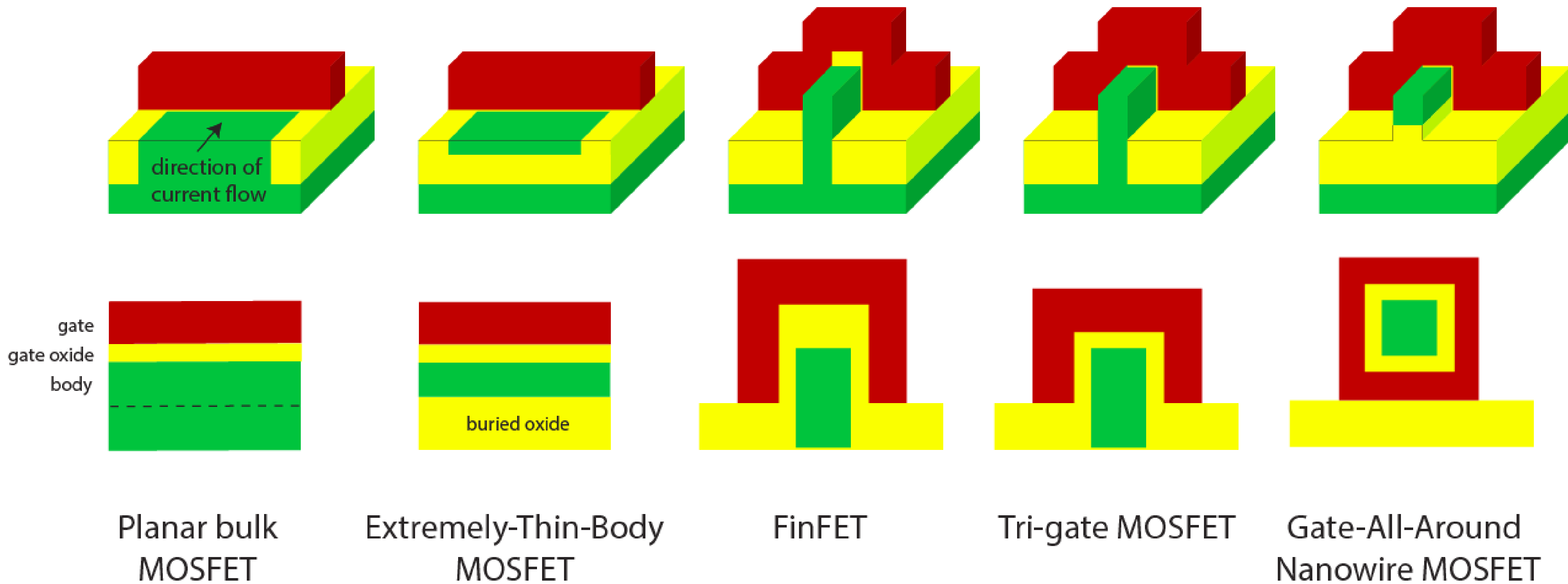
Measurements of electron injection velocity in HEMTs:



del Alamo, Nature 2011

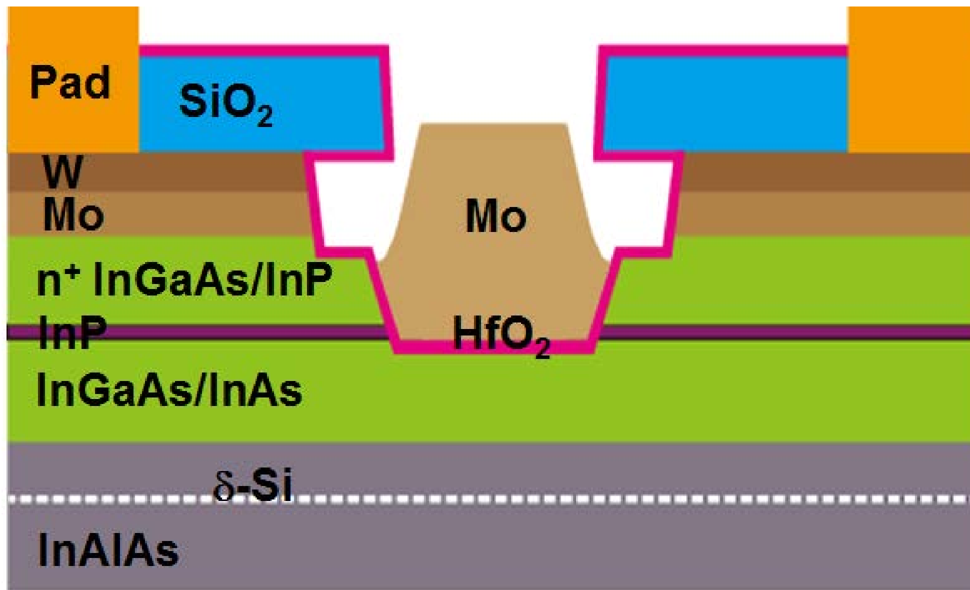
- v_{inj}(InGaAs) increases with InAs fraction in channel
- v_{inj}(InGaAs) > $2v_{inj}$(Si) at less than half V_{DD}
- ~100% ballistic transport at L_g~30 nm

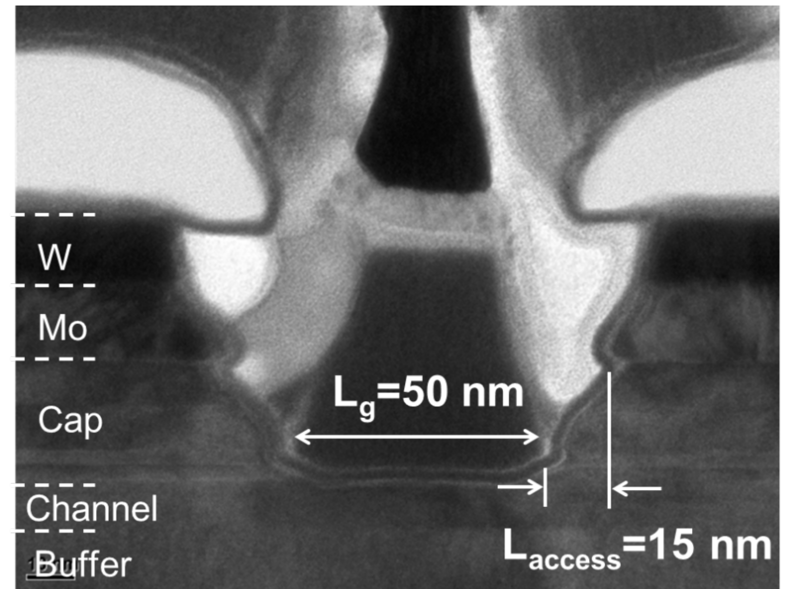
Logic InGaAs MOSFET: possible designs



Enhanced gate control → enhanced scalability

Self-aligned Planar InGaAs MOSFETs





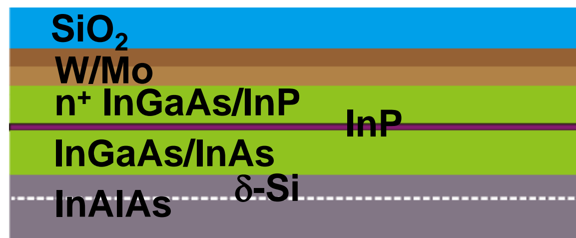
Lin, IEDM 2012, 2013, 2014

Recess-gate process:

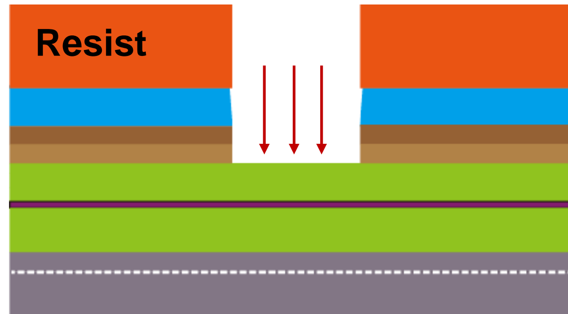
- CMOS-compatible
- Refractory ohmic contacts (W/Mo)
- Extensive use of RIE

Fabrication process

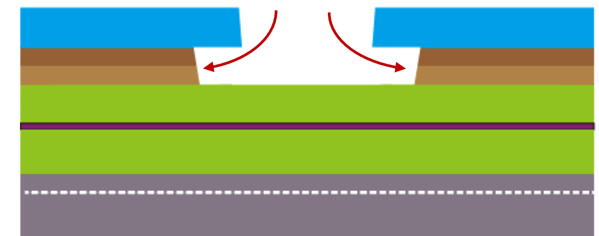
Mo/W ohmic contact
+ SiO_2 hardmask



SF_6, CF_4 anisotropic RIE

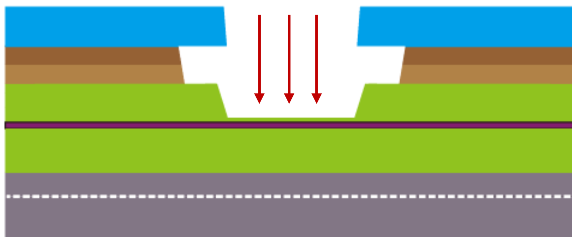


CF_4:O_2 isotropic RIE



Waldron, IEDM 2007

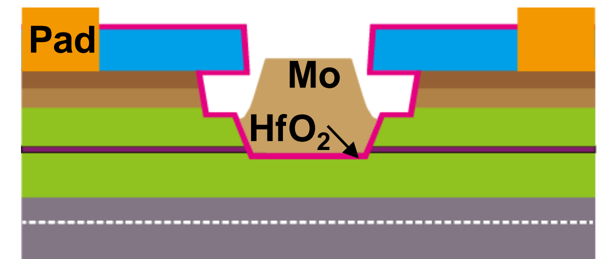
Cl_2:N_2 anisotropic RIE



Digital etch

O_2 plasma diluted H_2SO_4

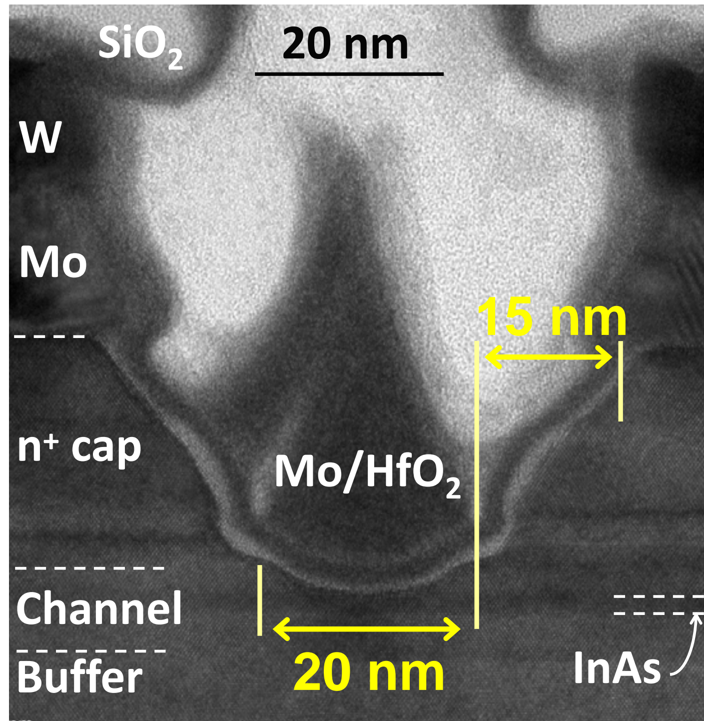
Gate stack and pads

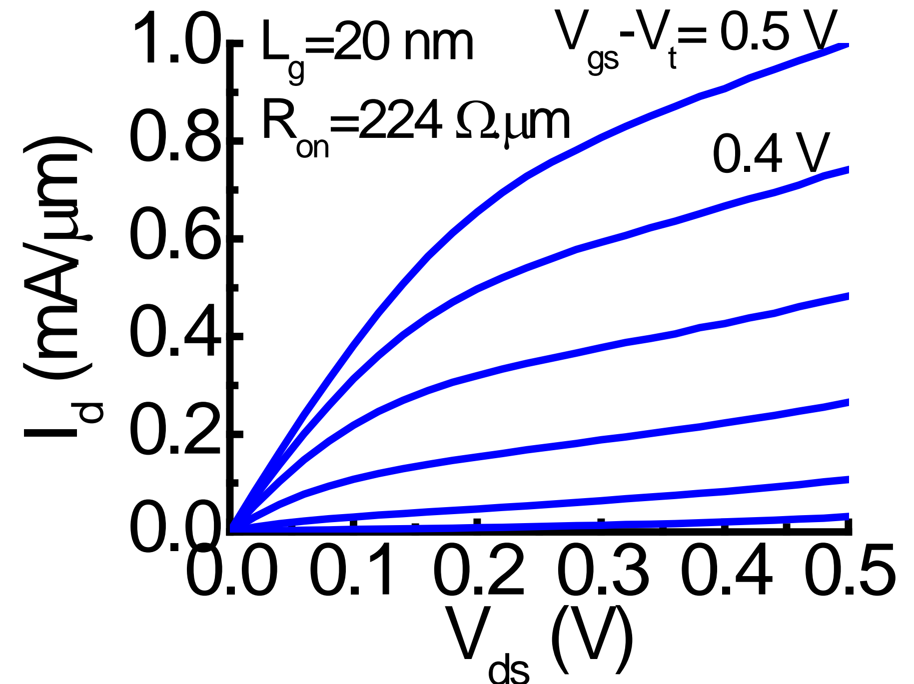


Lin, EDL 2014

- Ohmic contact first, gate last
- Precise control of vertical (~1 nm), lateral (~5 nm) dimensions
- MOS interface exposed late in process

L_g=20 nm InGaAs MOSFET





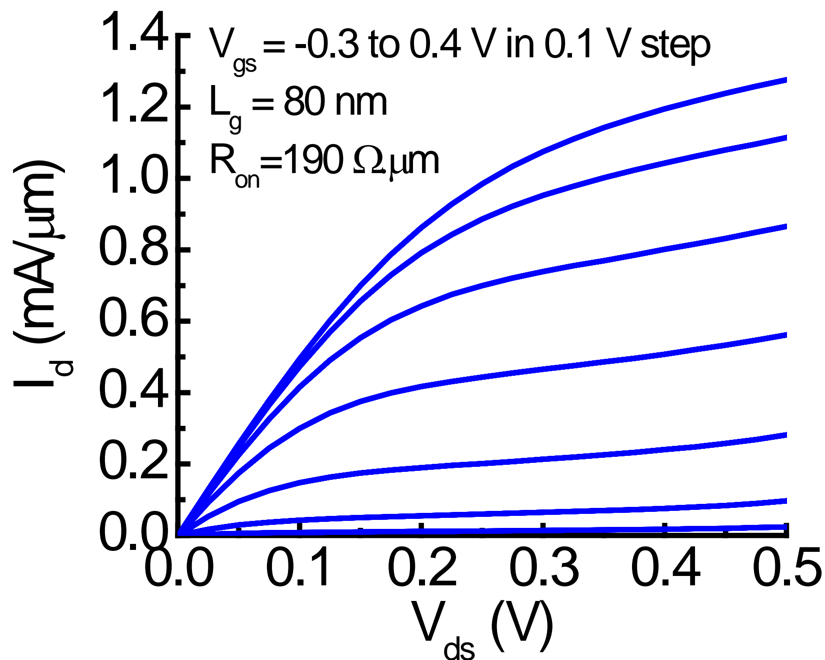
L_g = 20 nm, L_{access}= 15 nm MOSFET

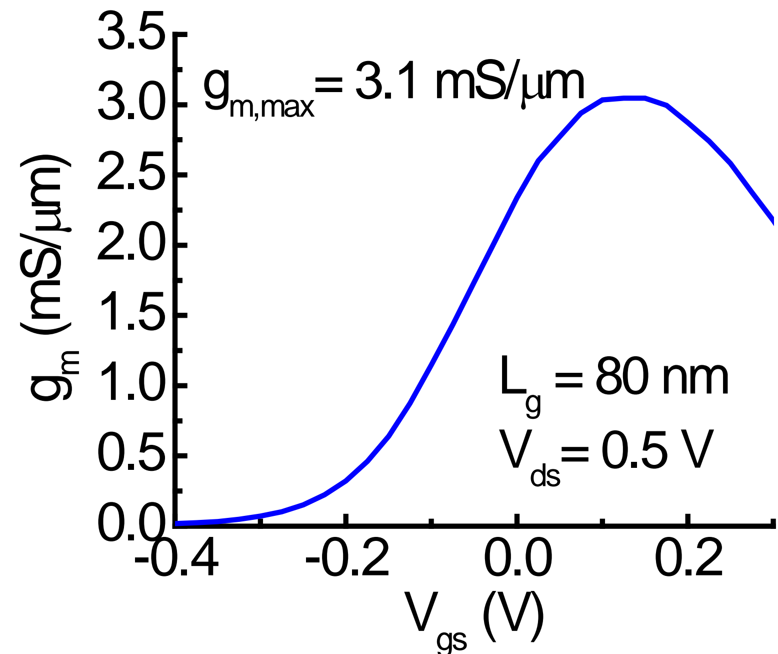
→ tightest III-V MOSFET ever made?

Lin, IEDM 2013

Highest performance InGaAs MOSFET

L_g =80 nm, EOT=0.5 nm (2.5 nm HfO_2), t_c=9 nm, L_{access}=15 nm



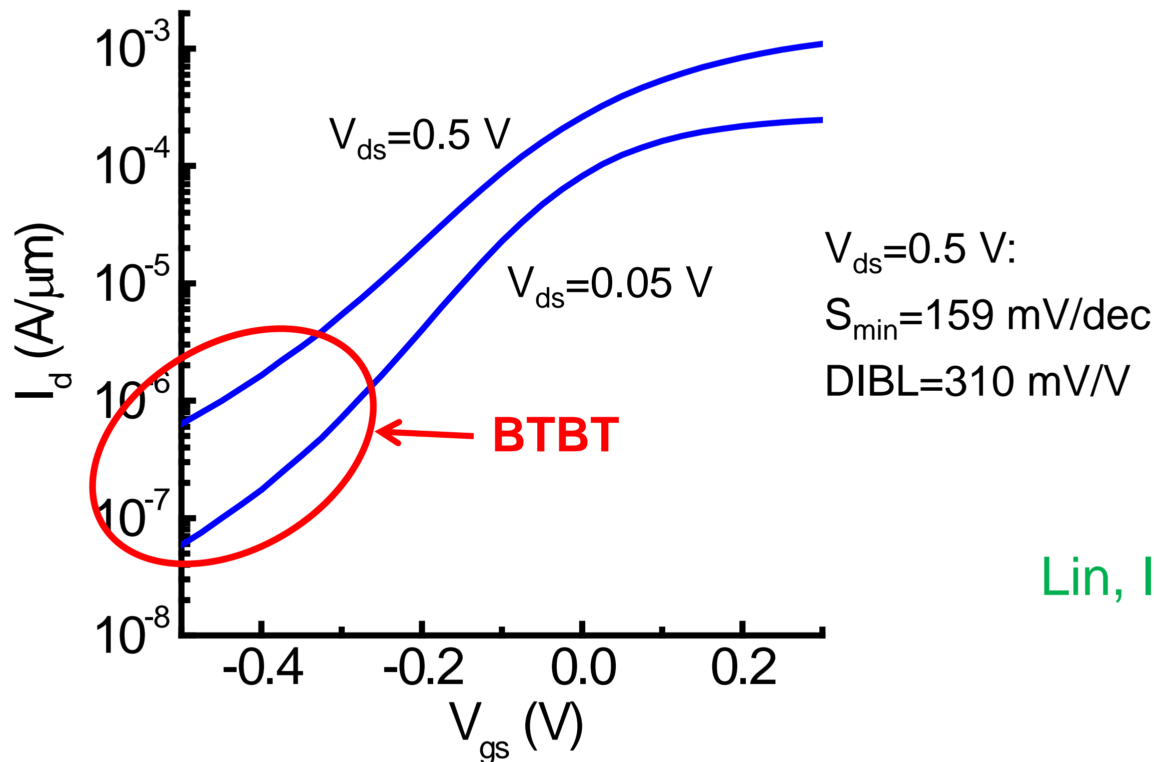


- Record $g_{m,max}$ = 3.1 mS/μm at V_{ds}= 0.5 V
- R_{on} = 190 Ω.μm

Lin, IEDM 2014

Subthreshold characteristics

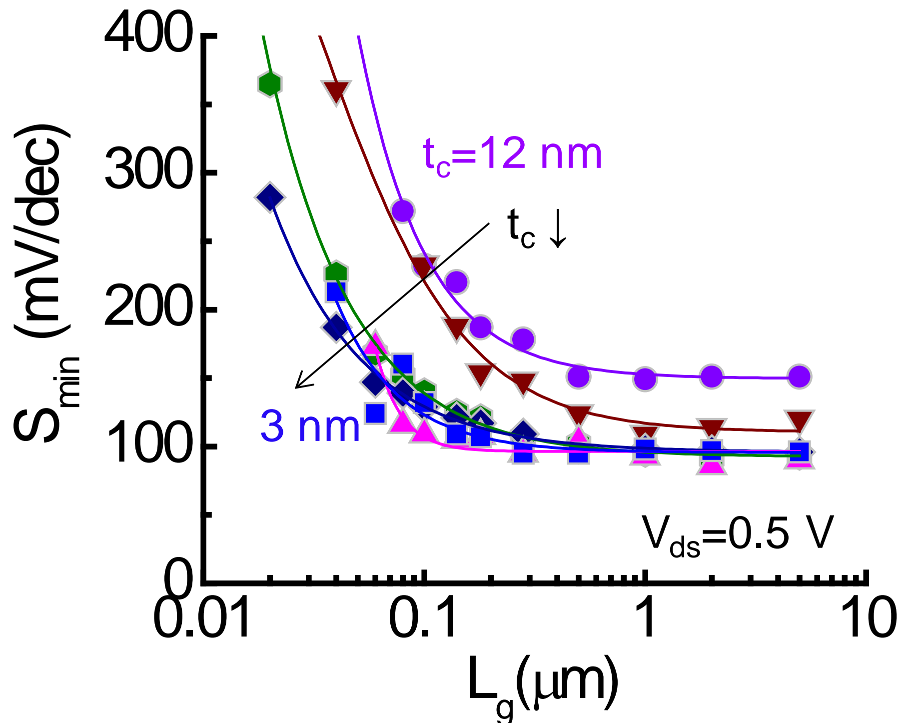
L_g =80 nm, EOT=0.5 nm (2.5 nm HfO_2), t_c=9 nm, L_{access}=15 nm

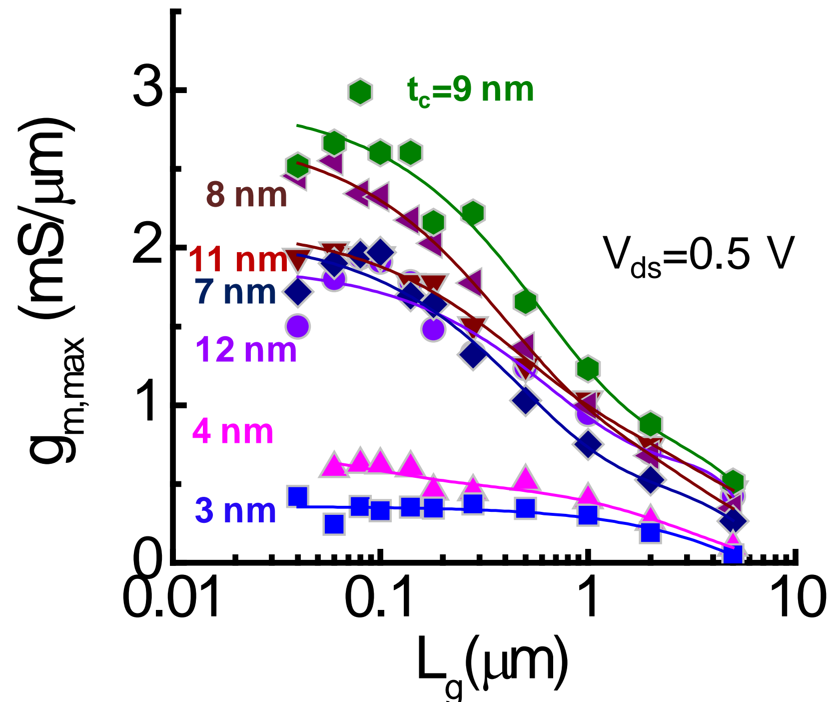


- Modest subthreshold swing, DIBL → explore channel thickness scaling
- Excess OFF current at V_{ds}=0.5 V → Band-to-Band Tunneling (BTBT)

Impact of channel thickness scaling

Lin, IEDM 2014



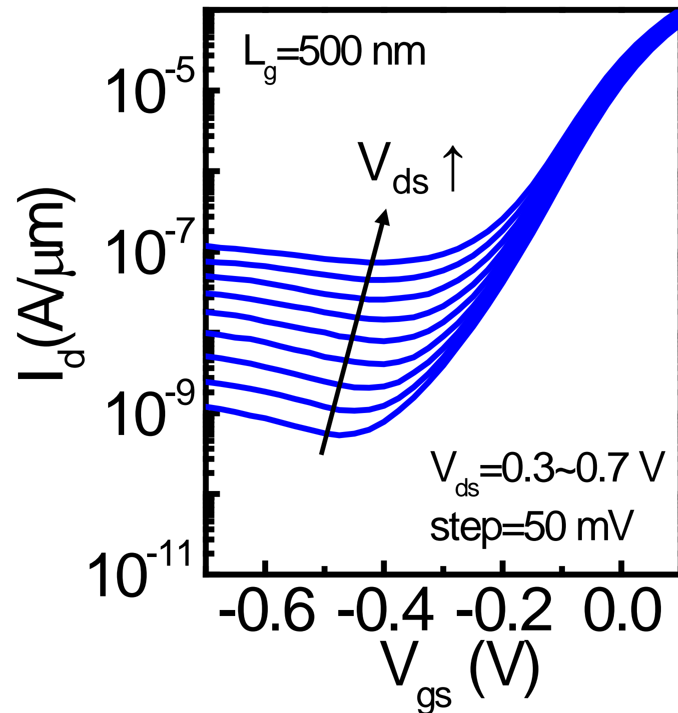


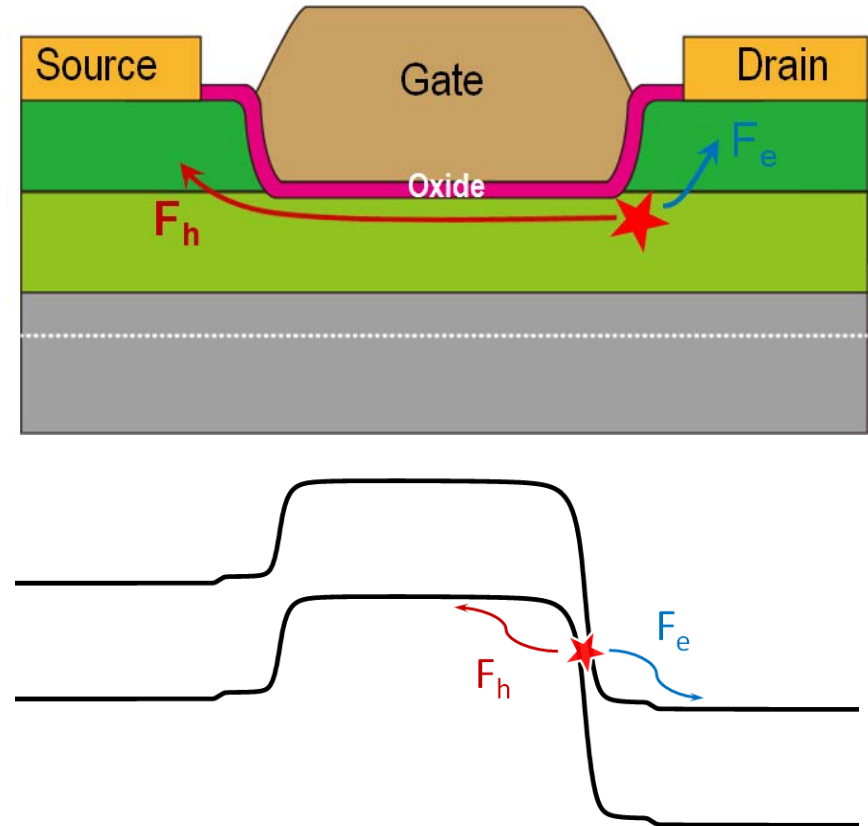
- t_c ↓ → S ↓ but also $g_{m,max}$ ↓
- Even at t_c=3 nm, $L_{g,min}$~40 nm

  → planar MOSFET at limit of scaling

Excess OFF-state current

Transistor fails to turn off:



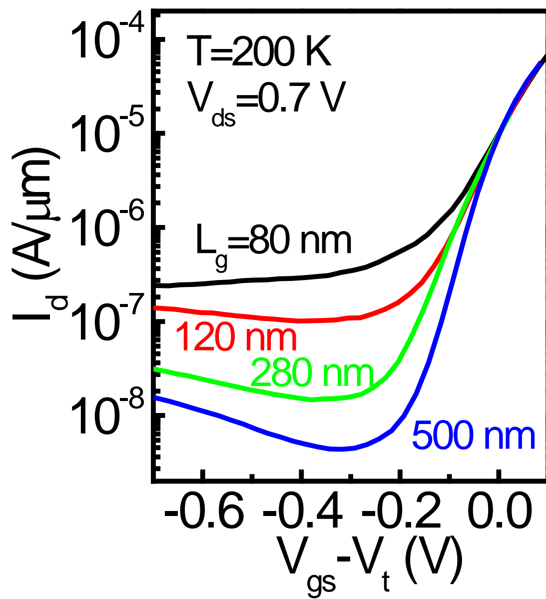


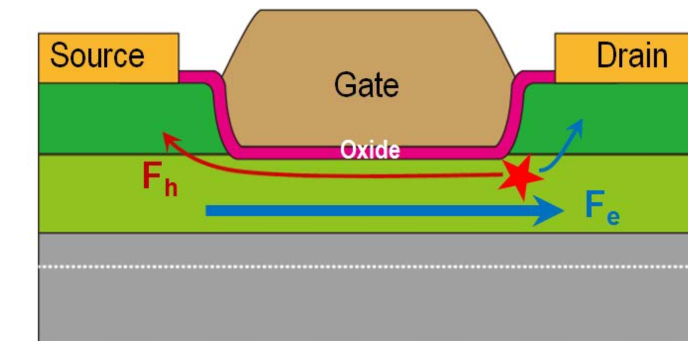
OFF-state current enhanced with V_{ds}

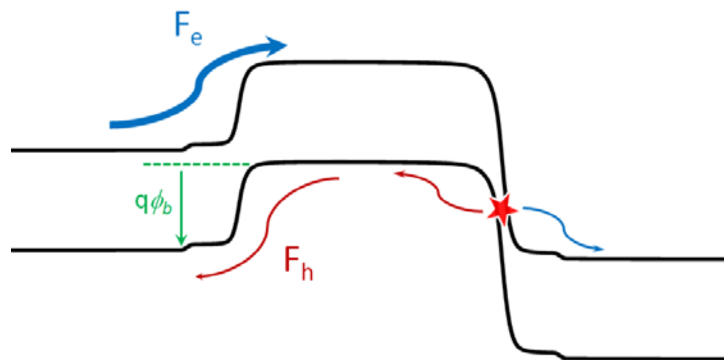
→ *Band-to-Band Tunneling (BTBT) or Gate-Induced Drain Leakage (GIDL)*

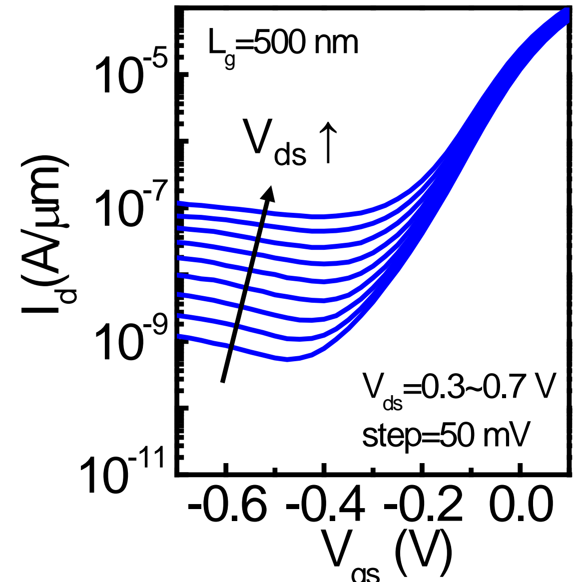
Lin, IEDM 2013

Excess OFF-state current

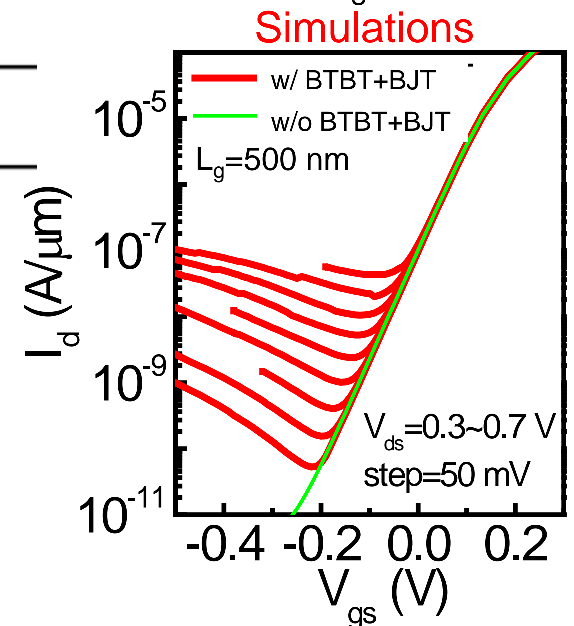








Simulations

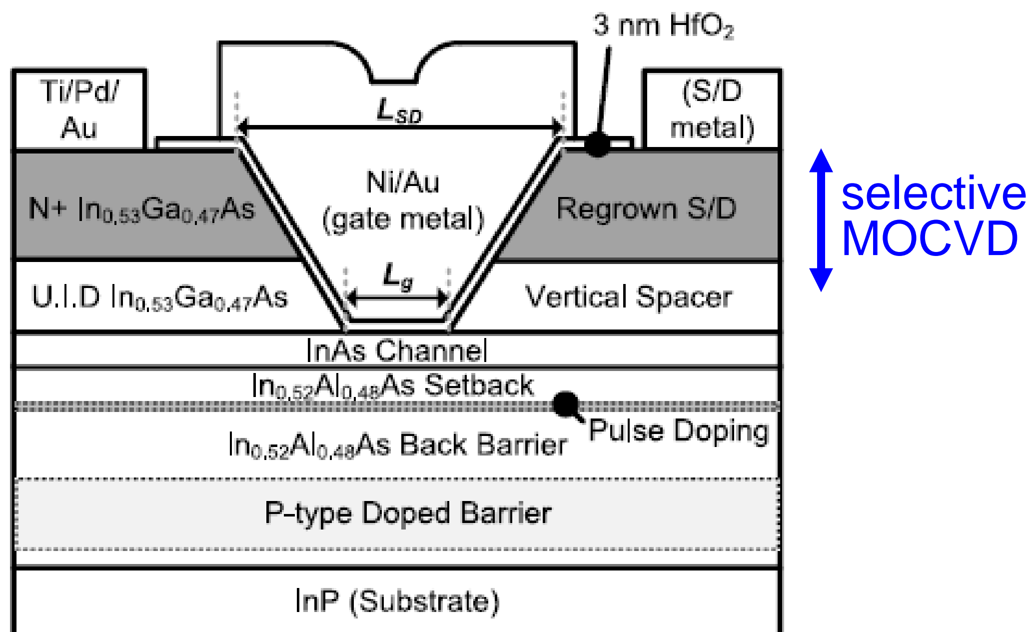


Lin, EDL 2014

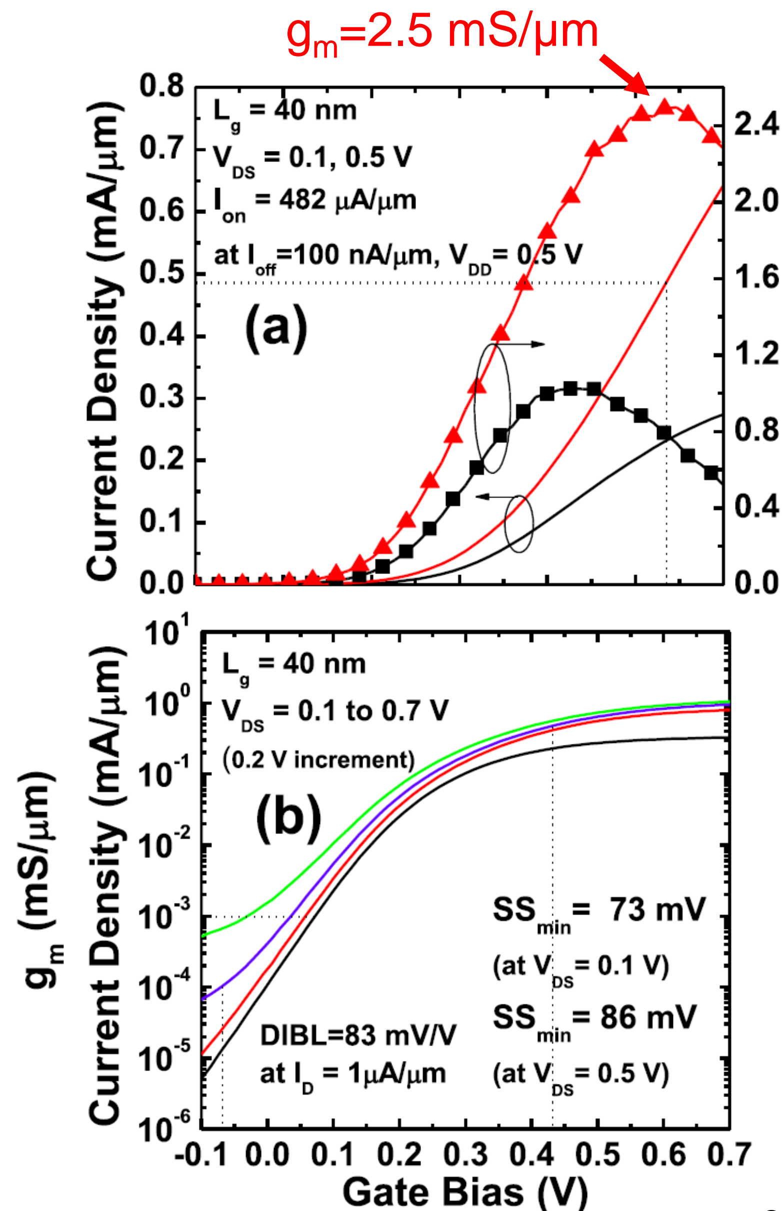
L_g↓ → OFF-state current ↑

→ additional *bipolar gain effect due to floating body*

Planar Regrown-contact InGaAs MOSFET



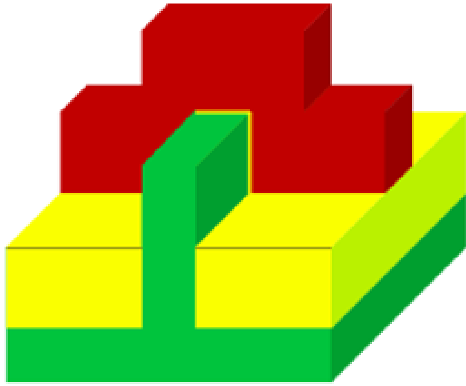
Lee, EDL 2014



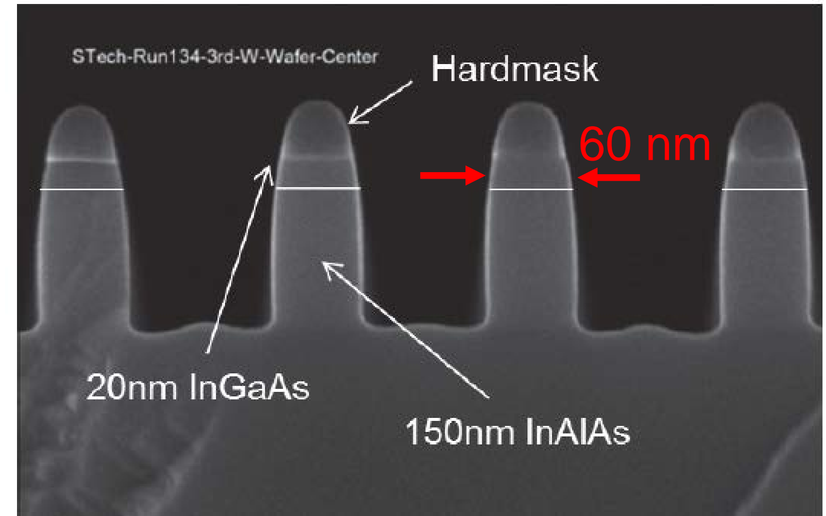
Regrown contact MOSFET:

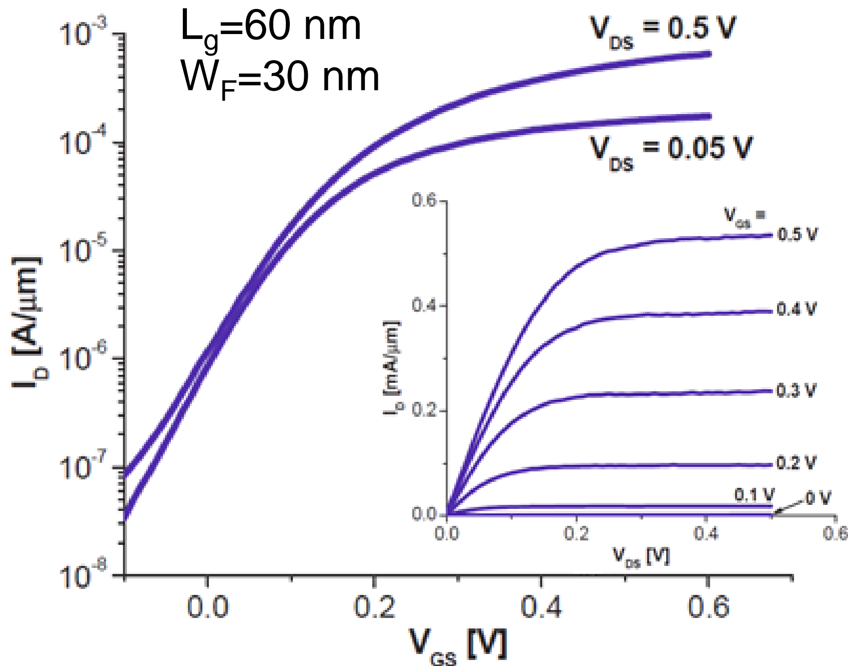
- Avoids RIE in intrinsic region
- Contacts self-aligned to dummy gate

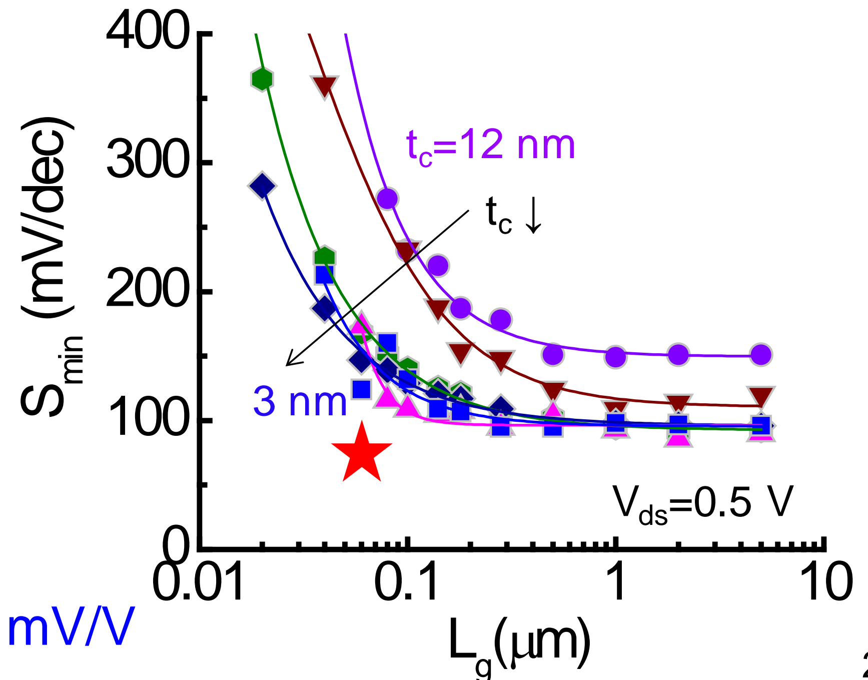
InGaAs Trigate MOSFET



Kim, IEDM 2013

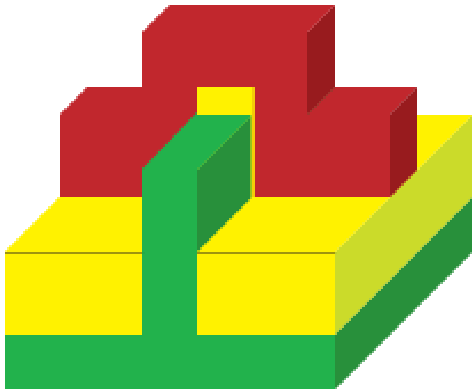


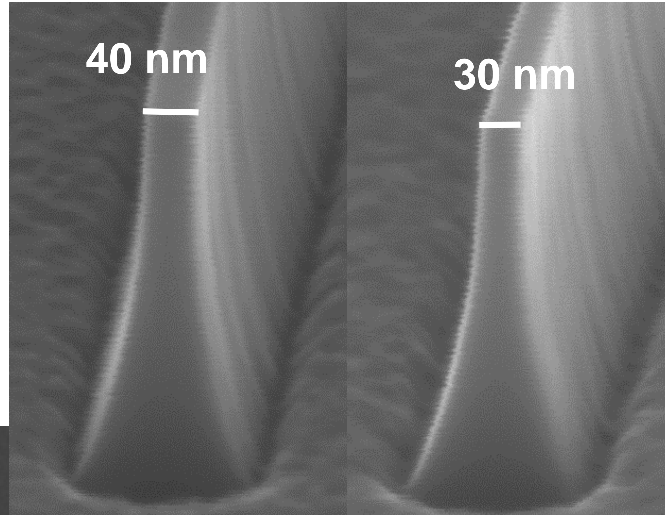


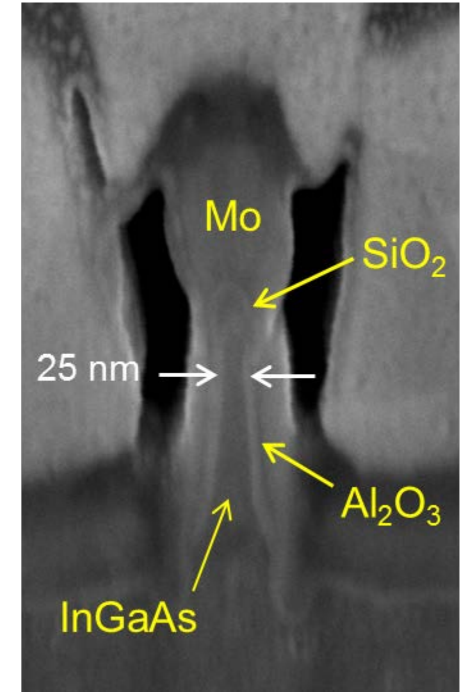


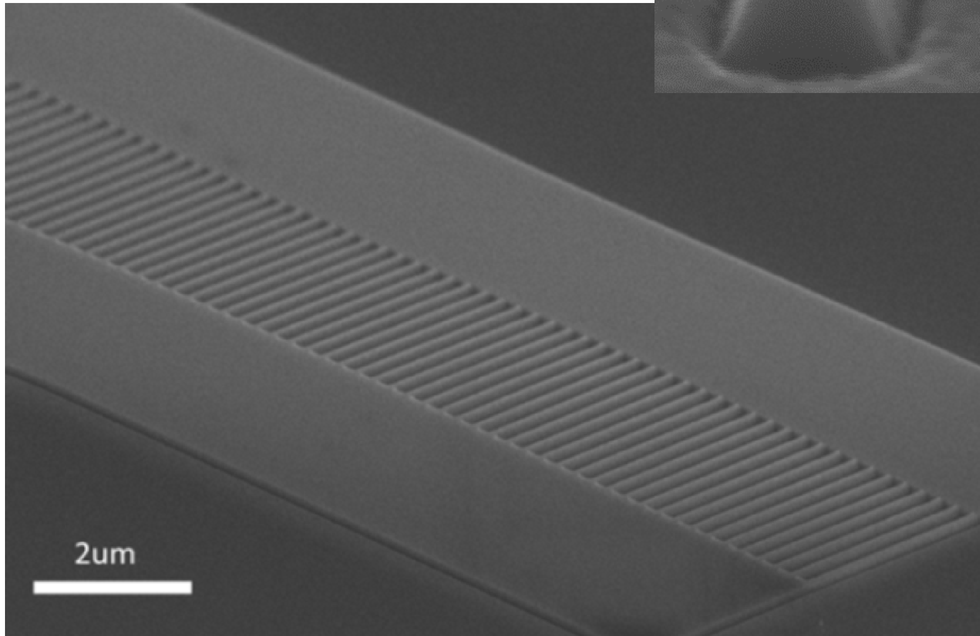
g_m=1.5 mS/μm, S=77 mV/dec, DIBL=10 mV/V

InGaAs double-gate MOSFET









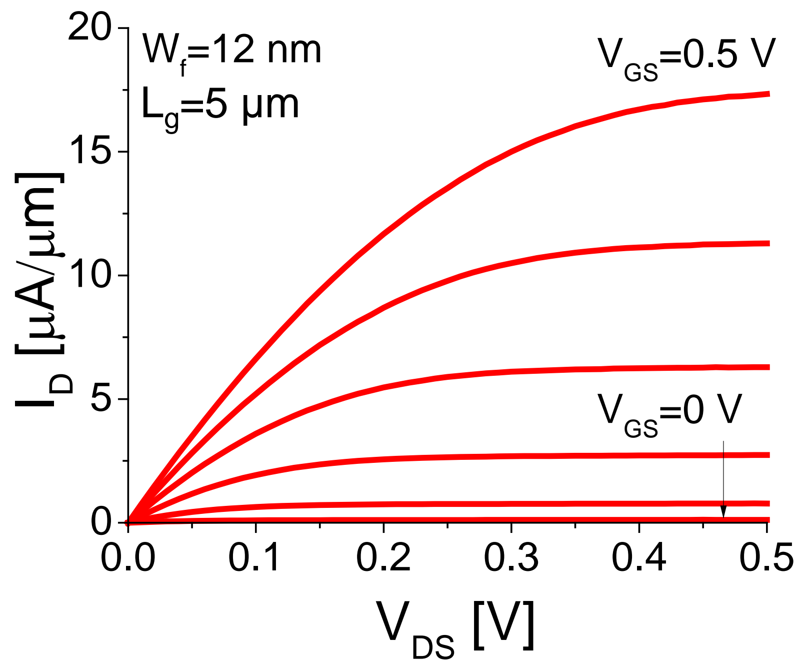
Key enabling technologies:

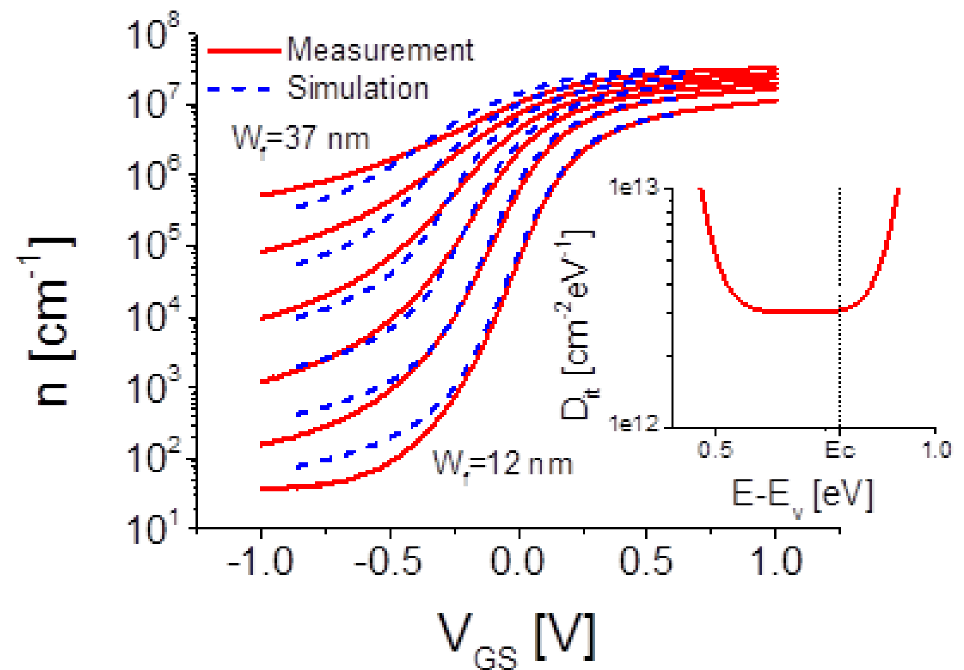
- $BCl_3/SiCl_4/Ar$ RIE
- digital etch

Zhao, EDL 2014; Vardi, DRC 2014

InGaAs double-gate MOSFET

Long-channel MOSFET characteristics (W_f=12~37 nm):

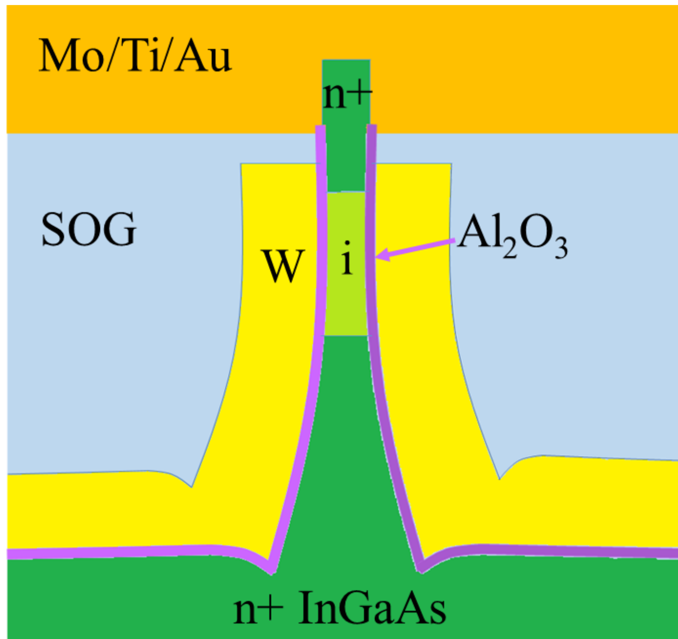




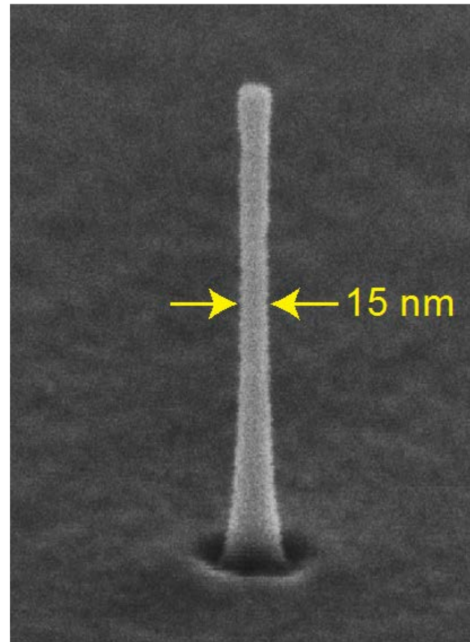
At sidewall: $D_{it,min}$ ~ $3x10^{12}$ $eV^{-1}.cm^{-2}$

Vardi, DRC 2014

Vertical nanowire InGaAs MOSFET

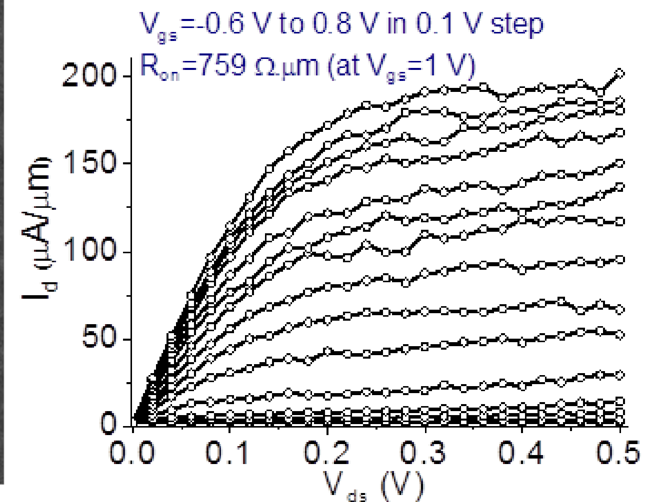


Zhao, IEDM 2013



Zhao, EDL 2014

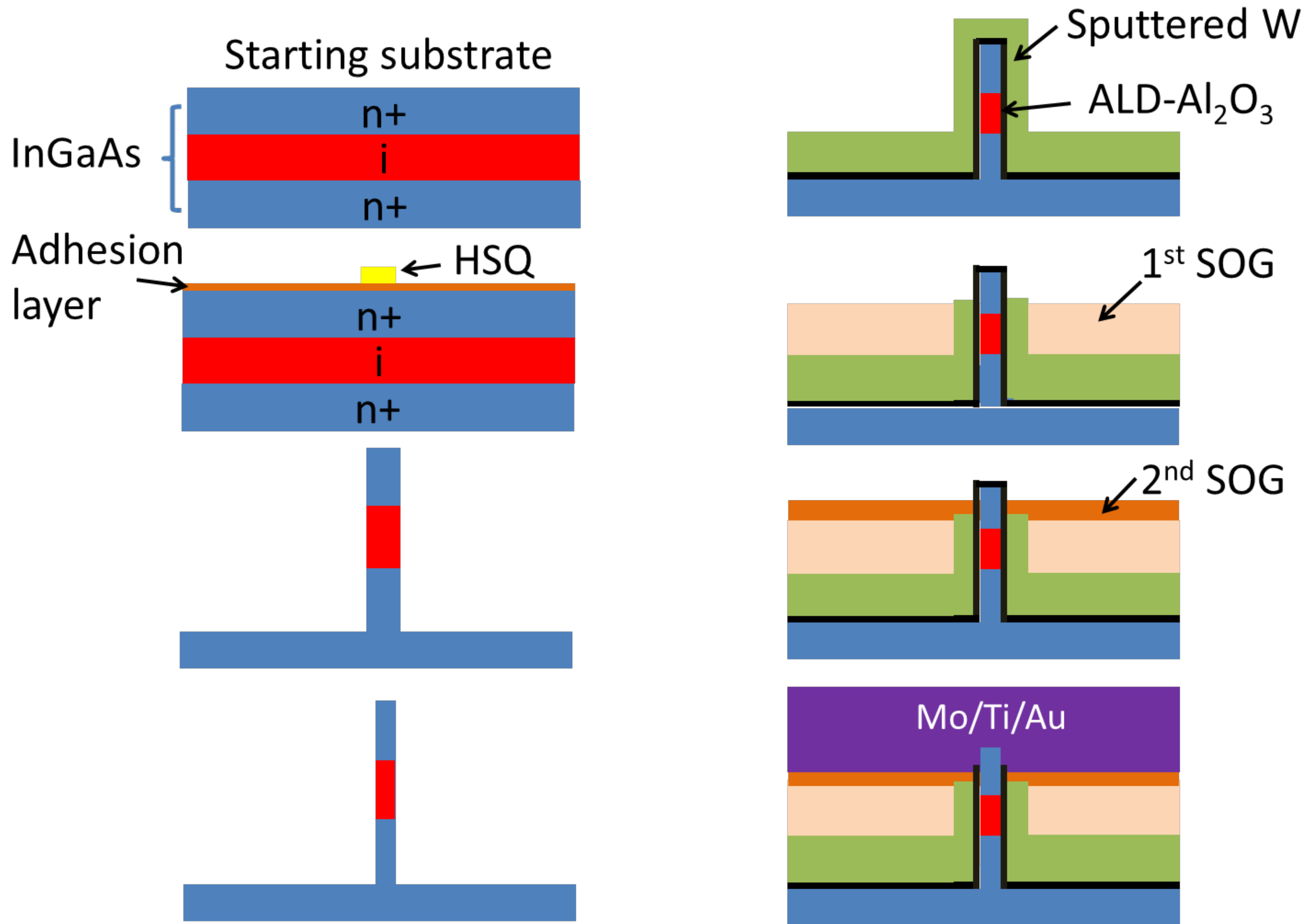
30 nm diameter
InGaAs NW-MOSFET



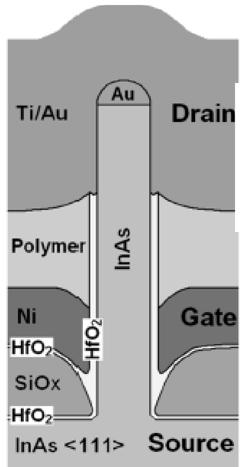
- Nanowire MOSFET: ultimate scalable transistor
- Vertical NW: uncouples footprint scaling from L_g scaling
- Top-down approach based on RIE + digital etch

Tomioka, Nature 2012
Persson, DRC 2012

Process flow

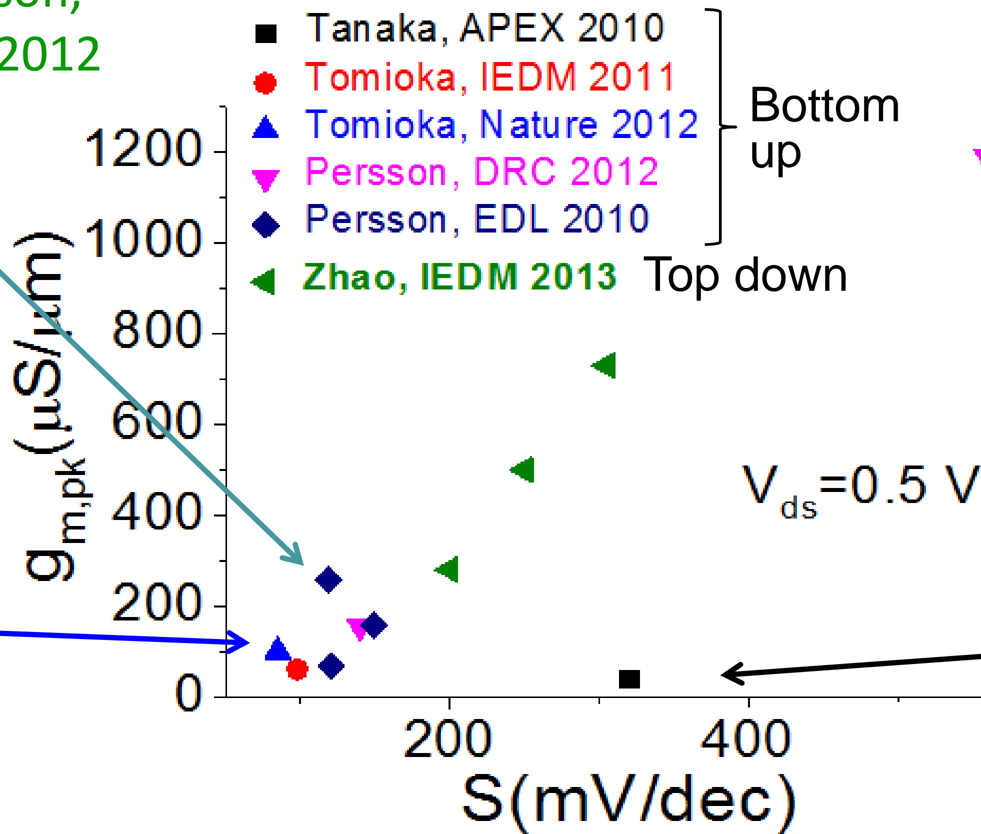


Trade-off between transport and short-channel effects

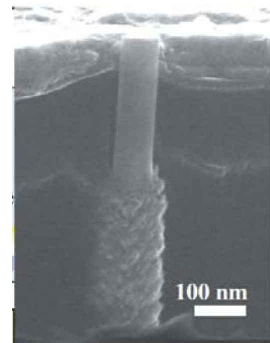


Persson, EDL 2012

Tomioka, Nature 2012



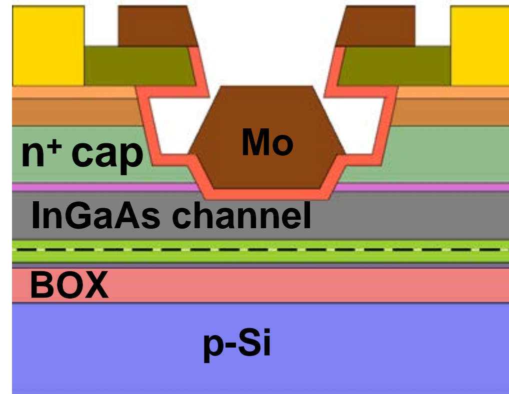
Persson, DRC 2012

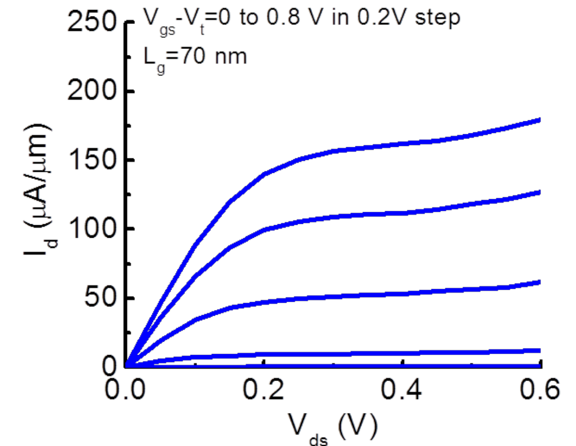


Tanaka, APEX 2010

D↓ → S↓ but also g_m↓

Si integration:
SOI-like InGaAs planar MOSFETs





III-V bonded SOI process:

Czornomaz, IEDM 2012

Lin, DRC 2014

InGaAs channel

n^+ cap

InP donor wafer

BOX: Al_2O_3

InP donor wafer

InP donor wafer

BOX

p-Si

BOX

p-Si

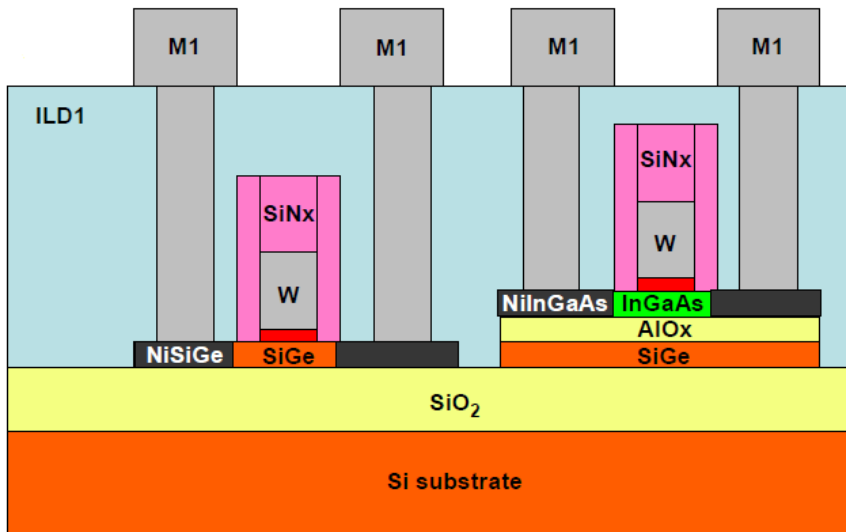
1. MBE growth

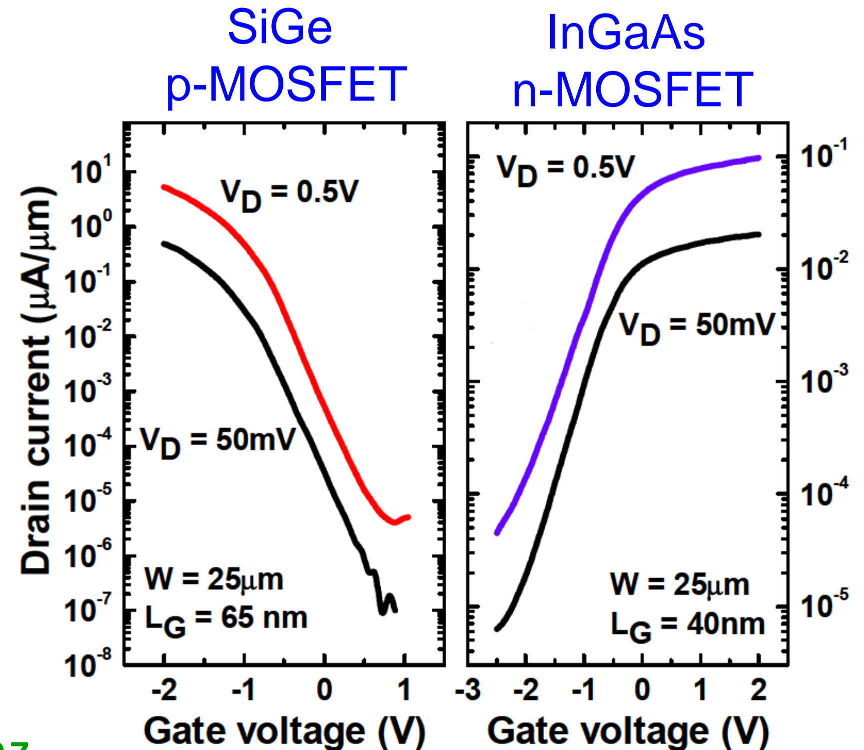
2. ALD Al_2O_3

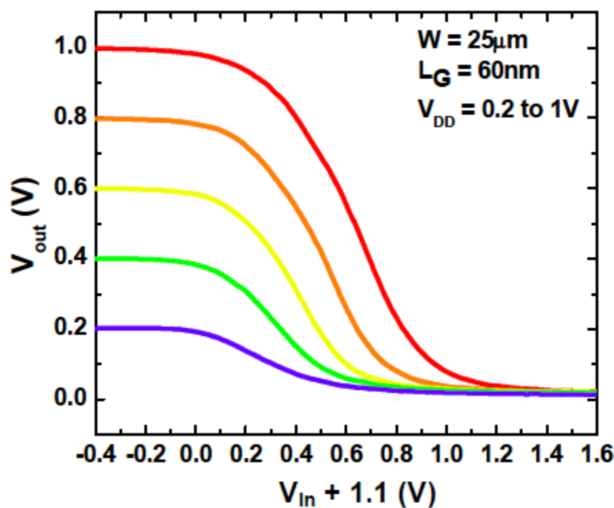
3. Wafer bonding

4. InP etch back

Si integration: SOI-like InGaAs planar MOSFETs

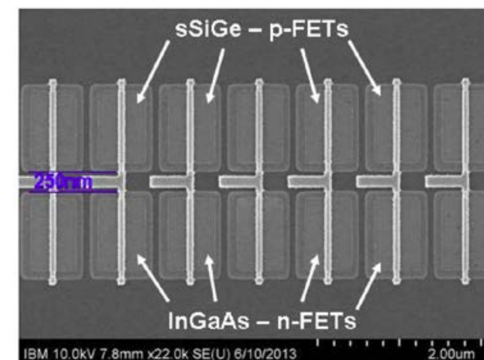




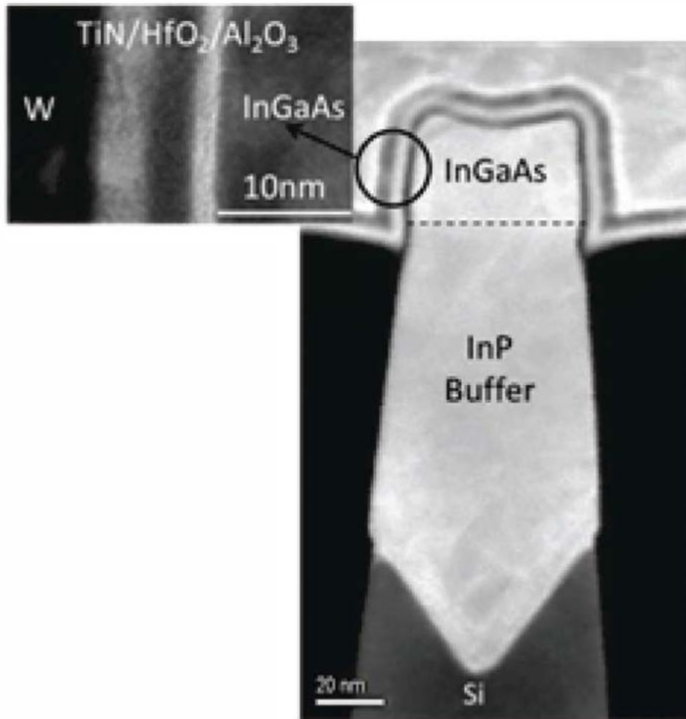


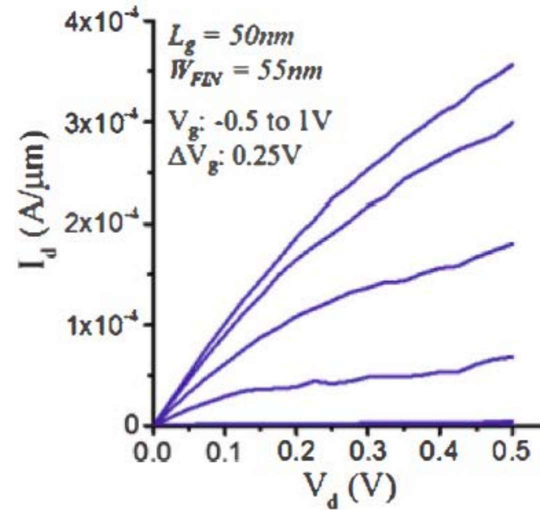
Czornomaz, IEDM 2013

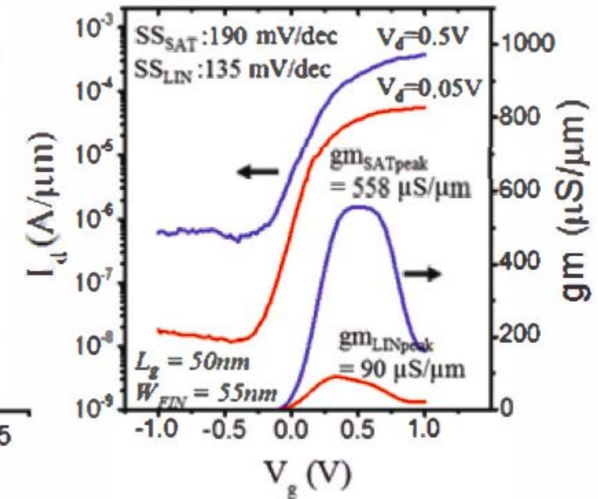
CMOS inverter transfer characteristics



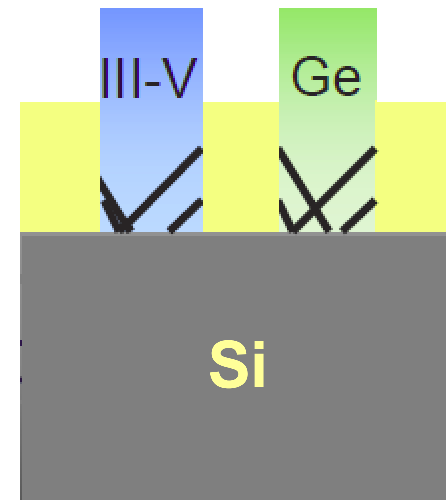
Si integration: InGaAs Trigate MOSFETs by Aspect Ratio Trapping





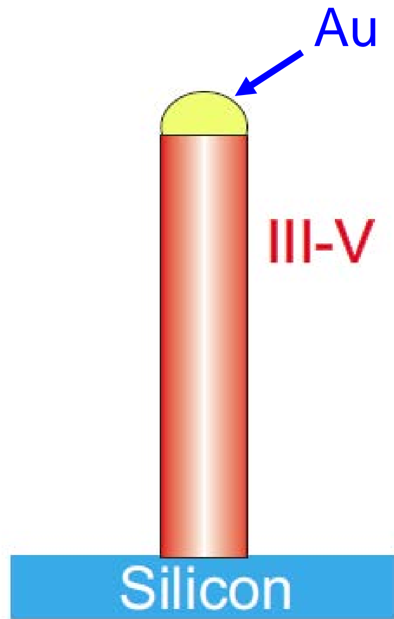


- Fin growth in narrow trench
- Mg-doped InP buffer

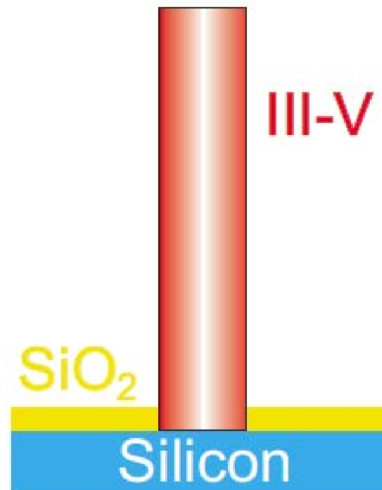


Waldron, VLSI Tech 2014

Si integration: InGaAs Vertical Nanowire MOSFETs by direct growth

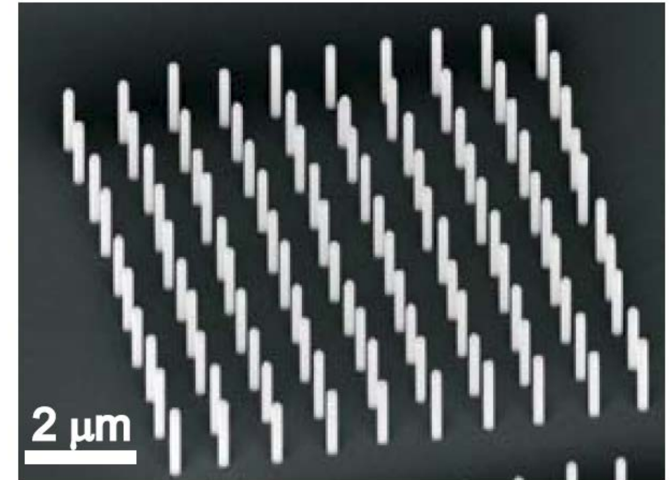


Vapor-Solid-Liquid (VLS) Technique

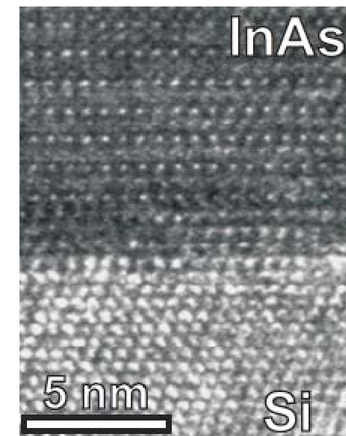


Selective-Area Epitaxy

Riel, MRS Bull 2014



InAs NWs on Si by SAE



Björk, JCG 2012

Conclusion:
exciting future for InGaAs electronics