



InGaAs Double-Gate Fin-Sidewall MOSFET

Alon Vardi, Xin Zhao and Jesús del Alamo
Microsystems Technology Laboratories, MIT

June 25, 2014

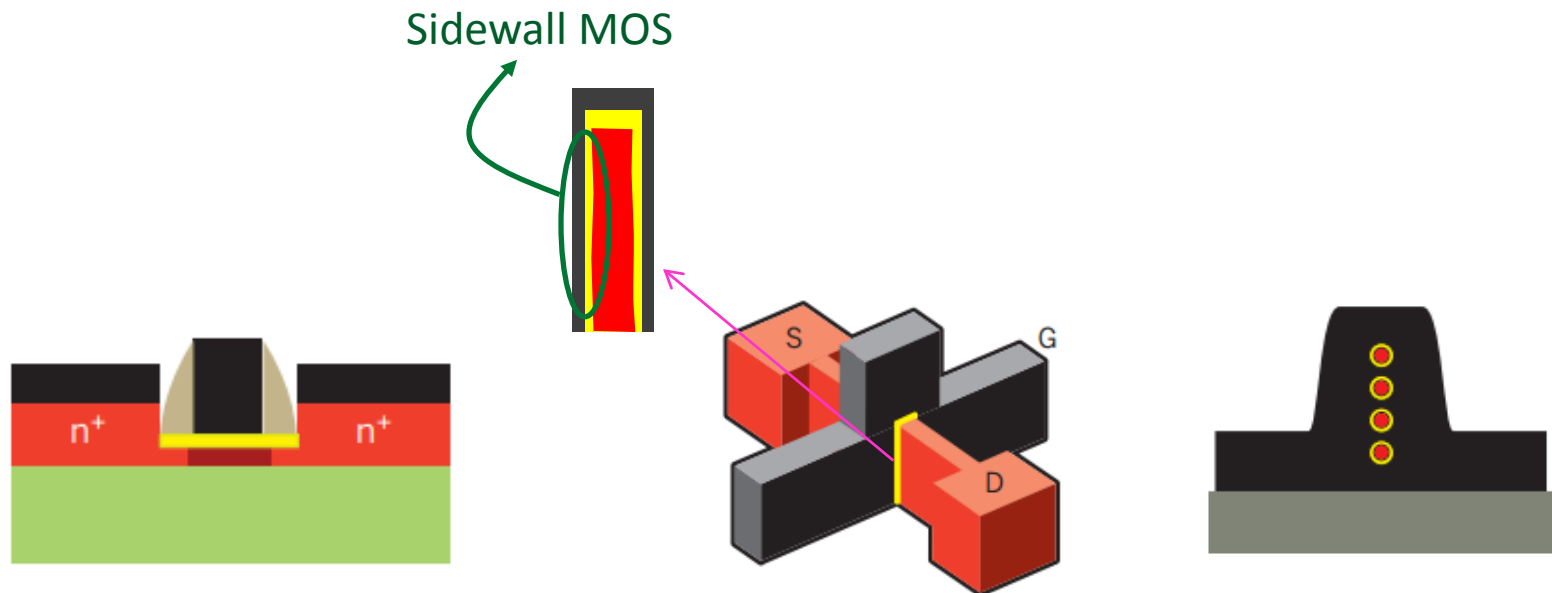
Sponsors: Sematech, Technion-MIT Fellowship,
and NSF E3S Center (#0939514)

Outline

- Motivation
- Process technology
- Results and analysis
- Conclusions

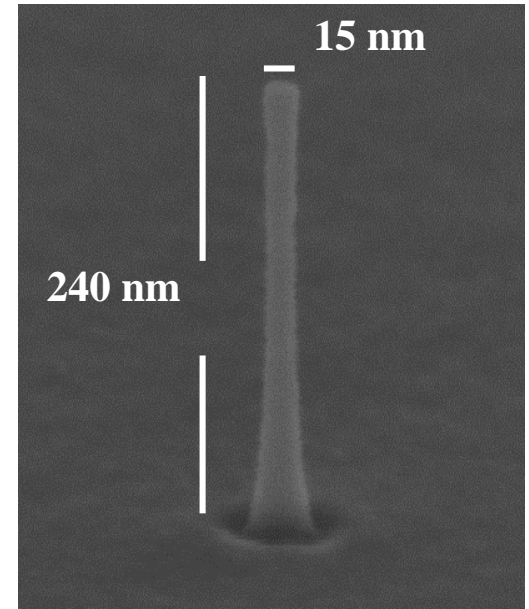
Motivation

- III-V MOSFET for sub – 10 nm CMOS
- Outstanding planar devices, but need tighter channel control through 3D designs
- Concerns about nano-structure sidewall fabricated by RIE
- Curing of plasma etching damage: forming gas annealing, digital etch



Key technologies

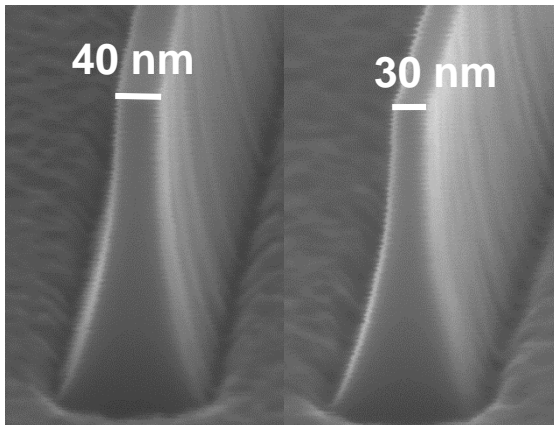
- **$\text{BCl}_3/\text{SiCl}_4/\text{Ar}$ RIE** of InGaAs nanostructures with smooth, vertical sidewall and high aspect ratio (>10).



Zhao, EDL 2014

- **Digital etch (DE)**: self-limiting O_2 plasma oxidation + H_2SO_4 oxide removal

Fins



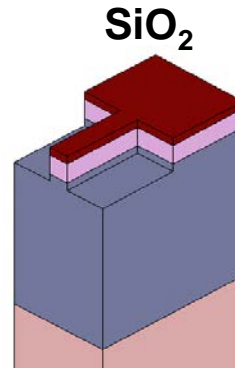
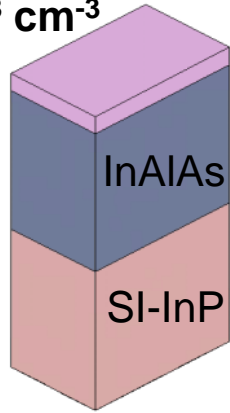
- Shrinks fin width by 2 nm per cycle
- Unchanged shape
- Reduced roughness

Lin, EDL 2014

As etched \rightarrow 5 cycles DE

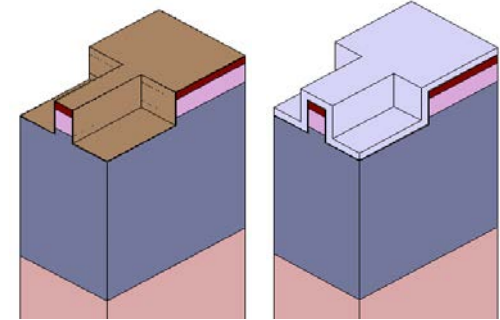
InGaAs finFET process flow

100 nm thick, n-InGaAs
 $N_d=10^{18} \text{ cm}^{-3}$



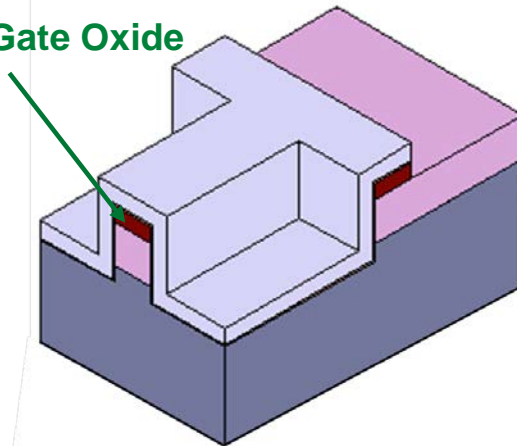
Fin Patterning

Gate dielectric Mo

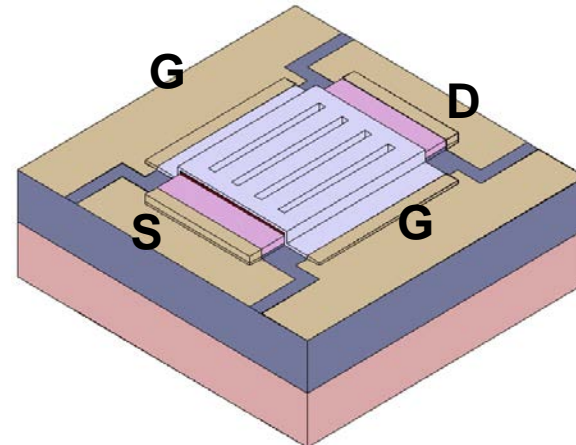


Gate stack

Thick Top Gate Oxide

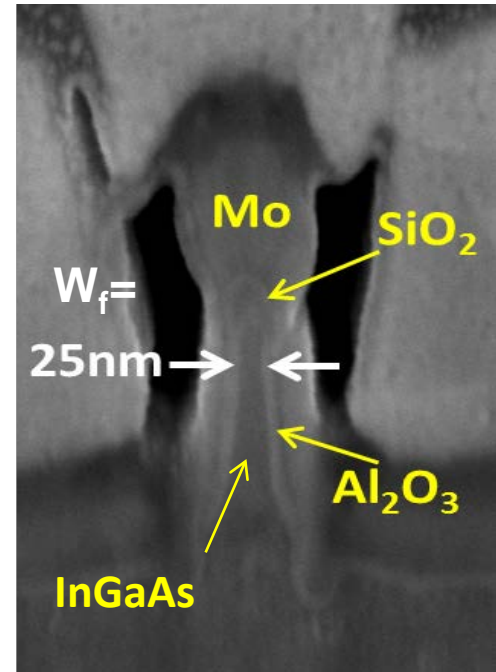
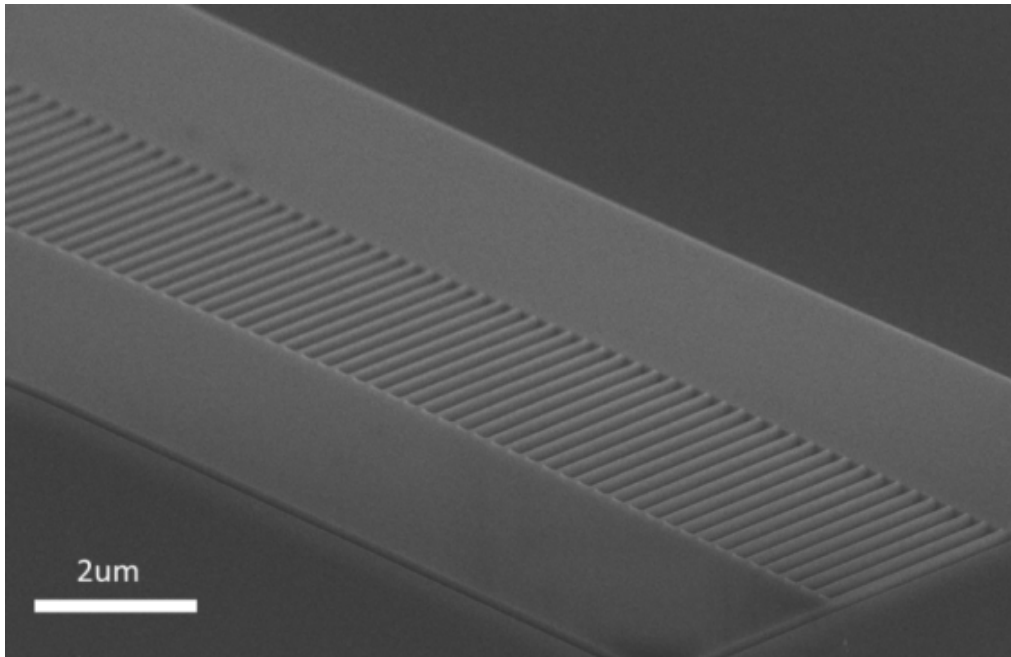


Gate Patterning



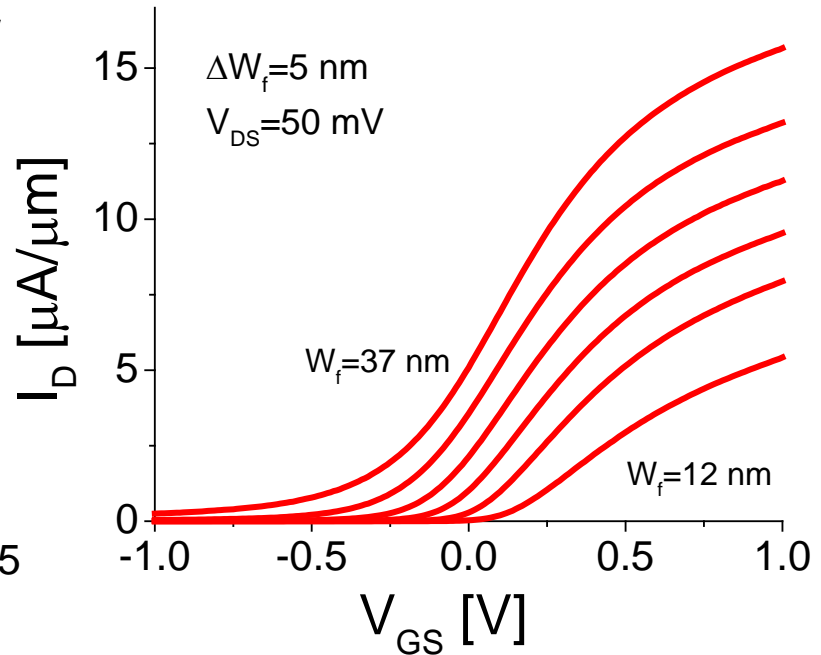
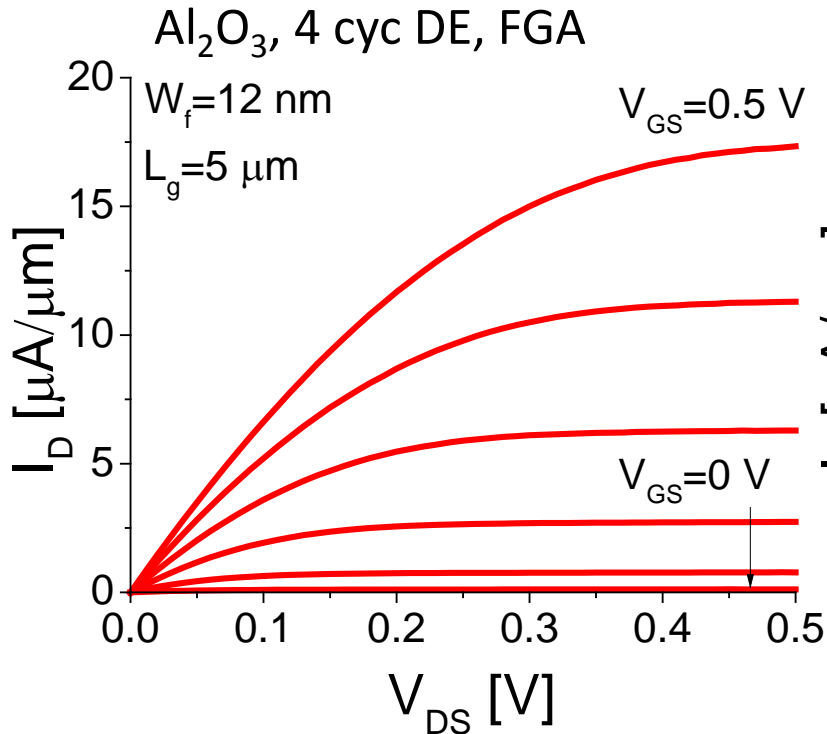
Contacts + Pads

InGaAs finFETs



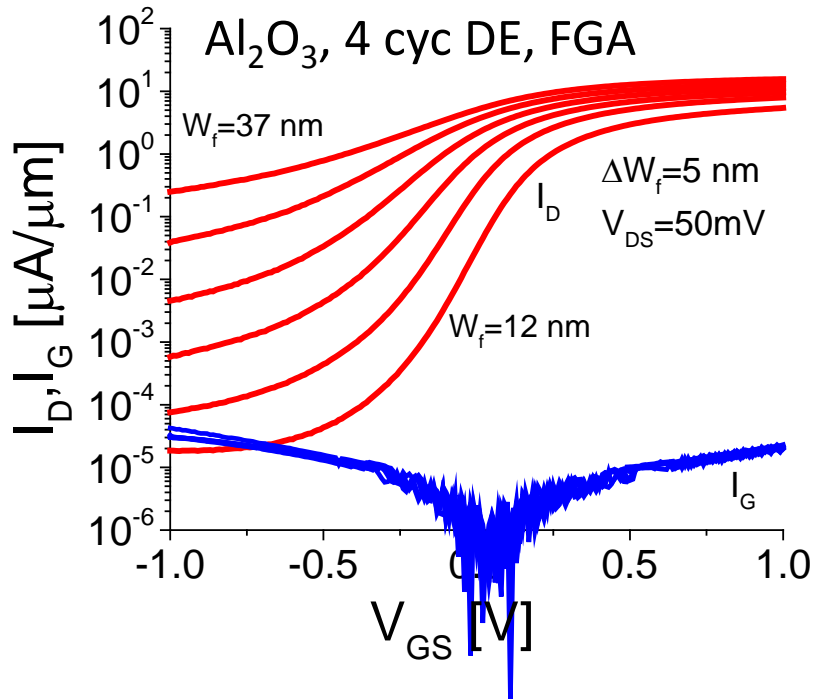
- Typical device consists of 100 fins, $L_g=5 \mu\text{m}$
- Process splits:
 - Number of digital etch cycles: 1, 2 and 4
 - HfO_2 vs. Al_2O_3 (same EOT of 4 nm)
 - w/ and w/o forming gas anneal (FGA): 30 min, 400°C

Electrical Characteristics

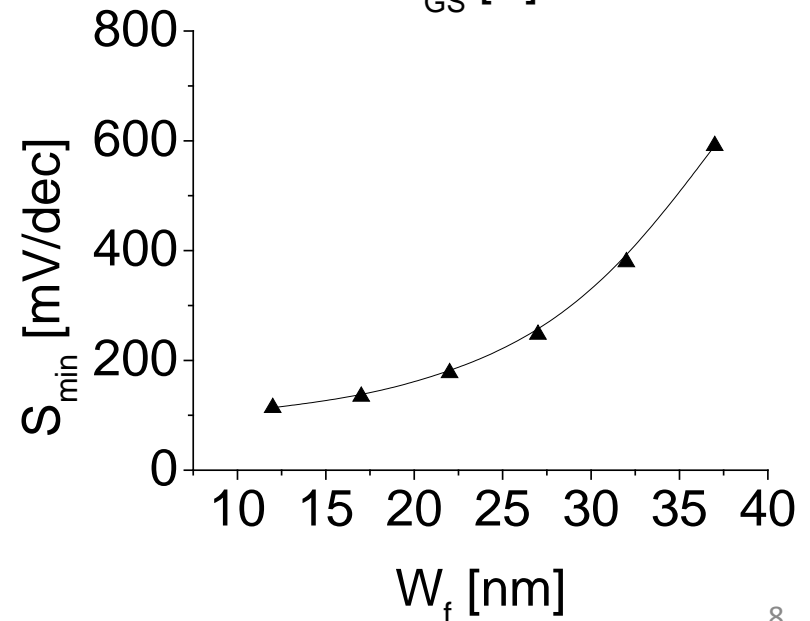
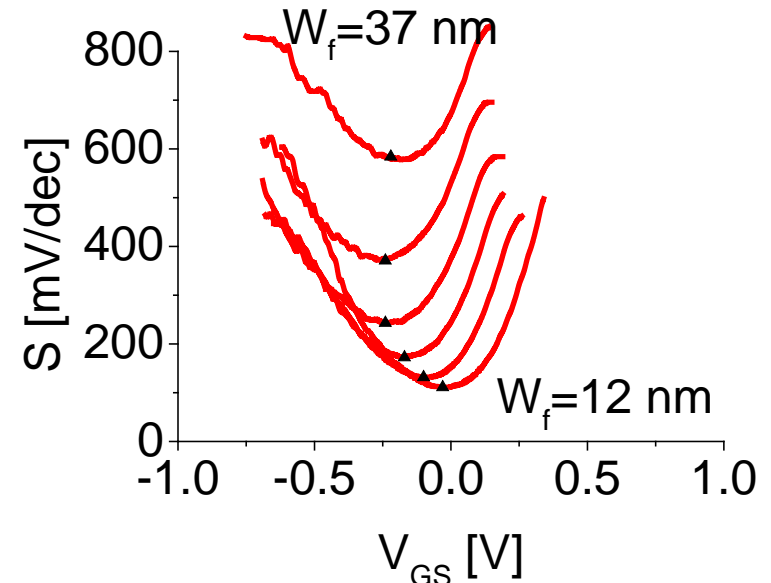


- Current normalized to active layer thickness (100 nm) and number of fins
- Good electrostatic control over fin sidewalls
- $W_f \uparrow \rightarrow V_t \downarrow$

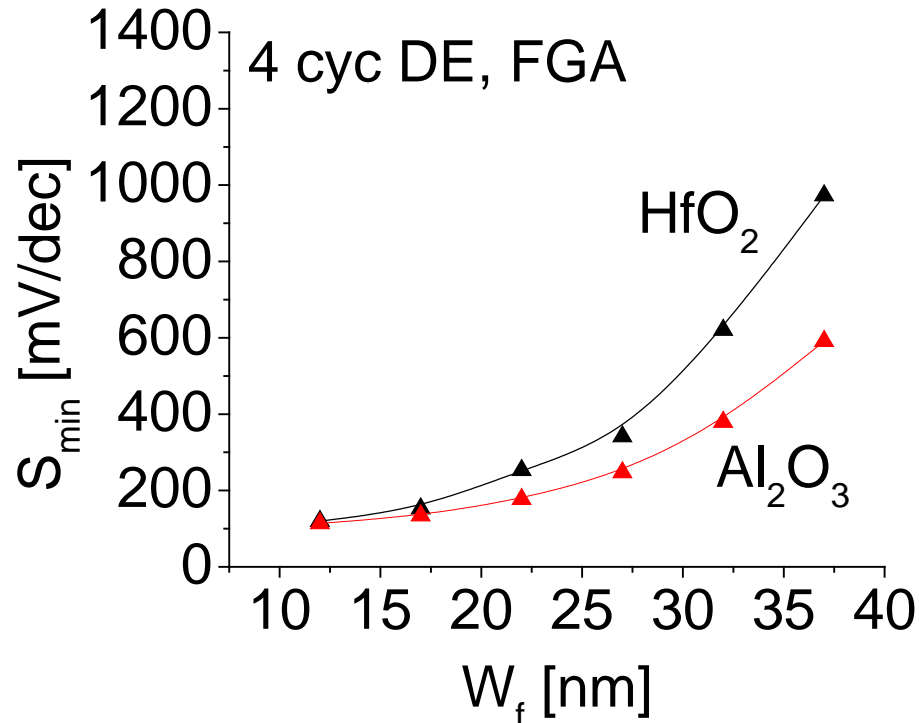
Subthreshold characteristics



- Subthreshold characteristics unrelated to I_G and governed by D_{it} on fin sidewalls

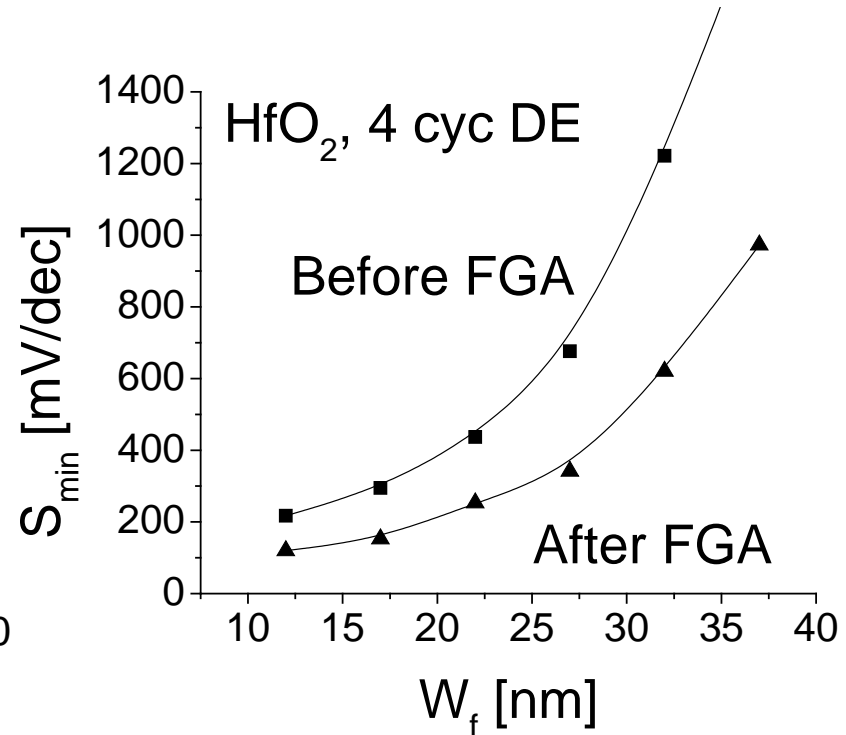
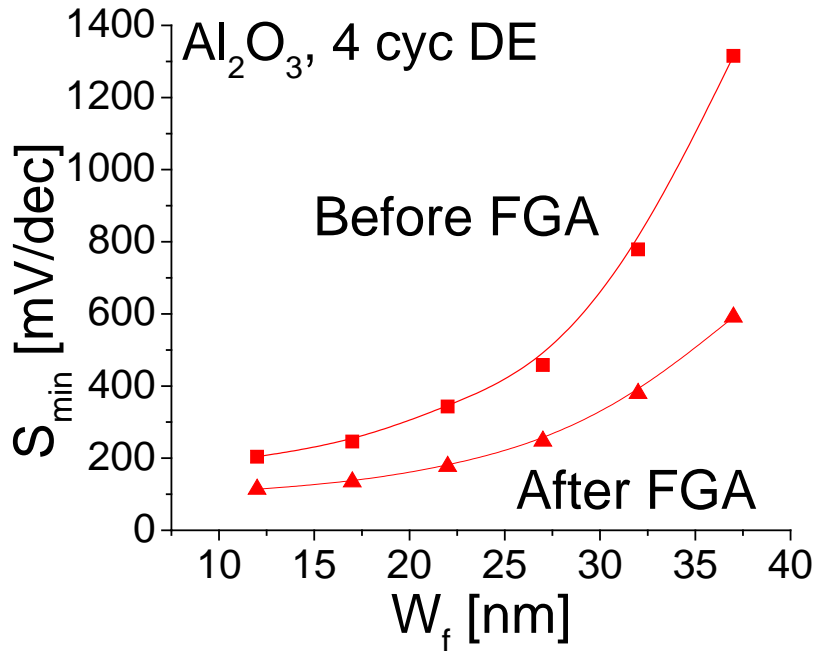


S_{\min} : Al_2O_3 vs. HfO_2



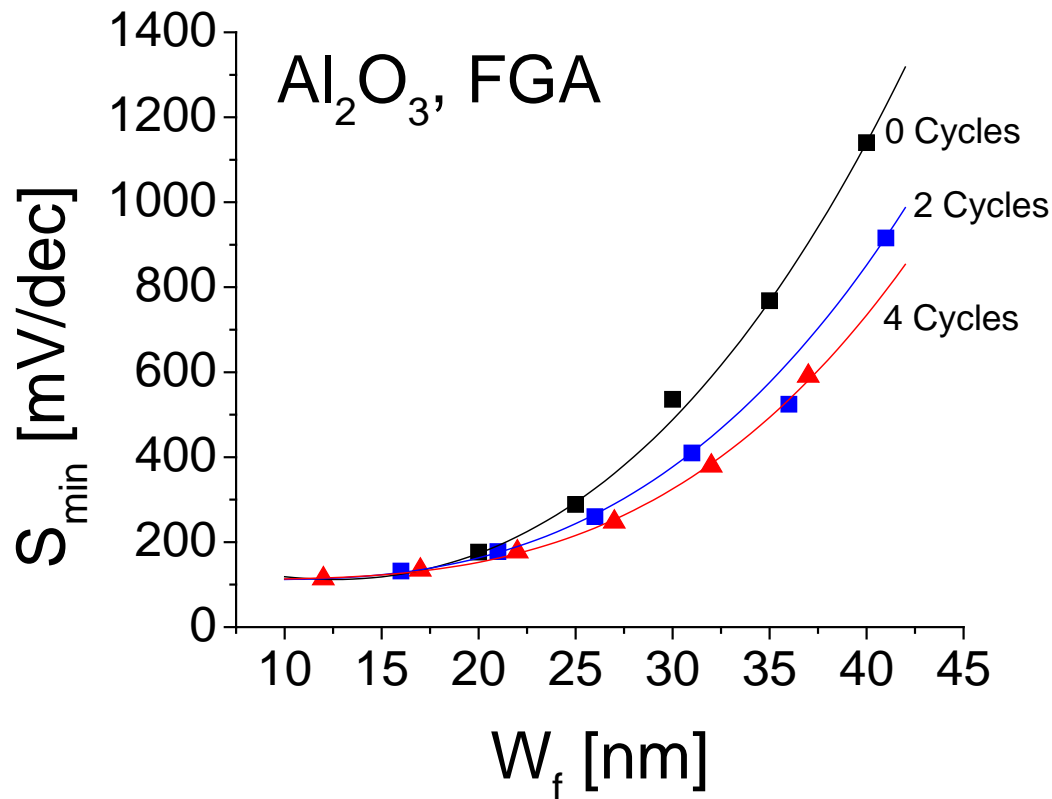
- Narrow W_f : $S_{\min}(\text{HfO}_2) \cong S_{\min}(\text{Al}_2\text{O}_3)$
- Wide W_f : $S_{\min}(\text{HfO}_2) > S_{\min}(\text{Al}_2\text{O}_3)$

S_{\min} : Effect of forming gas annealing



- FGA $\rightarrow S_{\min} \downarrow$ at all W_f on both oxides

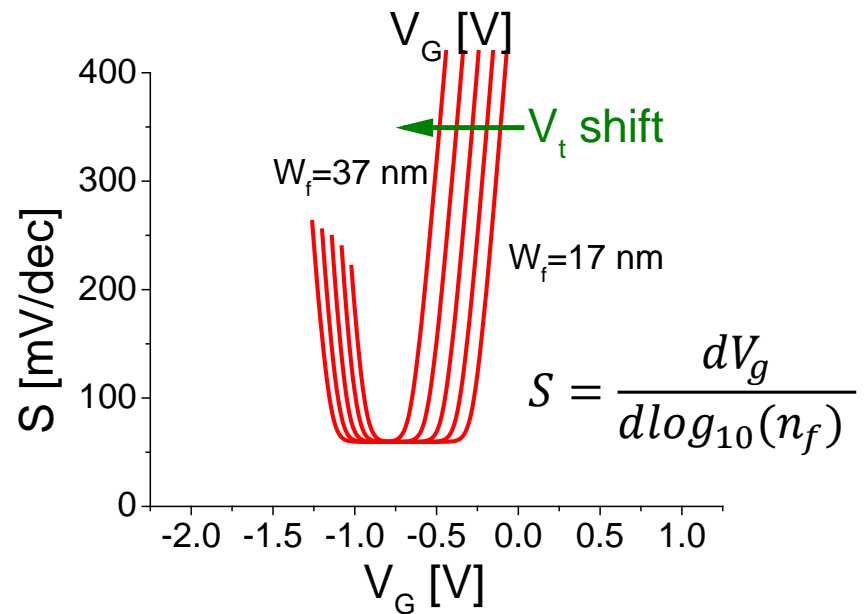
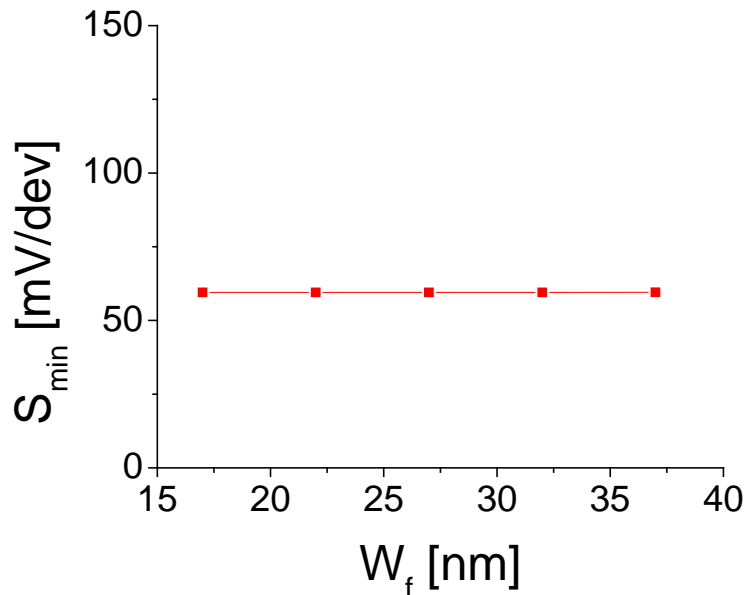
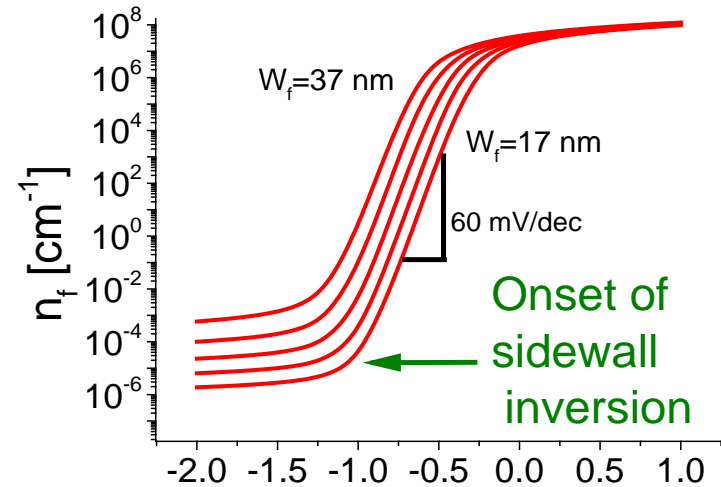
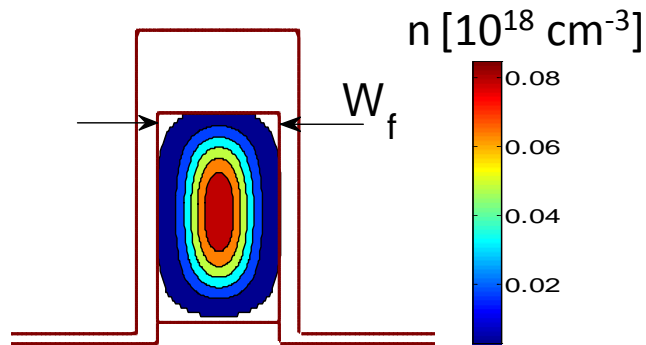
S_{\min} : Effect of digital etching



- Narrow W_f : S not affected by digital etch
- Wide W_f : #DE cycles $\uparrow \rightarrow S_{\min} \downarrow$

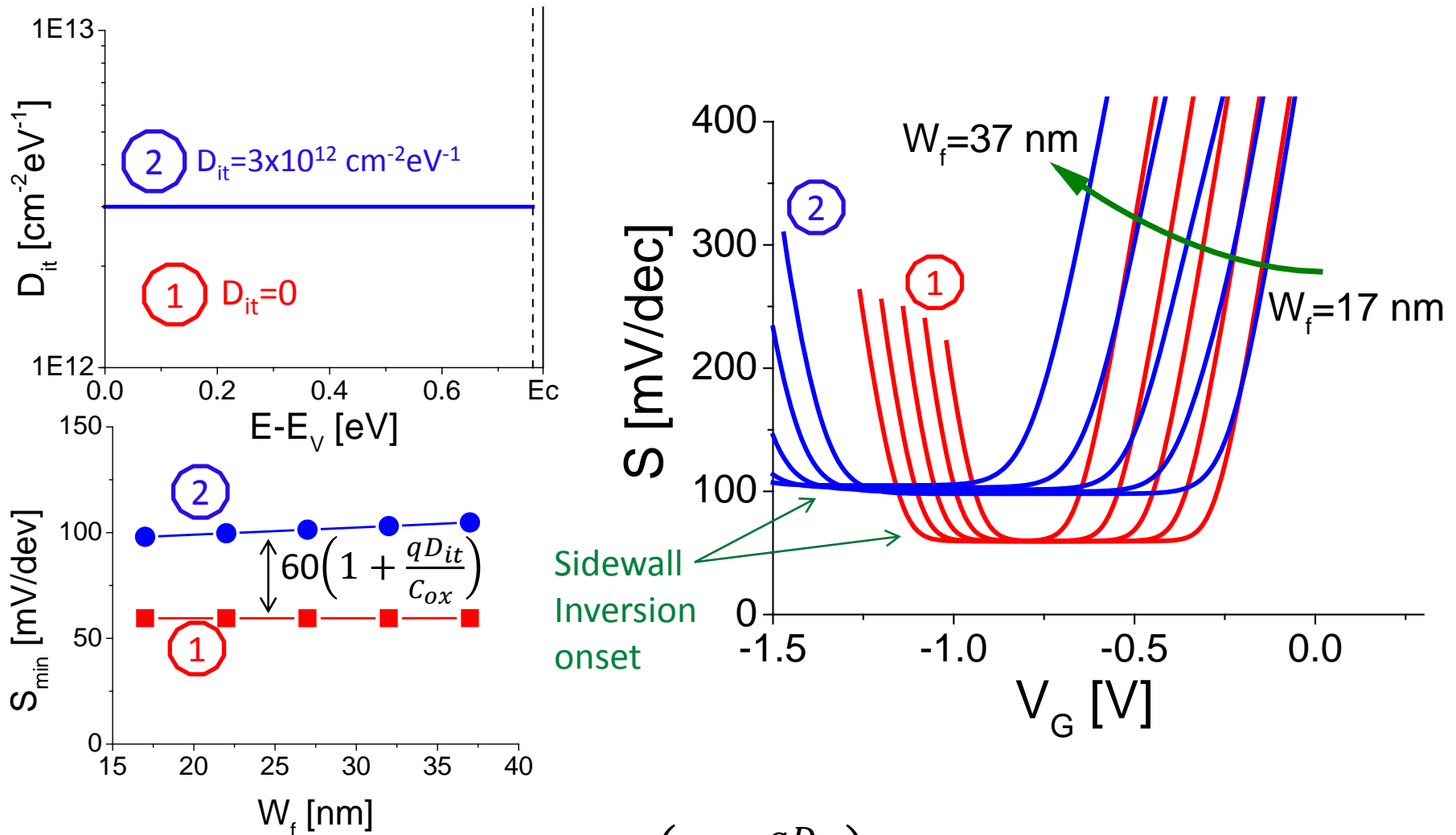
Simulations: Ideal interface

2D Poisson-Schrödinger (nextnano)



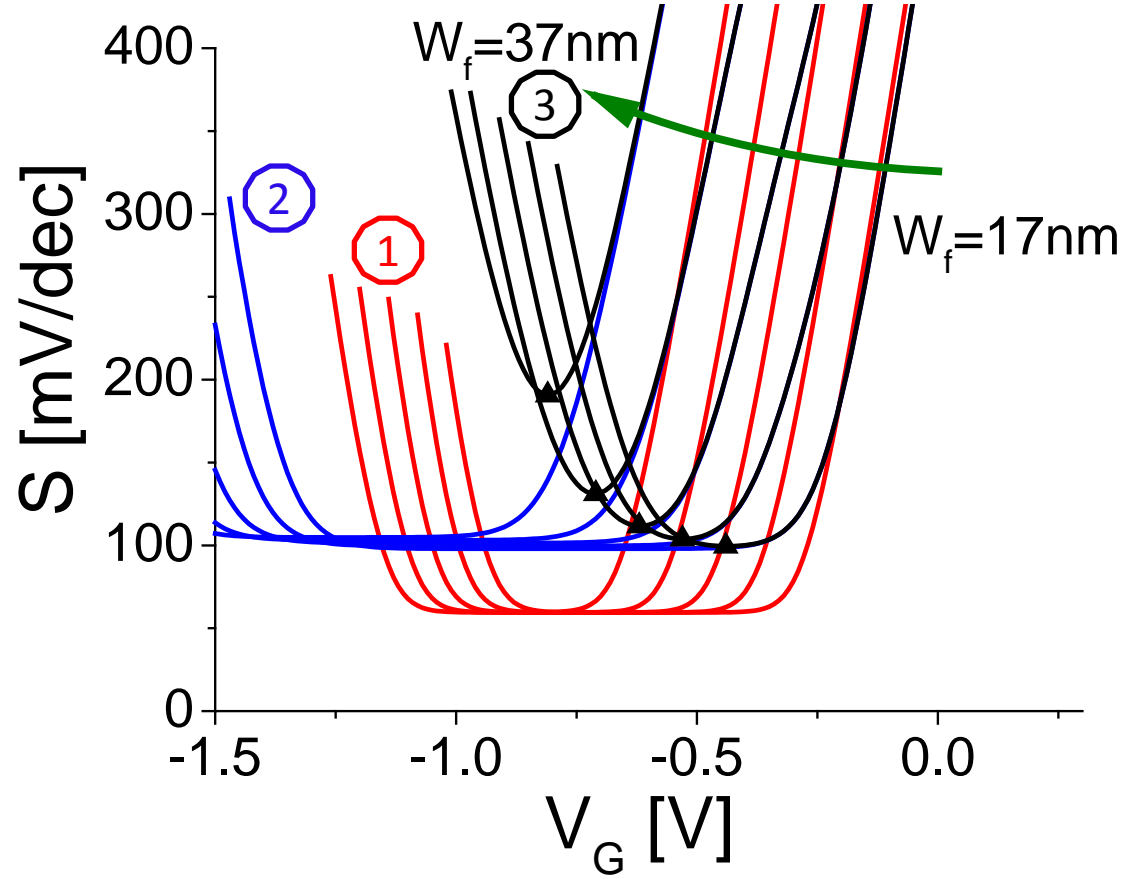
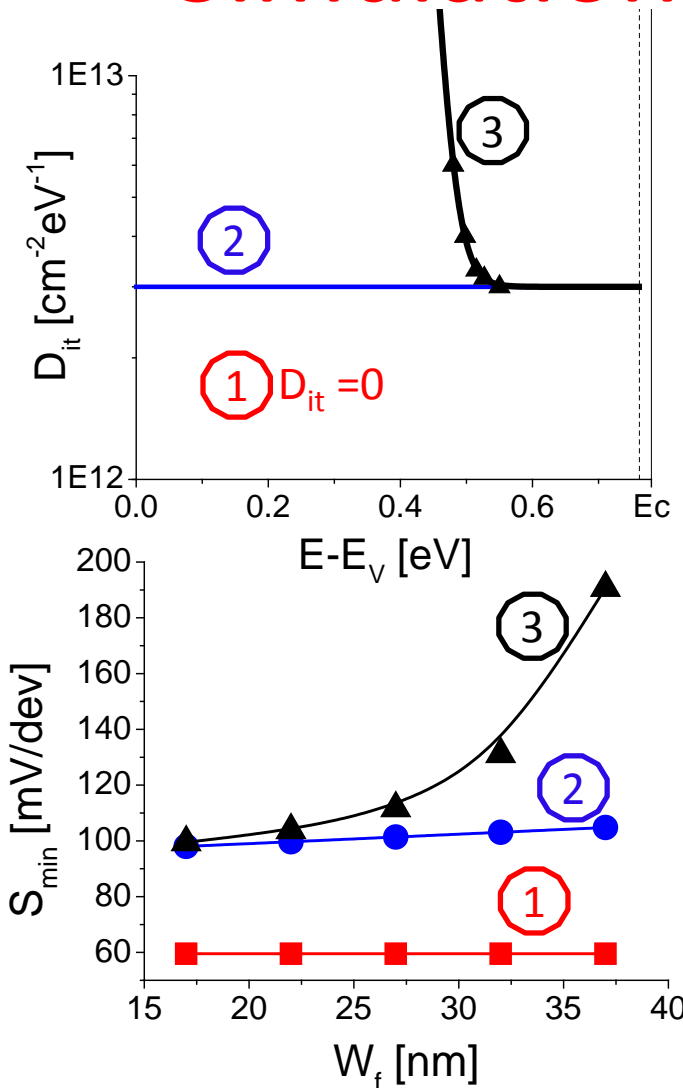
- $D_{it}=0 \rightarrow S_{\min}=60 \text{ mV/dec}$, independent of W_f

Simulations: uniform D_{it} across bandgap



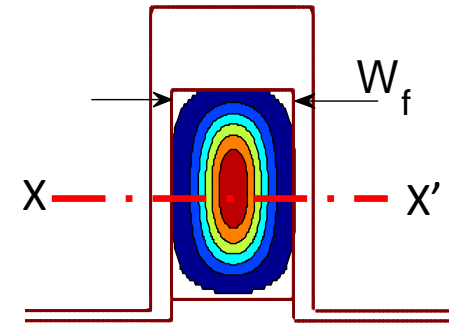
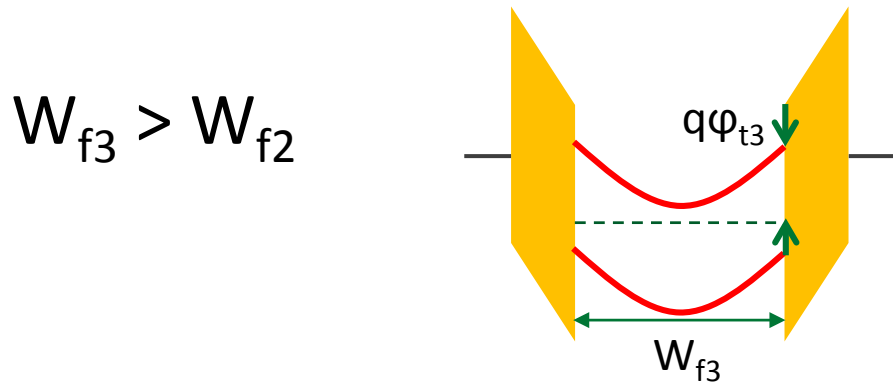
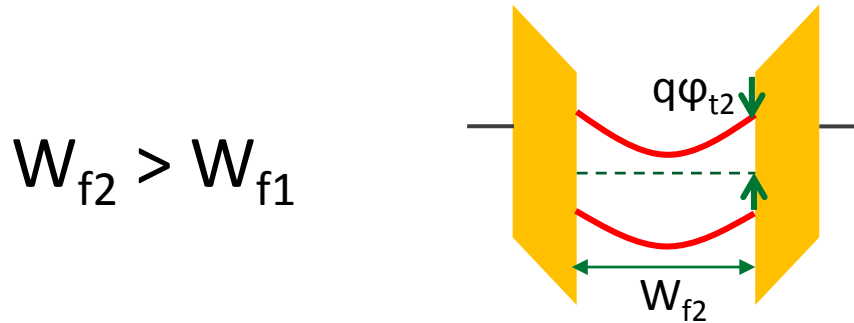
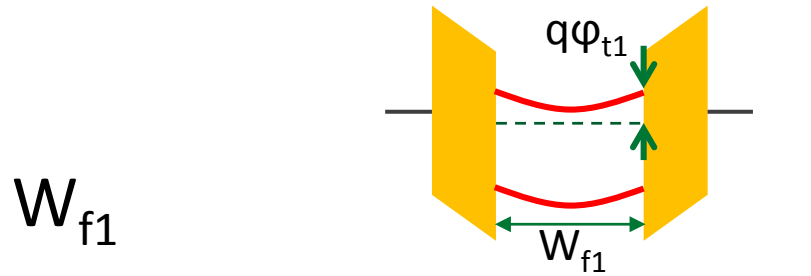
- $D_{it} > 0$ (uniform) $\rightarrow S_{min} = 60 \left(1 + \frac{qD_{it}}{C_{ox}} \right)$, independent of W_f
- Onset of inversion shifts to negative voltage (stretch out)

Simulations: D_{it} rising toward VB



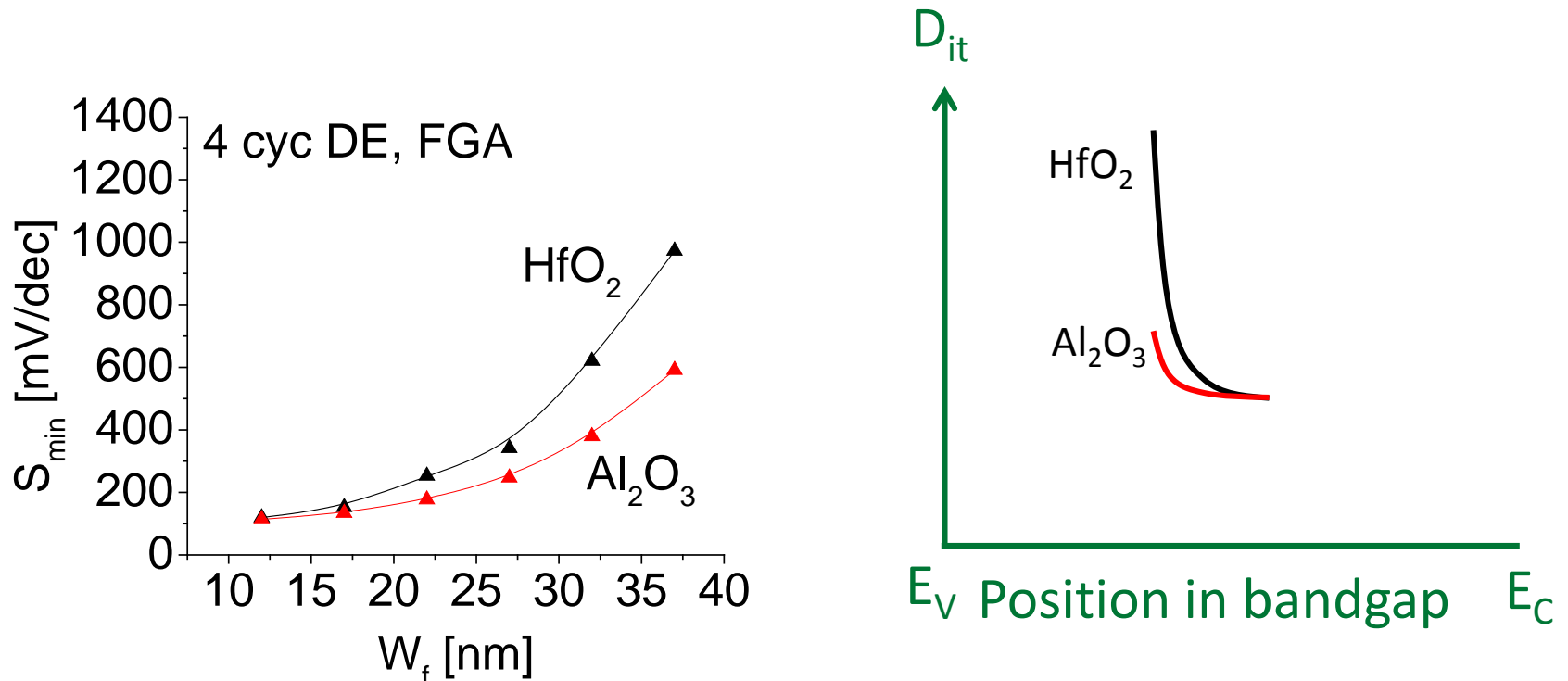
- D_{it} rising towards VB: $W_f \uparrow \rightarrow S_{min} \uparrow$
- S_{min} for different W_f probe D_{it} at different locations in the band gap

Simulations: $S_{\min} \leftrightarrow \varphi_s$



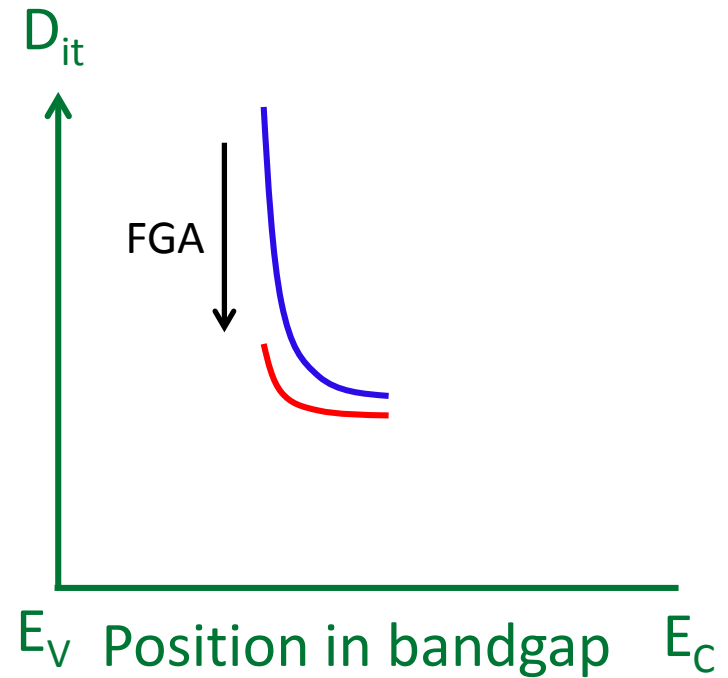
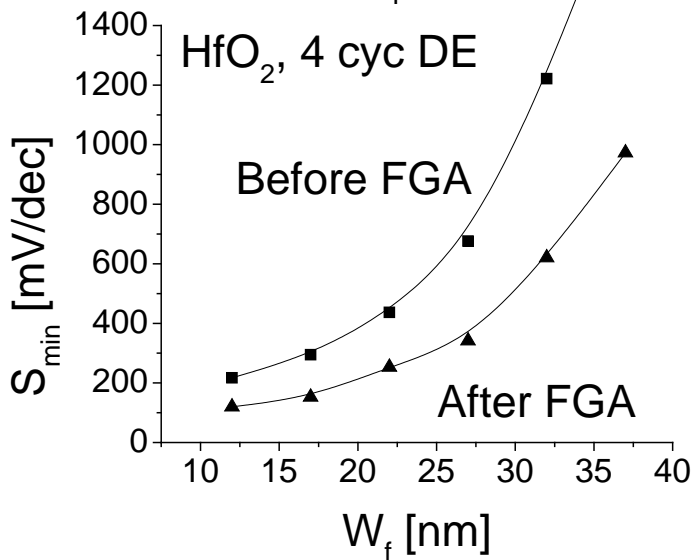
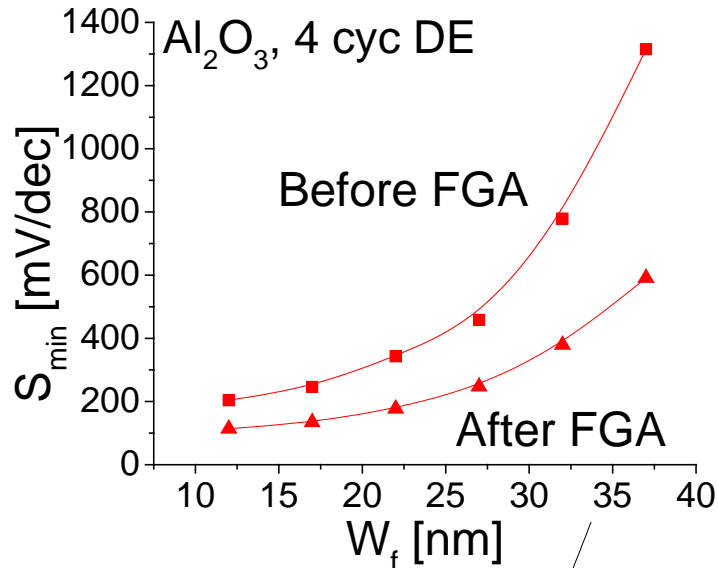
- $W_f \uparrow \rightarrow |\varphi_t| \uparrow \rightarrow |V_t| \uparrow$ (negative V_t shift)
- $W_f \uparrow \rightarrow S_{\min}$ probe D_{it} closer to VB

Effect of Oxide type on D_{it} profile



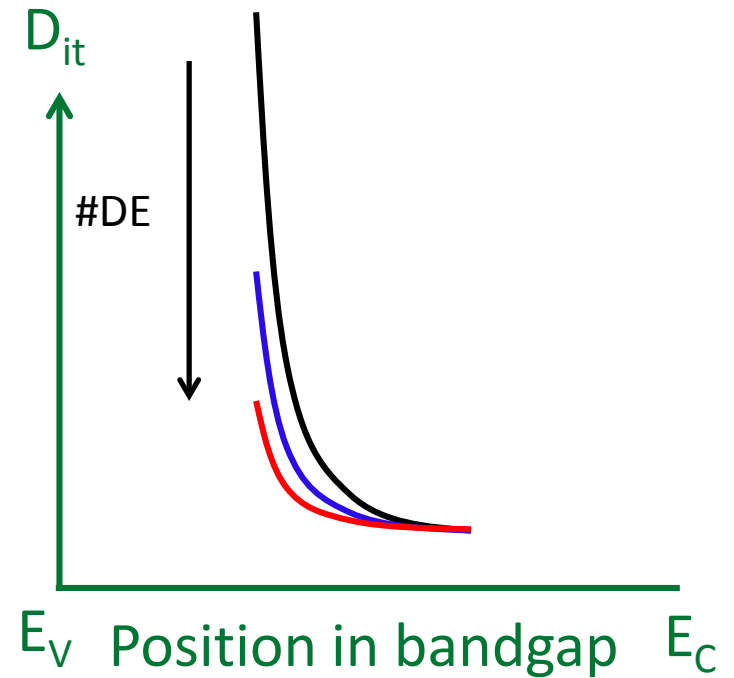
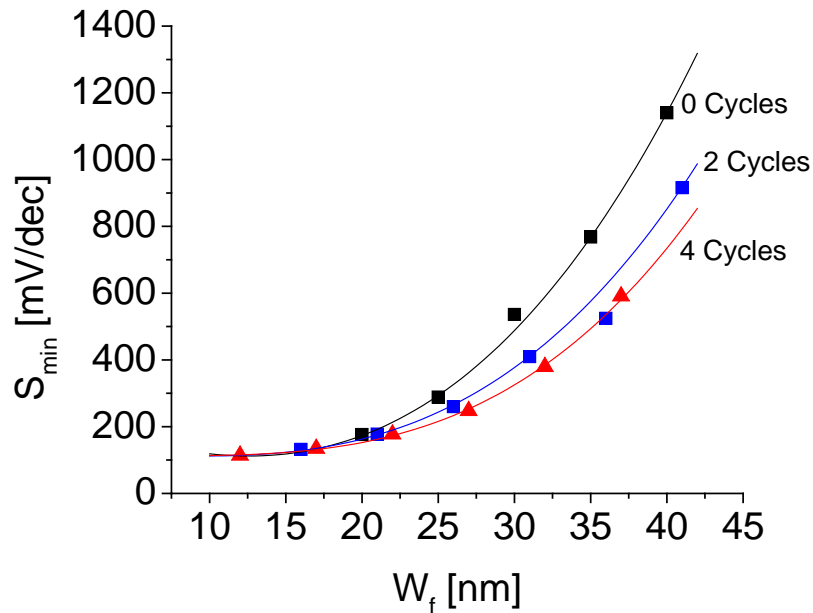
- Al_2O_3 yield better D_{it} than HfO_2 in lower part of bandgap

Effect of FGA on D_{it} profile



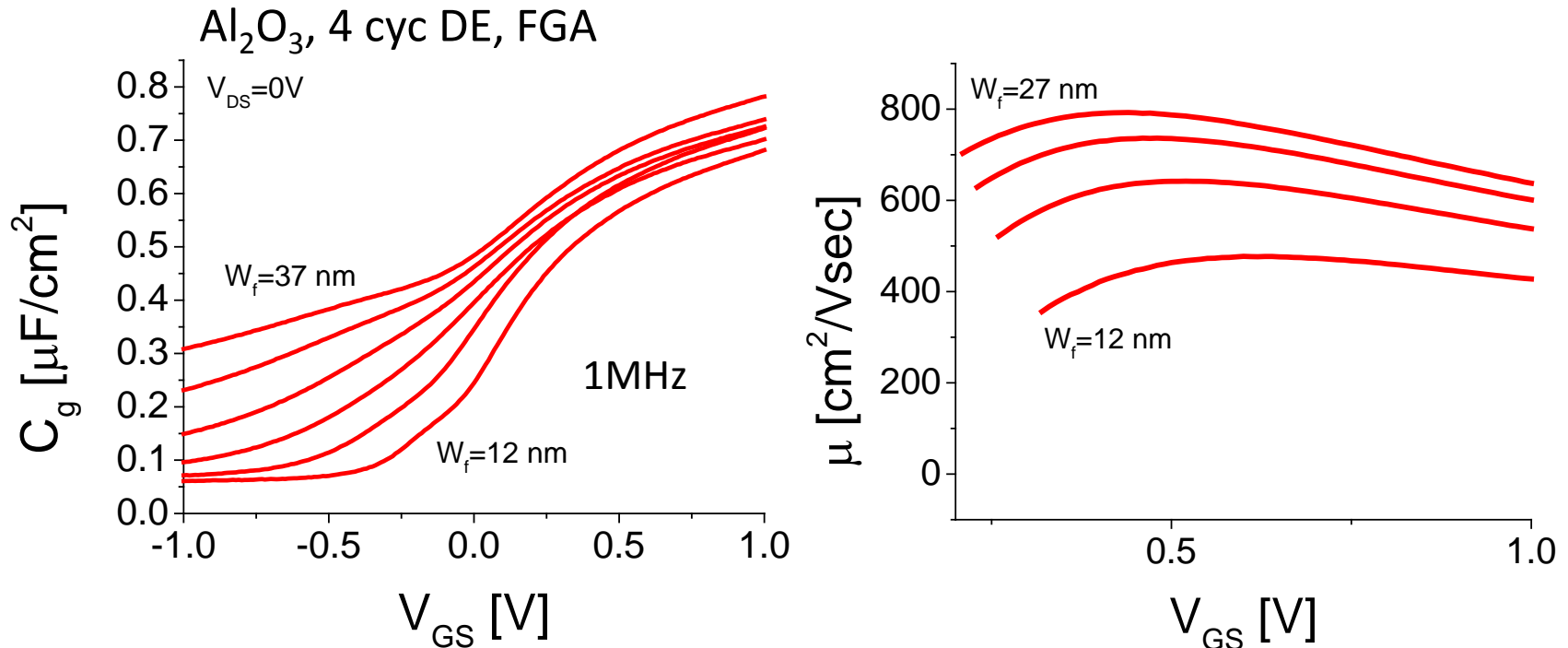
- FGA reduces D_{it} everywhere in bandgap

Effect of DE on D_{it} profile



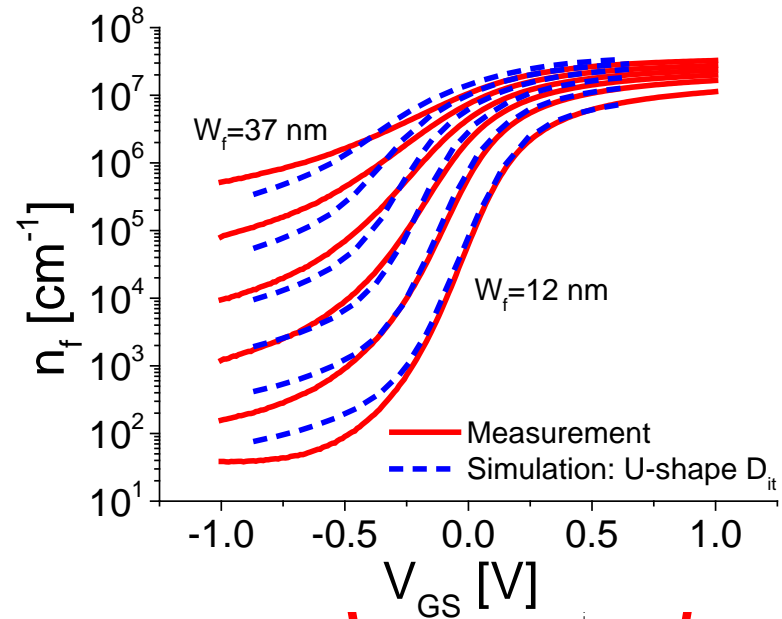
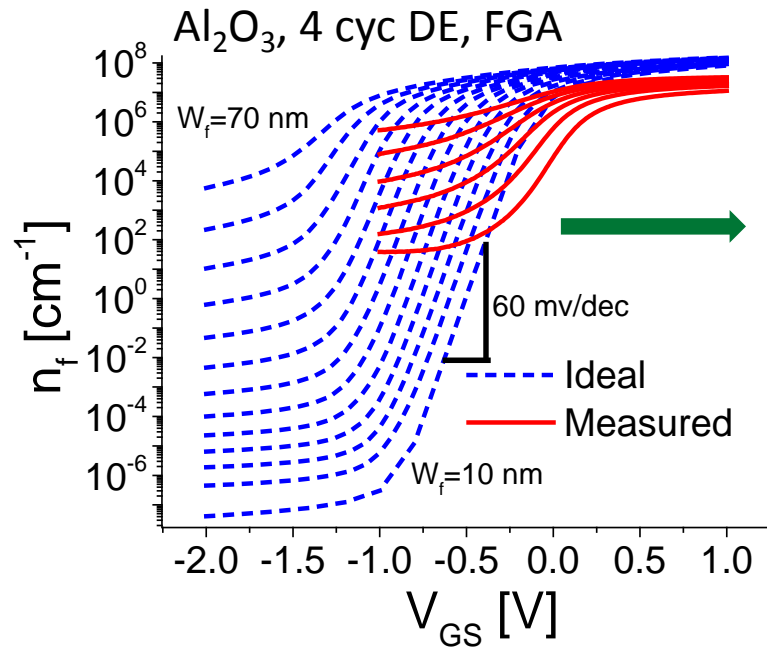
- DE reduces D_{it} in lower part of bandgap

Towards a more detailed analysis: Mobility extraction

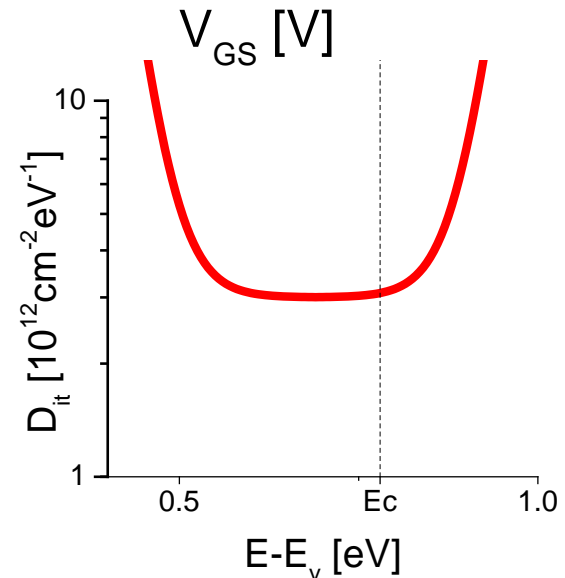


- Mobility is 5-7 times smaller than expected
- $W_f \downarrow \rightarrow \mu \downarrow \rightarrow$ sidewall scattering
- From I_D and $\mu \rightarrow$ extract n_f

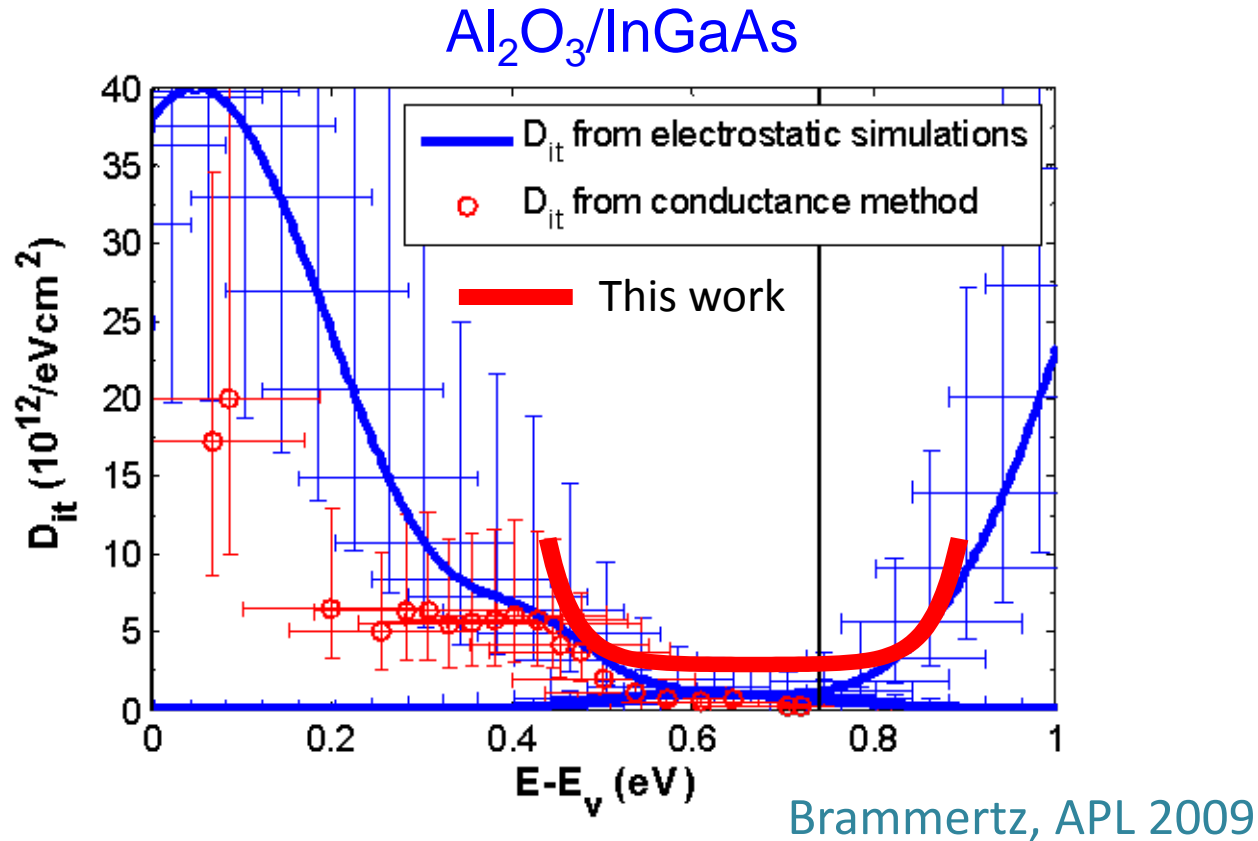
Fitting of D_{it} profile



- U-shape D_{it} profile provides excellent agreement with measurements



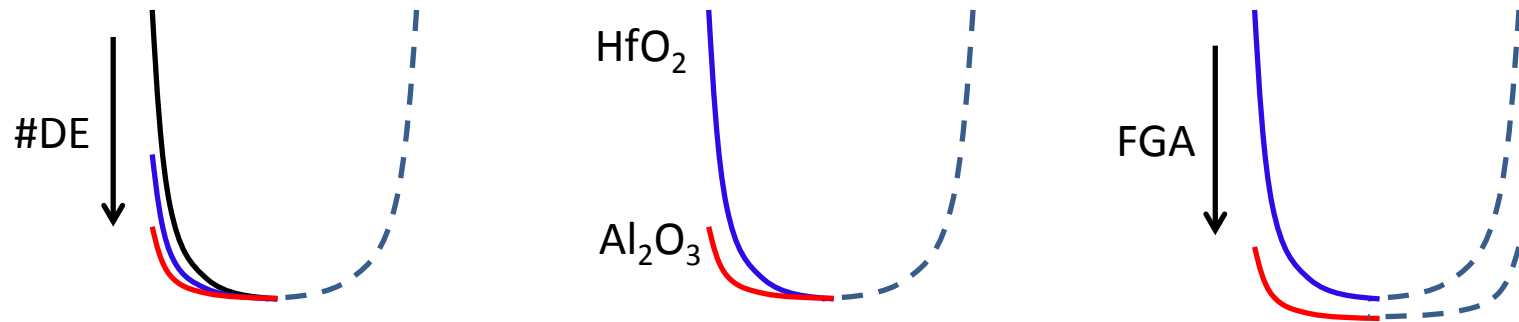
Comparison to planar structures



- D_{it} distribution on properly prepared dry etched sidewalls approaches that of planar structures

Conclusions

- Study of D_{it} on dry etched nano-structure sidewalls
- U – shape D_{it} distribution as in planar MOSFETs
- FGA reduces D_{it} everywhere while DE lowers D_{it} toward the valence band
- HfO_2 and Al_2O_3 give comparable results near CB, but rise of D_{it} toward VB stronger for HfO_2



- With all treatments, D_{it} level approaches level obtained on planar structures