Nanometer-Scale III-V Electronics

J. A. del Alamo

Microsystems Technology Laboratories, MIT

The Age of Silicon Symposium

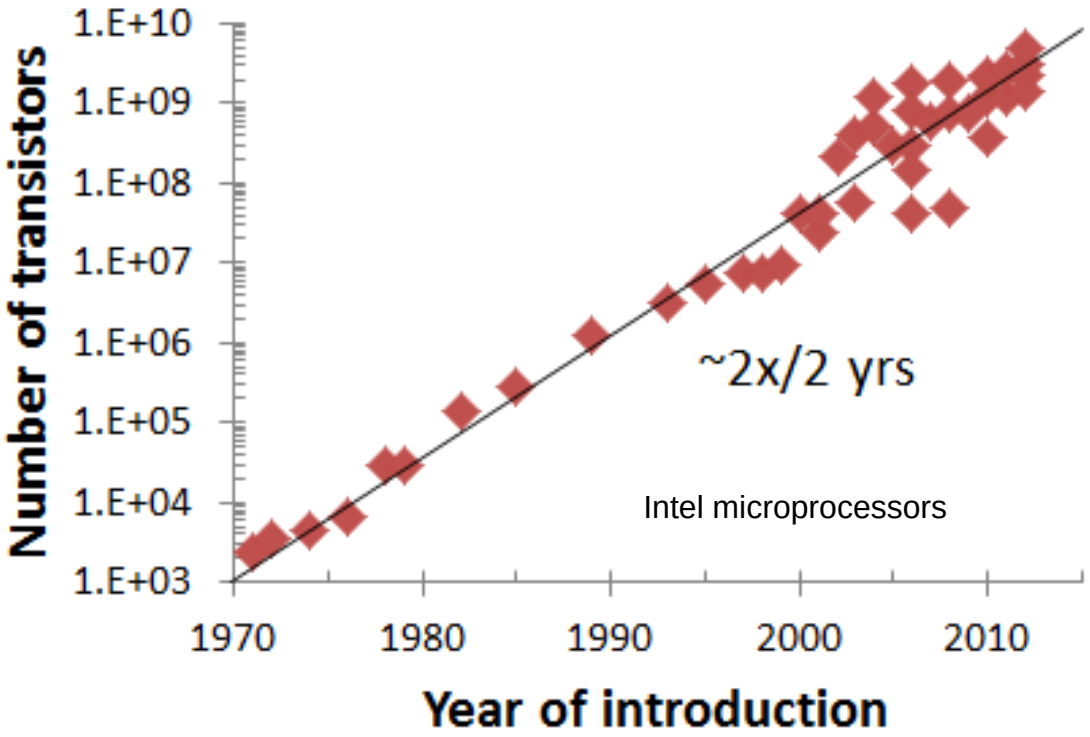
MIT, July 25, 2014

Acknowledgements:

- D. Antoniadis, A. Guo, D.-H. Kim, T.-W. Kim, D. Jin, J. Lin, W. Lu, A. Vardi, N. Waldron, L. Xia, X. Zhao
- Sponsors: Intel, FCRP-MSD, ARL, SRC, NSF, Sematech, Samsung
- Labs at MIT: MTL, NSL, SEBL

Moore’s Law

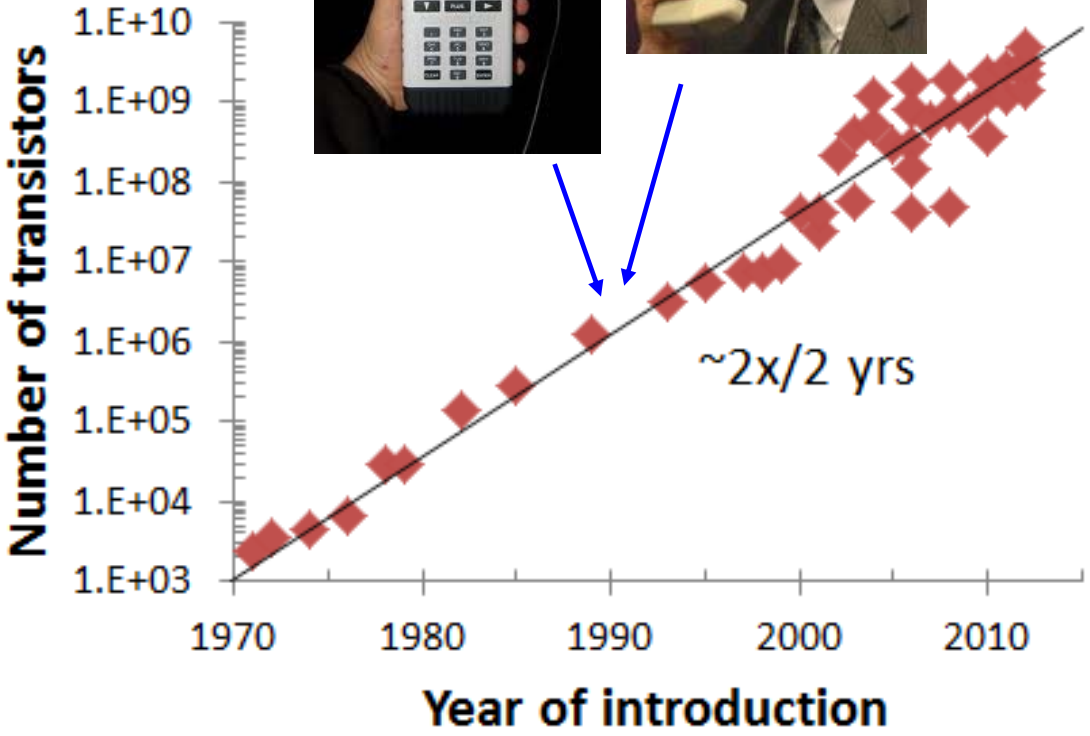
Moore’s Law = exponential increase in transistor density



What if Moore's Law had stopped in 1990?

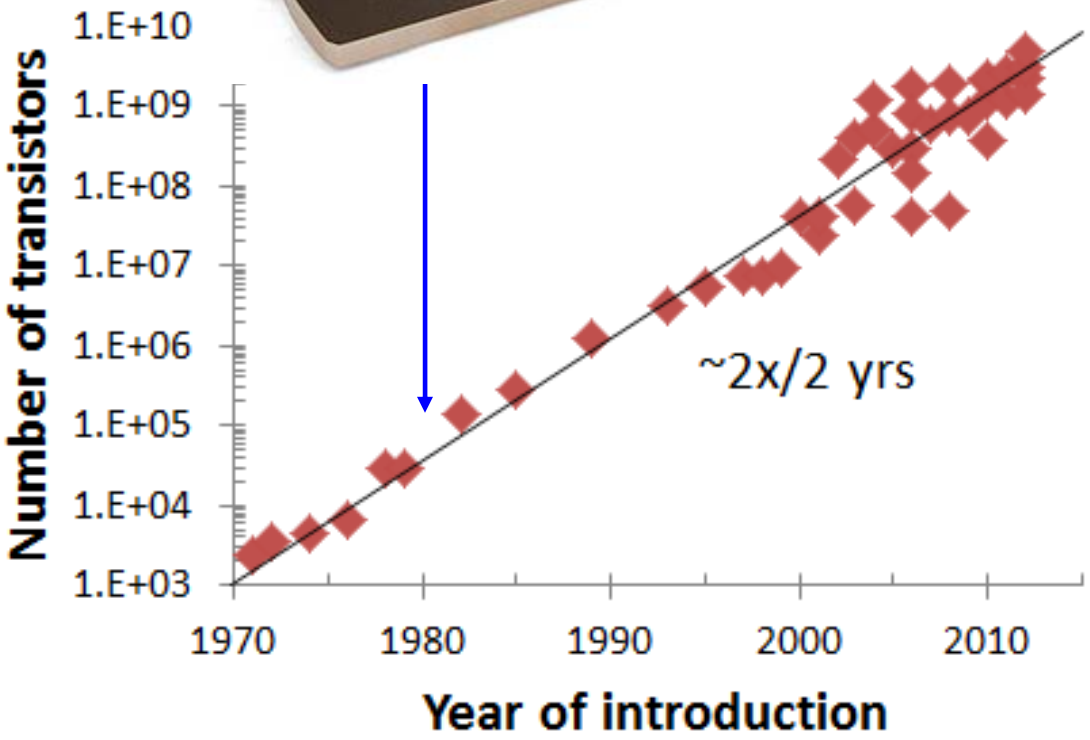
GPS handheld device circa 1990

Cell phone circa 1990



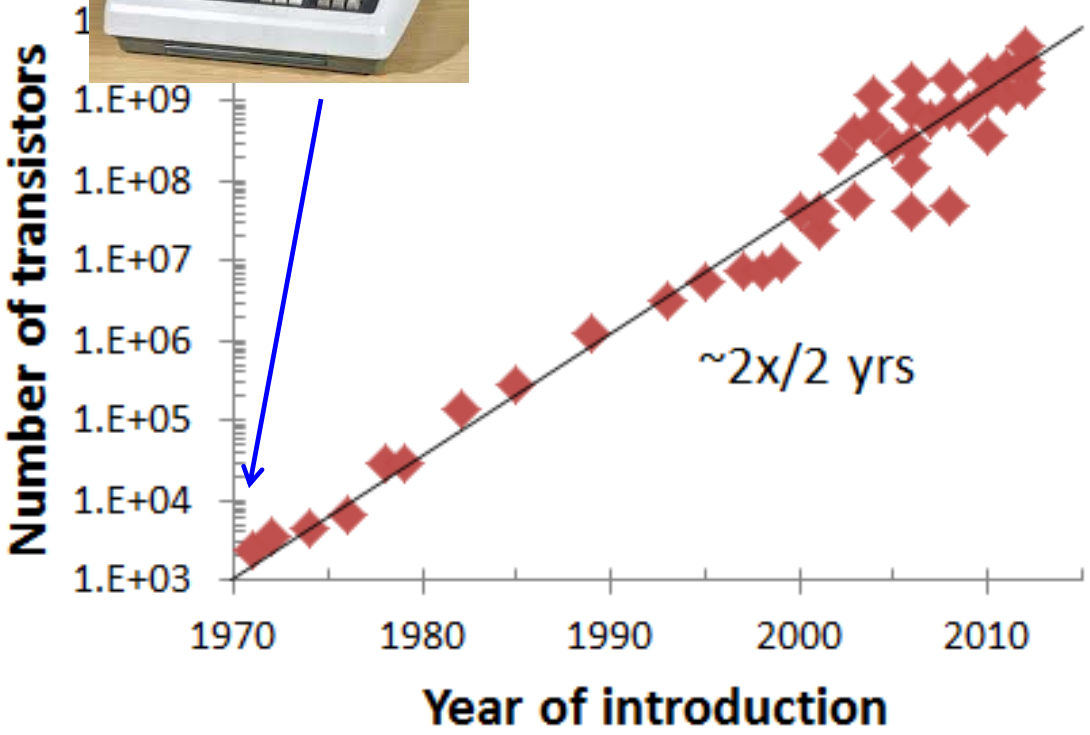
What if Moore's Law had stopped in 1980?

Laptop computer circa 1981

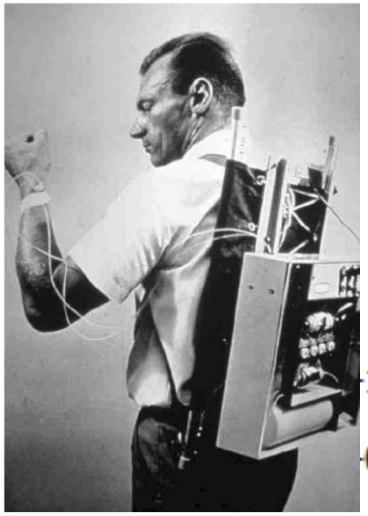


What if Moore's Law had stopped in 1970?

Desktop calculator 1970

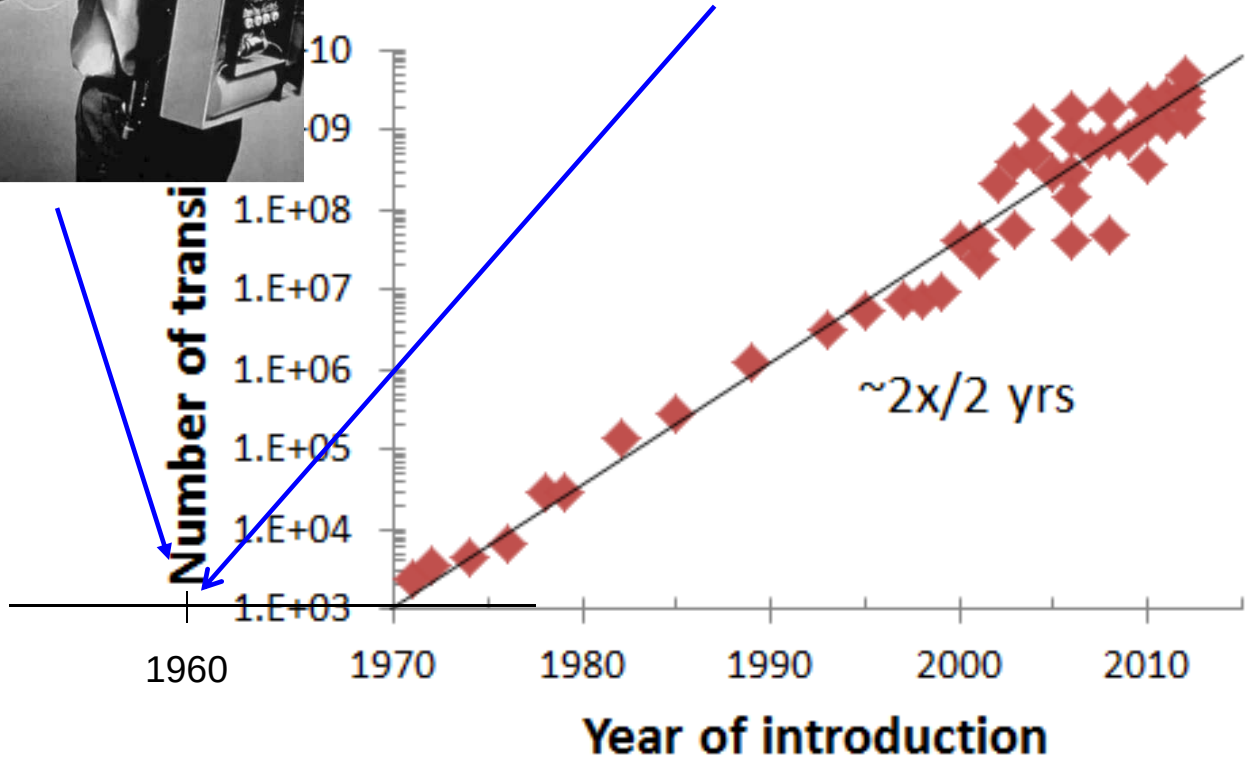


What if Moore's Law had never happened?



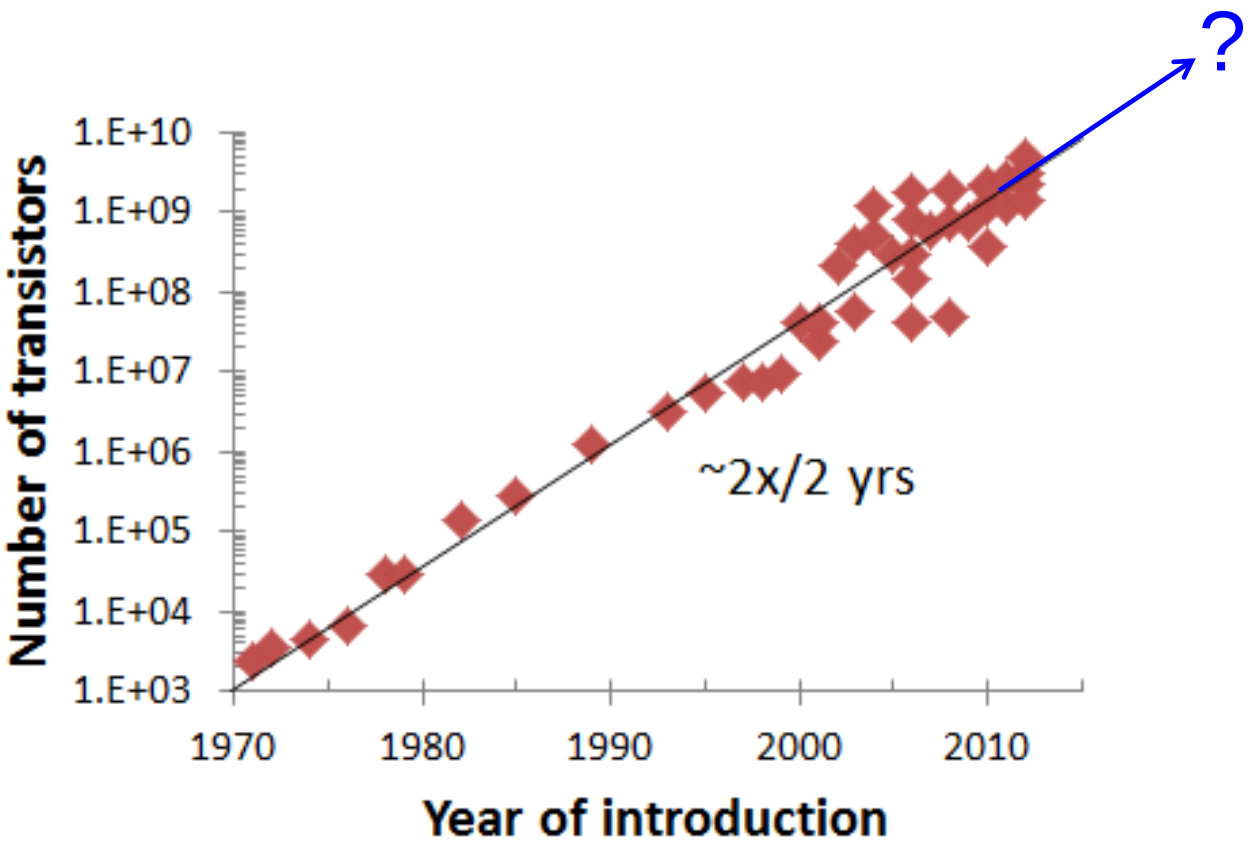
Insulin pump circa 1960

"Personal calculator" circa 1960



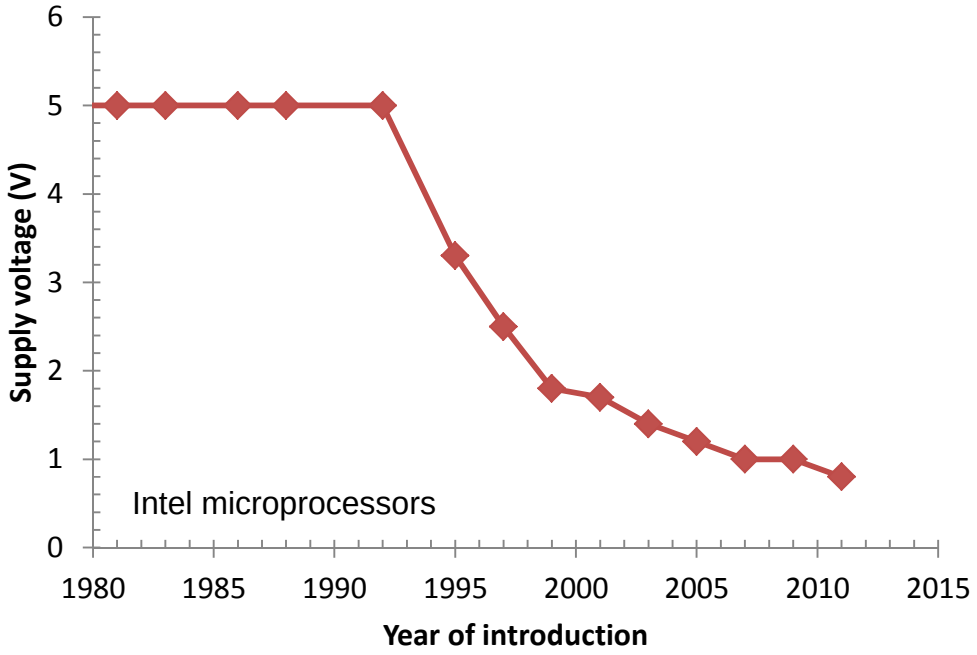
Moore's Law

How far can Si support Moore's Law?



Transistor scaling → Voltage scaling

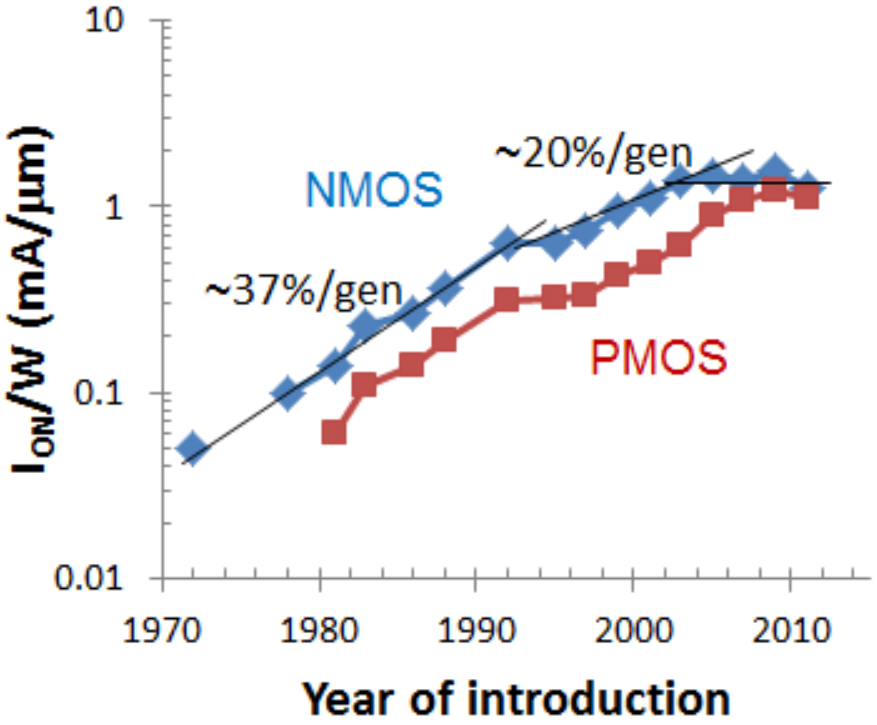
Power management demands reduction in supply voltage.



Supply voltage reduction saturating in recent years

Voltage scaling → Si transistor performance suffers

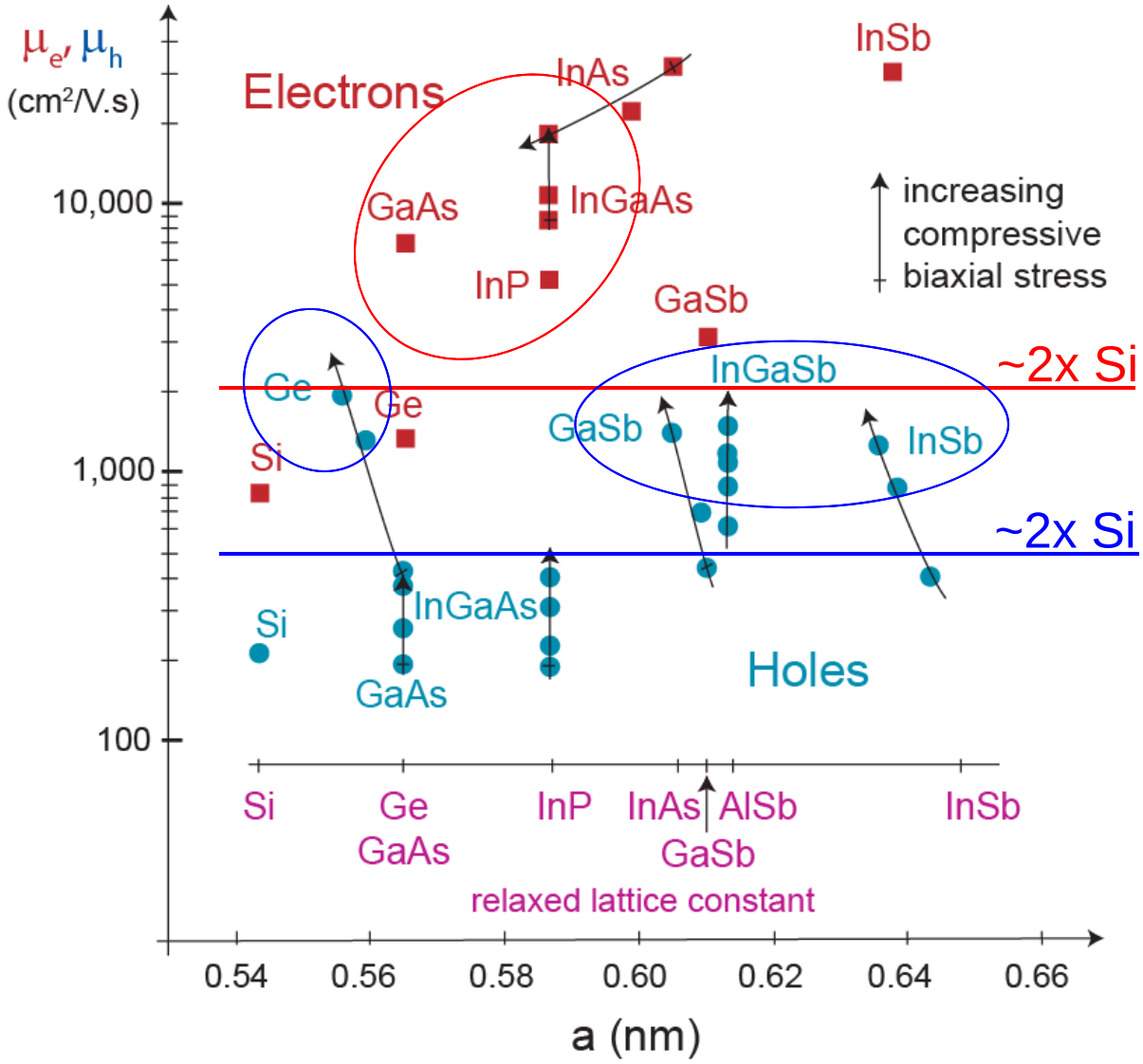
Transistor current density:



Transistor performance saturated in recent years


THE END IS NEAR.
YOU WISH.

Options for post-Si CMOS



NMOS:

→ GaAs, InGaAs, InP

PMOS:

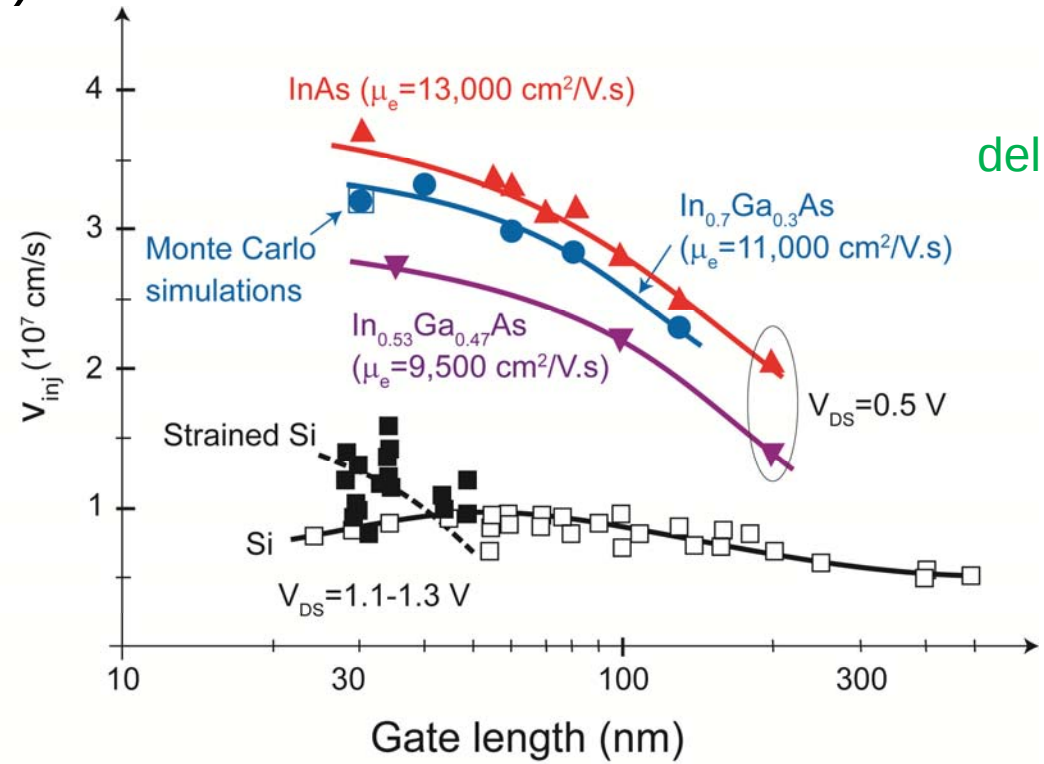
→ Ge, InGaSb

Different lattice constant for n-FETs and p-FETs

del Alamo, Nature 2011

Electron injection velocity: InGaAs vs. Si

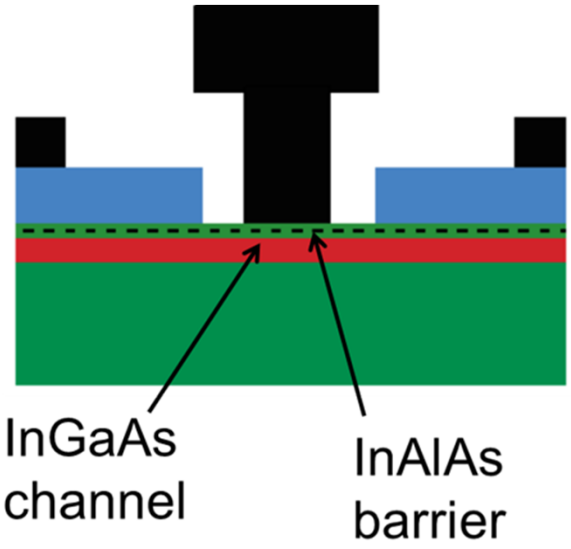
Measurements in High Electron Mobility Transistors (HEMTs):

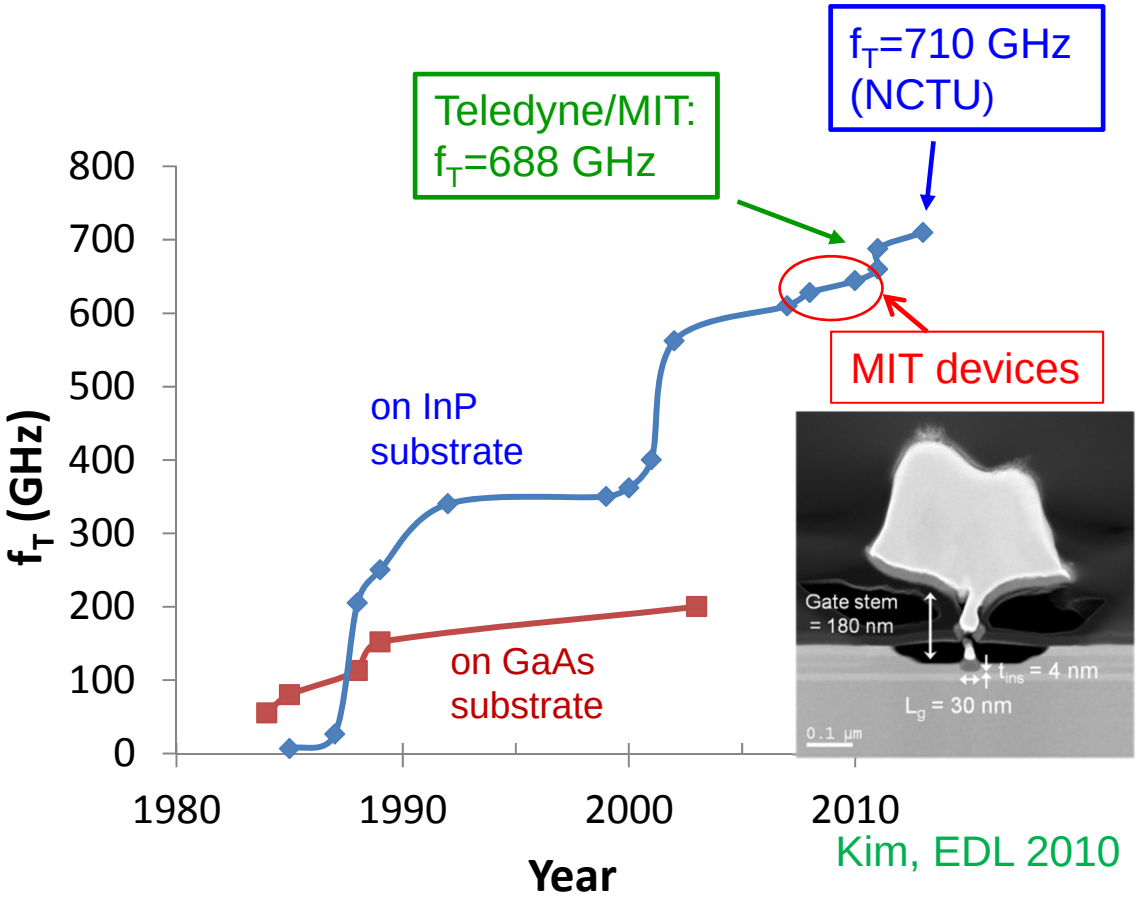


del Alamo, Nature 2011

- v_{inj}(InGaAs) increases with InAs fraction in channel
- v_{inj}(InGaAs) > 2v_{inj}(Si) at less than half V_{DD}
- ~100% ballistic transport at L_g~30 nm

InGaAs HEMT: high-frequency record vs. time





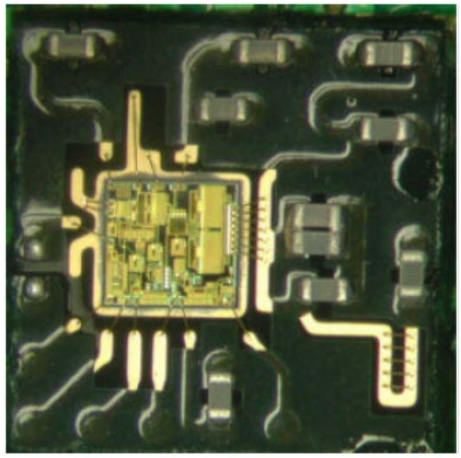
Kim, EDL 2010

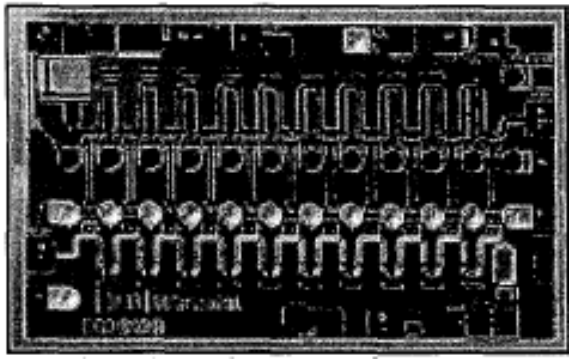
Best high-frequency performance of any transistor on any material system

InGaAs Electronics Today

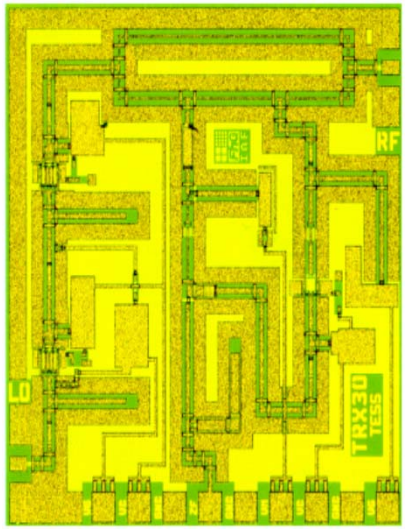
TriQuint and Skyworks Power iPhone 5

UMTS-LTE PA module
Chow, MTT-S 2008

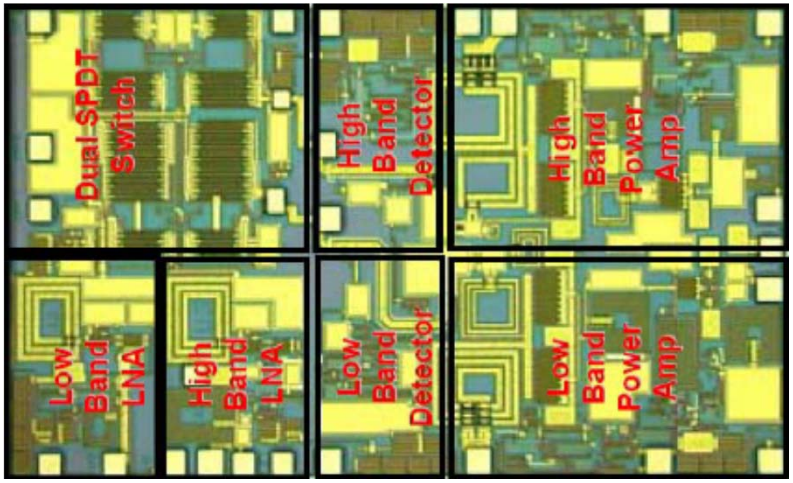




40 Gb/s modulator driver
Carroll, MTT-S 2002

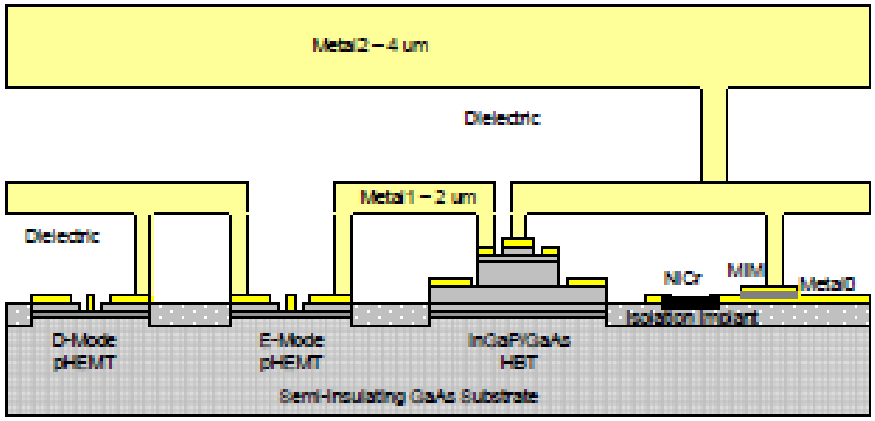


77 GHz transceiver
Tessmann, GaAs IC 1999



Single-chip WLAN MMIC, Morkner, RFIC 2007

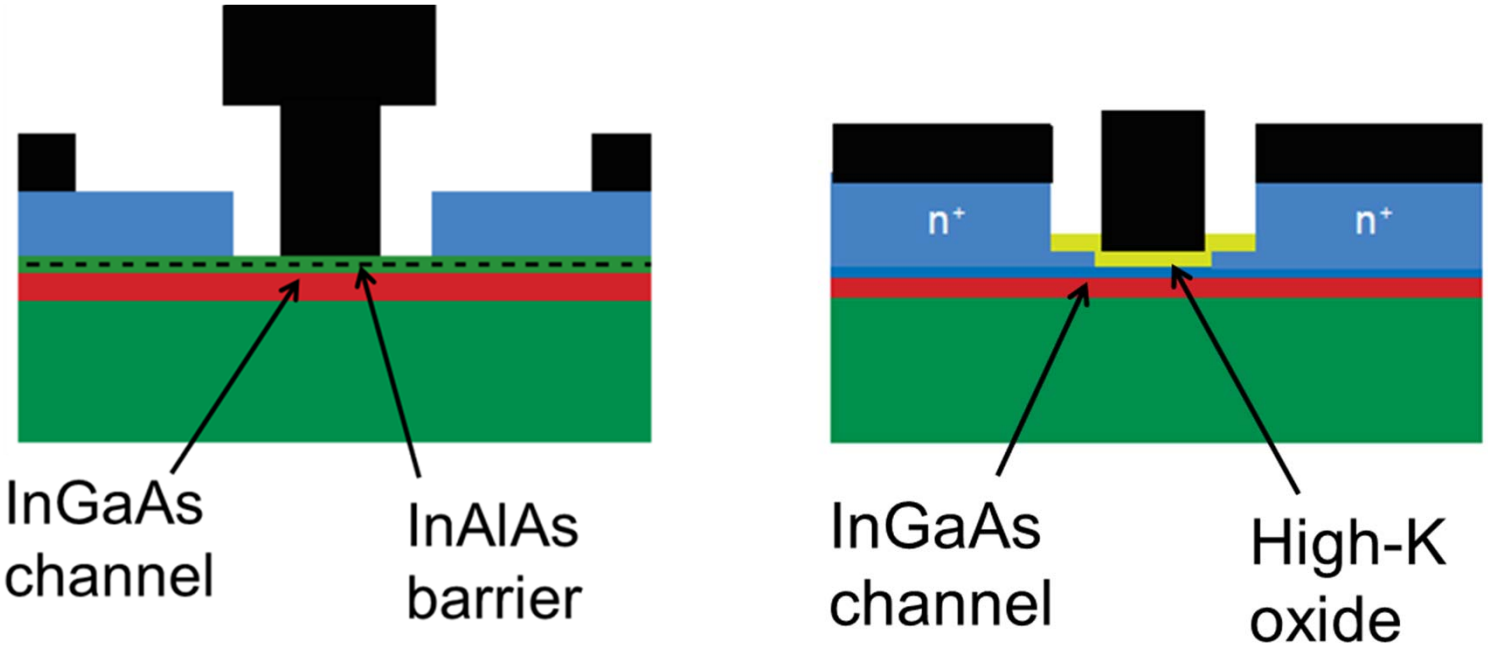
Bipolar/E-D PHEMT process



Henderson, Mantech 2007

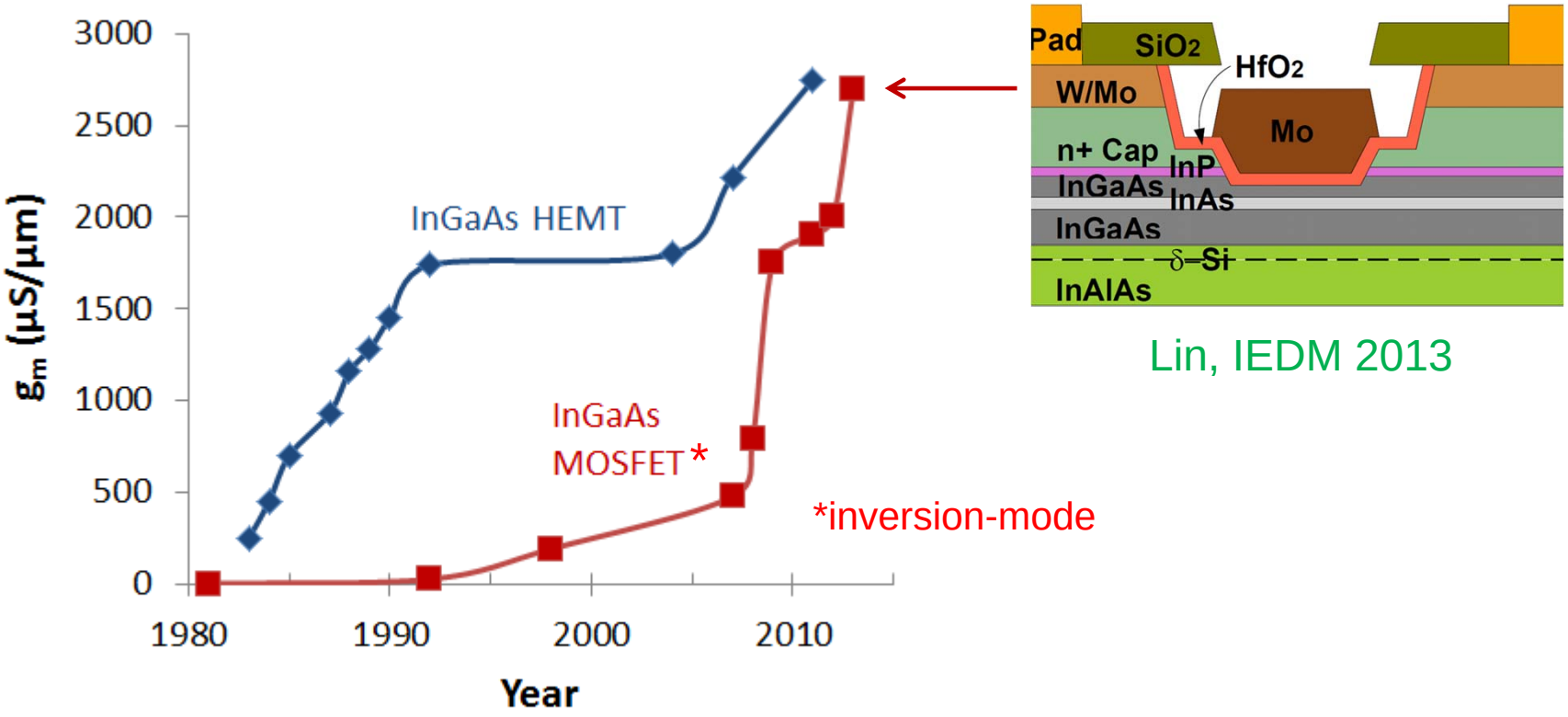
InGaAs HEMT vs. MOSFET

HEMT not suitable for logic: too much gate leakage current



MOSFET incorporates gate oxide → gate leakage suppressed

InGaAs MOSFETs vs. HEMTs: historical evolution



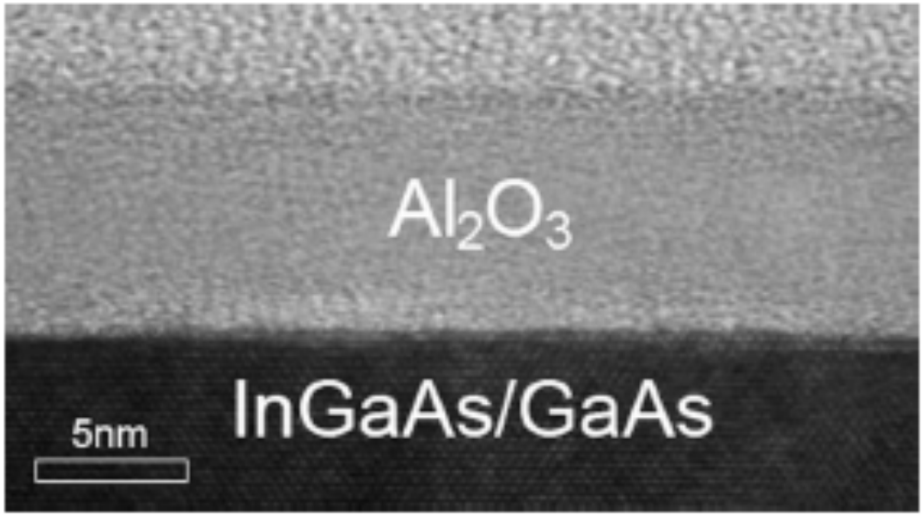
Lin, IEDM 2013

Progress reflects improvements in oxide/III-V interface

What made the difference?
Atomic Layer Deposition (ALD) of oxide

ALD eliminates surface oxides that pin Fermi level

→ "Self cleaning"

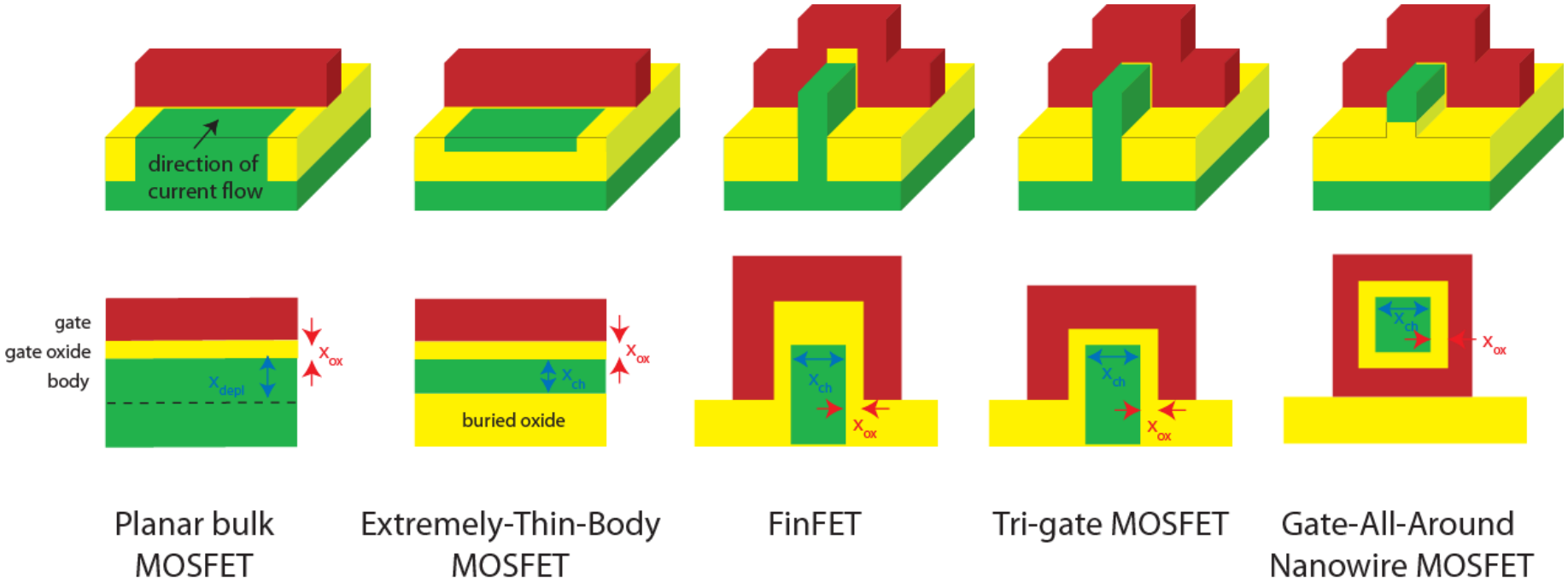


Huang, APL 2005

← Clean, smooth interface without surface oxides

- First observed with Al_2O_3, then with other high-K dielectrics
- First seen in GaAs, then in other III-Vs

InGaAs MOSFET: possible designs

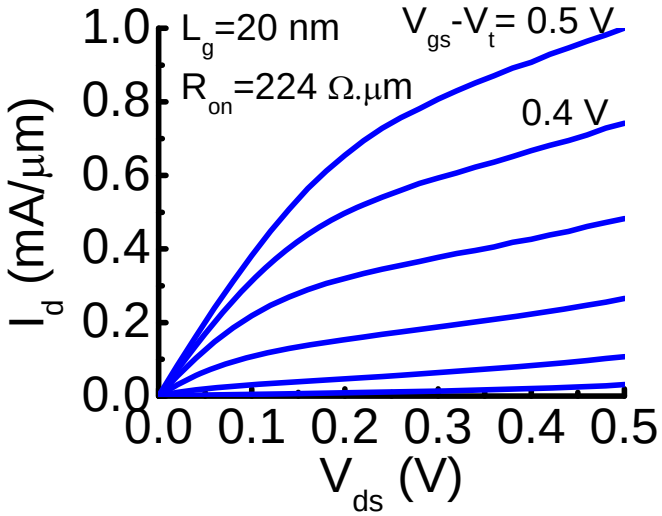


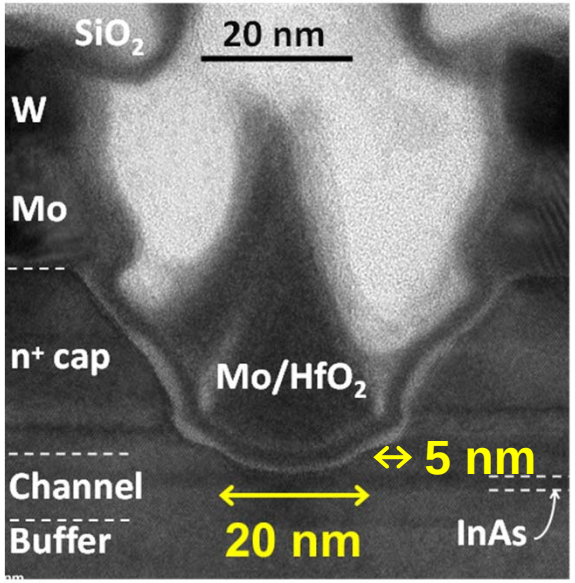
Planar bulk MOSFET | Extremely-Thin-Body MOSFET | FinFET | Tri-gate MOSFET | Gate-All-Around Nanowire MOSFET

Enhanced gate control → enhanced scalability

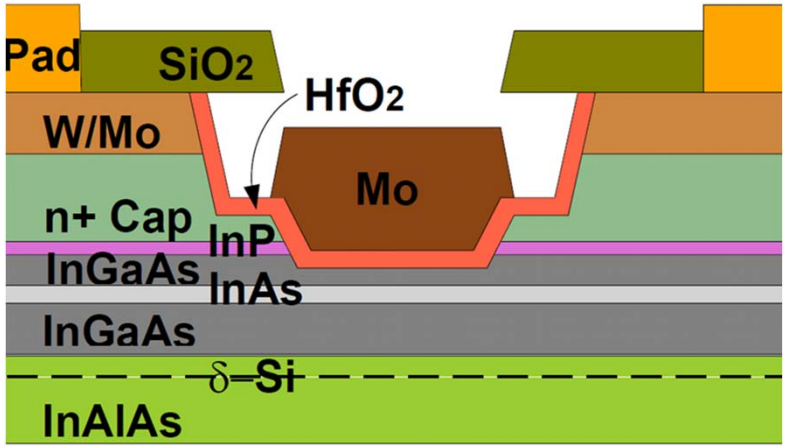
Self-Aligned InGaAs Quantum-Well MOSFETs

- Channel: $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ (1/2/5 nm)
- Gate oxide: HfO_2 (2.5 nm, EOT~0.5 nm)
- Self-aligned contacts (L_{side}~5 nm)
- Si compatible process (RIE, metals)

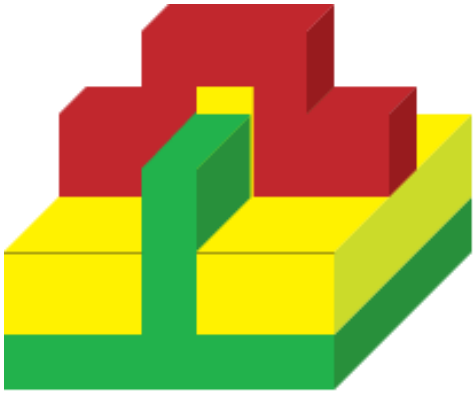




Lin, IEDM 2013

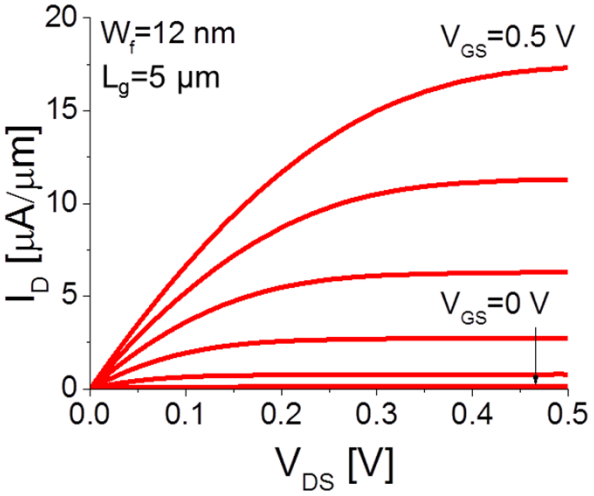


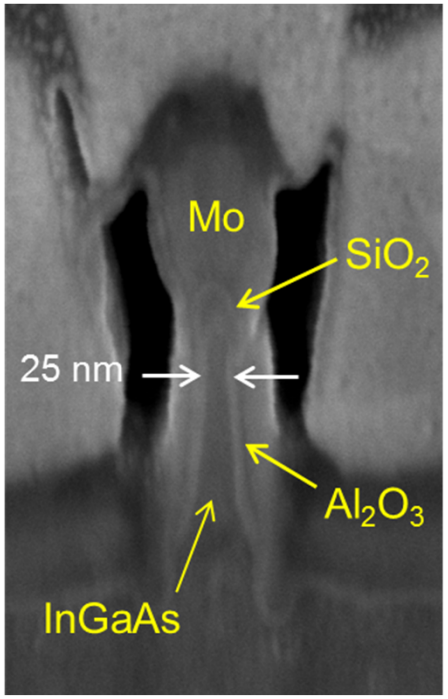
InGaAs double-gate Fin-MOSFET

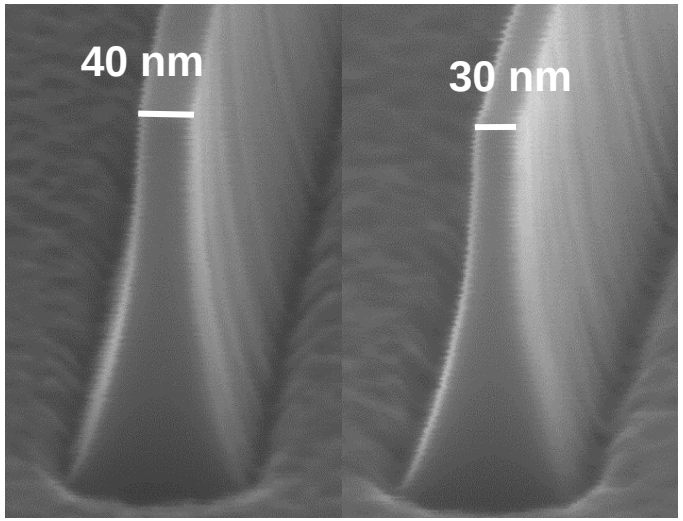


Key enabling technologies:

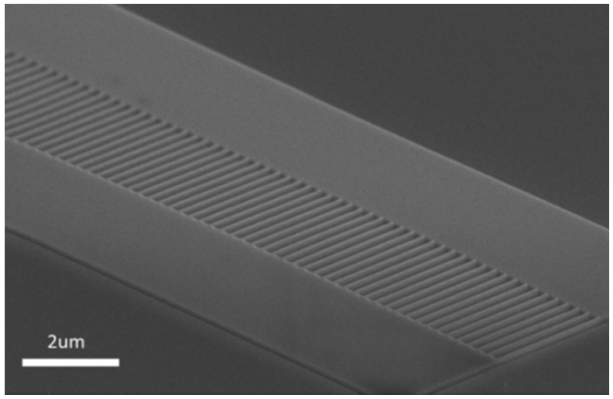
- $BCl_3/SiCl_4/Ar$ RIE
- digital etch





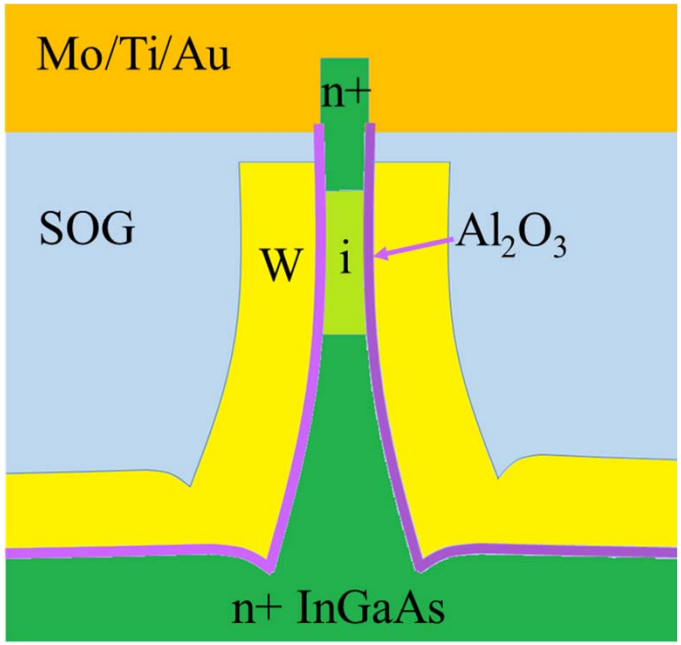


Zhao, EDL 2014

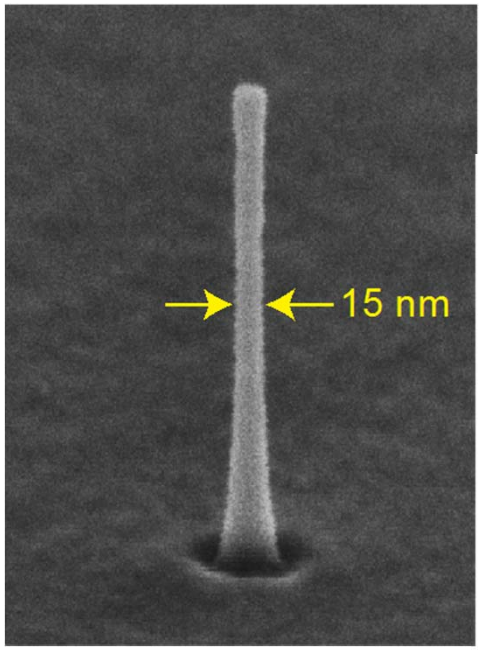


Vardi, DRC 2014

Vertical nanowire InGaAs MOSFETs

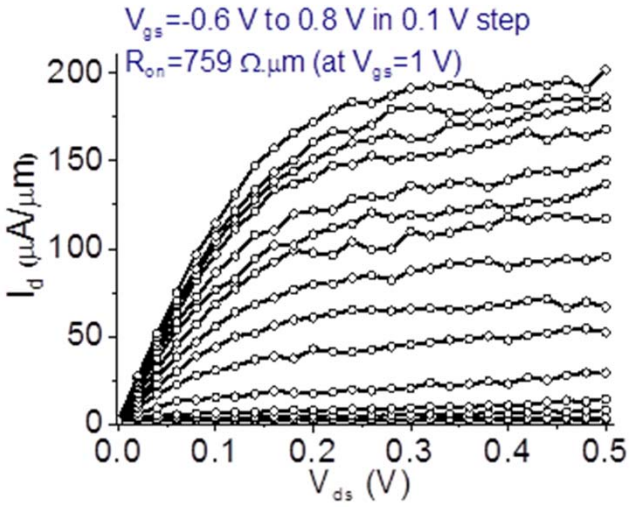


Zhao, IEDM 2013



Zhao, EDL 2014

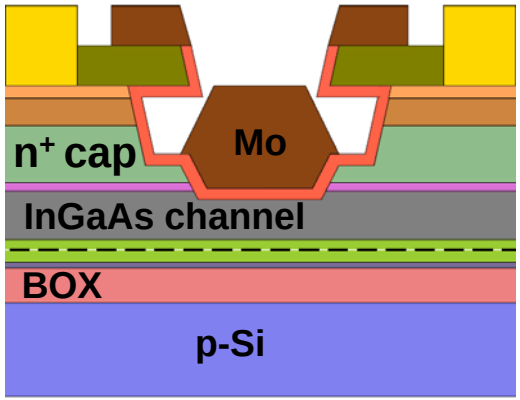
30 nm diameter
InGaAs NW-MOSFET

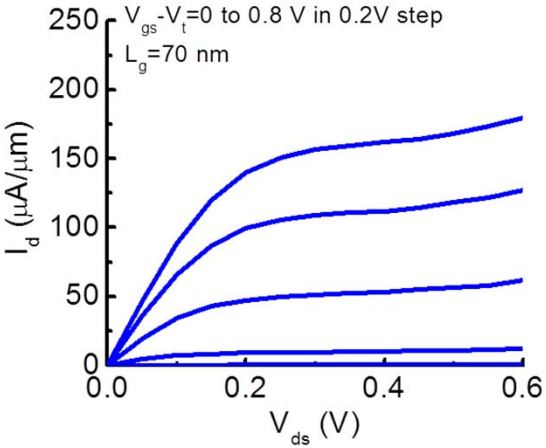


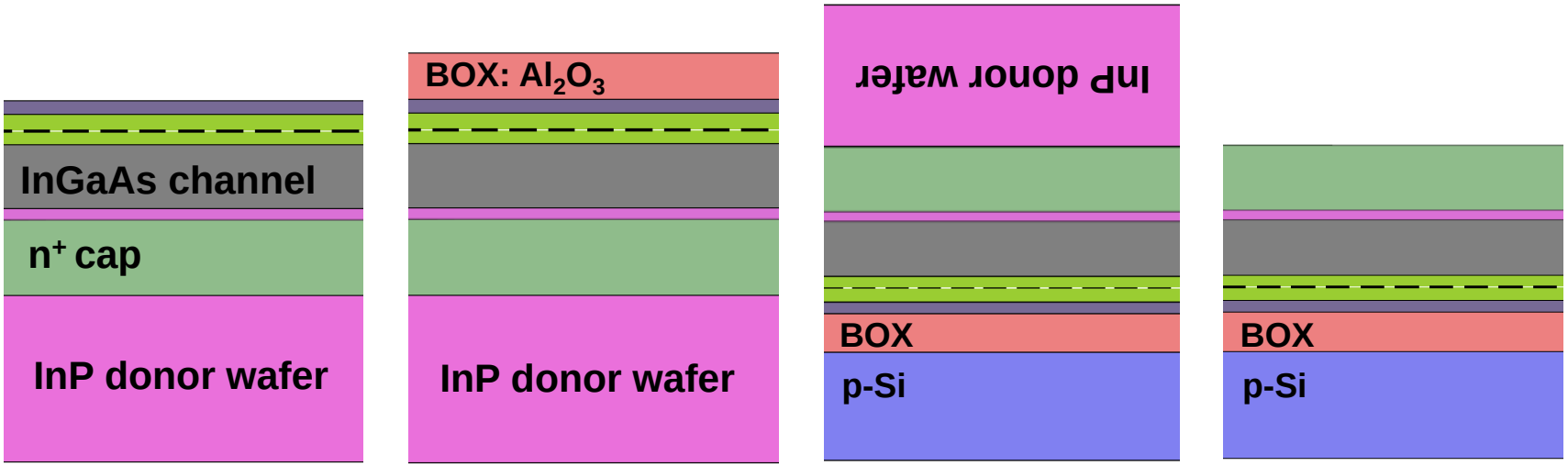
- Nanowire MOSFET: ultimate scalable transistor
- Vertical NW: uncouples footprint scaling from L_g scaling
- Top-down approach based on RIE + digital etch

Si integration: InGaAs SOI MOSFETs

III-V bonded SOI process of IBM Zurich:
Czornomaz, IEDM 2012







1. MBE growth
2. ALD Al_2O_3
3. Wafer bonding
4. InP etch back

Conclusions: exciting future for InGaAs electronics on Silicon

- Most promising material for ultra-high frequency and ultra-high speed applications

  → first THz transistor?

- Most promising material for n-MOSFET in a post-Si CMOS logic technology

  → first sub-10 nm CMOS logic?

- InGaAs + Si integration:

  → THz + CMOS + optics integrated systems?