A New Self-aligned Quantum-Well MOSFET Architecture Fabricated by a Scalable Tight-Pitch Process

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Abstract

We have developed a new III-V self-aligned Quantum-Well MOSFET (QW-MOSFET) architecture that features a scalable highly conducting ledge over the channel access region. The extensive use of RIE and digital etching techniques enables the precise design of the length and thickness of the ledge and allows the careful balancing of performance against short-channel effects. We demonstrate L_g=70 nm InAs MOSFETs with a ledge length of 5 nm that feature a record g_m of 2.7 mS/μm. Separately, devices with a ledge length of 70 nm yield a record ON-current of 410 μA/μm (V_{dd}=0.5 V and I_{off}=100 nA/μm). We also demonstrate working MOSFETs with L_g = 20 nm and a very tight metal contact spacing. Devices with a 5 nm ledge length reveal for the first time the existence of off-state leakage (GIDL) in III-V MOSFETs.

Introduction

InAs and InGaAs are promising channel material candidates for CMOS applications **[1-6]**. While great progress has taken place recently in demonstrating III-V MOSFETs, transistors displaying well-balanced electron transport, electrostatic integrity and parasitic resistance together with potential for high device density and tight pitch have yet to be demonstrated. We present here a wet-etch free process (no wet etching except for native oxide removal) for self-aligned InAs QW-MOSFETs that provides unprecedented control over the lateral dimensions of the gate access regions. We demonstrate devices with the highest transconductance and the highest ON-current of any III-V MOSFET to date.

Fabrication Process

Our new architecture leverages the self-aligned process presented in **[2]** but it incorporates new elements designed to implement highly conducting and tightly controlled channel access regions. In essence (**Fig. 1**), this is a gate-last process with the contacts formed first and the intrinsic region created by etching of the contact and cap layers. The gate is then nested in this opening in a self-aligned manner. In our new process, we use W above the Mo contact in order to prevent the oxidation of Mo during CVD SiO_2 deposition that in the past caused a deep lateral undercut during Mo RIE **[2]**.

The heart of our new process is a novel wet-etch free gate recess approach that provides unprecedented control over the vertical and lateral dimensions of the recess. This takes place in 3 steps (**Fig. 2**). The first step is time-controlled RIE of W/Mo sidewall **[7]** (**Fig. 2a**). Then the n^+ cap is removed by a low power Cl_2-based anisotropic RIE (**Fig. 2b**), instead of the common peroxide based wet etch that results in an isotropic undercut **[2-4].** It is observed that surface roughness strongly depends on RIE temperature. High temperature facilitates the removal of the etch byproducts from the surface, thus yielding a smooth surface. We used 130°C with an etch rate of ~11 nm/min. The final step is a digital etch that separates the etch chemistry into its two components: surface oxidation (in O_2 plasma) and oxide removal (in H_2SO_4), both of which are self-saturating (**Fig.2c**). It allows us to remove material in a controlled manner at an etch rate of ~0.9 nm per cycle. Our combined RIE+digital etch leaves the surface only slightly rougher than a wet etch, as shown in **Fig. 3**. This process results in a highly conducting "ledge" of precisely controlled length linking the access region of the device (**Fig. 2d**).

We demonstrate our new tight-pitch self-aligned process by fabricating surface-channel InAs MOSFETs with L_g=20-500 nm and L_{ledge} of 5 nm (**Figs. 4a, 4b**) and 70 nm (**Fig. 4c, 4d).** The layer structure of the ledge consists of ~5 nm n^+ InP, 3 nm n^+ InAlAs and 3 nm undoped InP etch stop and has a total electron concentration of ~ 2 x 10^{12} cm^{-2}.

- W/Mo contact and CVD SiO_2 hard mask
- Gate Ebeam-lithography
- **Gate recess 1**: SiO_2/W/Mo etch/pull-in
- Mesa isolation
- **Gate recess 2**: Dry recess of III-V
- Damage annealing **[8]**
- **Gate recess 3**: Digital etch
- H_2SO_4 cleaning
- ALD gate dielectric deposition
- Mo gate evaporation
- Gate head photo and patterning
- Pad formation

Fig. 1 Process flow for tight-pitch QW-MOSFETs.

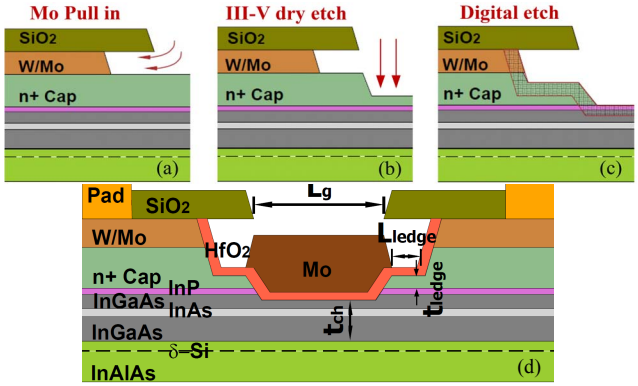

Fig. 2 Illustration of 3-step gate recess process: (a) W/Mo pull in, (b) time-controlled Cl_2 dry etch, (c) cap and barrier digital etch. (d) Cross section schematic of complete device structure.

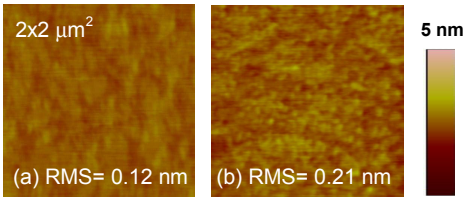

Fig. 3 AFM of InGaAs surface after (a) cap wet etch and (b) cap dry etch (~ 20 nm) + 4 cycle digital etch.

RIE damage annealing is performed before ALD gate oxide deposition **[8]**. For gate oxide, we use 2.5 nm HfO_2 directly on $In_{0.7}Ga_{0.3}As$. The channel is comprised of 1/2/5 nm $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ from top to bottom. The gate is dry-etched Mo. Because the process is wet-etch free and lift-off free, it is promising for aggressive footprint and tight pitch scaling. **Fig. 4e** shows TEM of a fully working device with L_g=20 nm and L_{ledge}=5 nm.

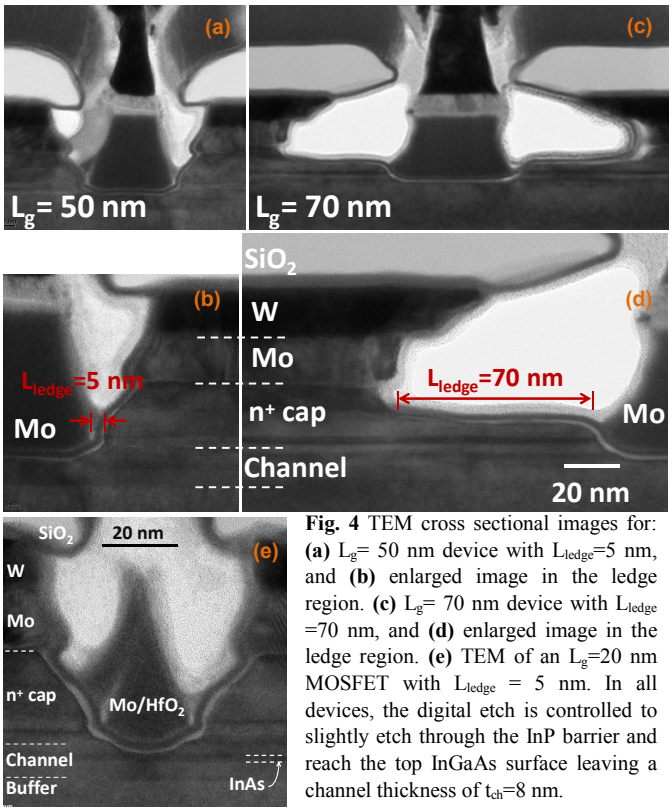

Fig. 4 TEM cross sectional images for: **(a)** L_g= 50 nm device with L_{ledge}=5 nm, and **(b)** enlarged image in the ledge region. **(c)** L_g= 70 nm device with L_{ledge} =70 nm, and **(d)** enlarged image in the ledge region. **(e)** TEM of an L_g=20 nm MOSFET with L_{ledge} = 5 nm. In all devices, the digital etch is controlled to slightly etch through the InP barrier and reach the top InGaAs surface leaving a channel thickness of t_{ch}=8 nm.

Results and discussion

Output characteristics of typical L_g=70 nm devices with both ledge lengths are shown in **Fig. 5**. Both devices exhibit excellent current saturation. The transconductance (g_m) of both L_g=70 nm devices is shown in **Fig. 6**. Thanks to the very low R_{sd}, the L_{ledge}=5 nm device demonstrates a record $g_{m,max}$=2.7 mS/μm at V_{ds}=0.5 V. This is the highest of any III-V MOSFET and matches the best HEMTs **[9]**. The L_{ledge}=70 nm device still exhibits an excellent $g_{m,max}$=1.9 mS/μm. The subthreshold characteristics are shown in **Fig. 7**. The long-ledge device features excellent short-channel effects with a minimum S=90 mV/dec at V_{ds}= 50 mV and 94 mV/dec at 0.5 V. This is the lowest S demonstrated to date at this gate length among III-V MOSFETs **[2]**. The short-ledge design leads to somewhat poorer short-channel effects. While I_g for both devices is very low (<3x10^{-12} A/μm), off-state leakage is higher in the short-ledge device (discussed below). Output characteristic of a fully functional L_g=20 nm device with L_{ledge}=5 nm are shown in **Fig. 8**. To our knowledge, this is the smallest III-V MOSFET demonstrated so far.

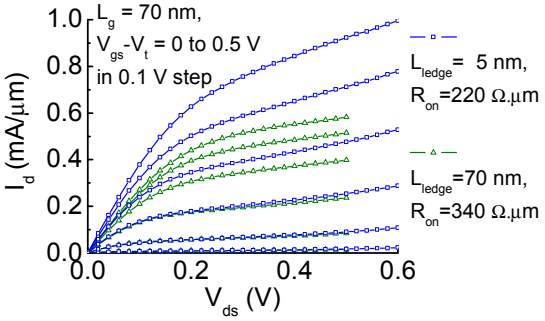

Fig. 5 L_g=70 nm MOSFET output characteristics of L_{ledge}=5 and L_{ledge} =70 nm devices.

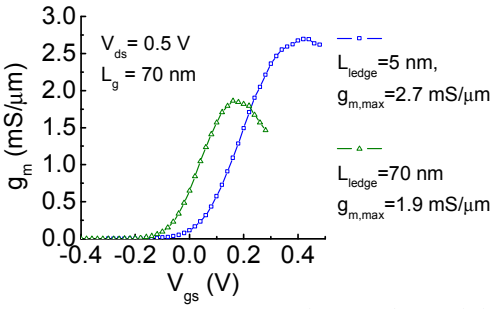

Fig. 6 L_g=70 nm MOSFET transconductance characteristics for L_{ledge}=5 and L_{ledge}=70 nm.

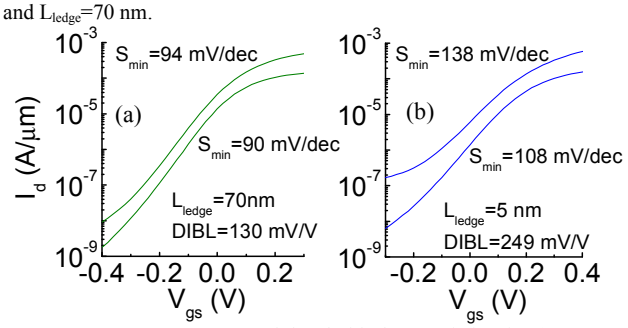

Fig. 7 L_g=70 nm MOSFET subthreshold characteristics for (a) L_{ledge}=70 and (b) L_{ledge} =5 nm at V_{ds} of 50 mV and 0.5 V. V_t at 50 mV are (a) -0.13 V and (b) -0.04 V. Gate leakage for both devices is below 3x10^{-12} A/μm across the whole gate voltage range.

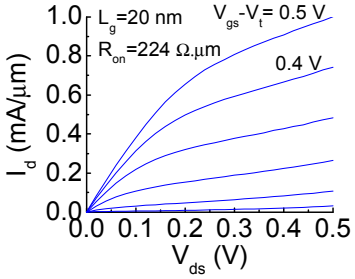

Fig. 8 Output characteristic of a L_g=20 nm MOSFET with L_{ledge}=5 nm.

The length of the ledge has a large impact on the parasitic resistance of the device. As L_{ledge} decreases, R_{sd} decreases from 302 Ω.µm to 206 Ω.µm (**Fig. 9**). R_{sd}=206 Ω.µm represents one of the lowest values ever demonstrated on III-V FETs of any kind. Inset of **Fig. 9** and **Table I** show the decomposition of the R_s components for both types of devices. Further reduction of R_s is expected by reducing the InP barrier thickness between the n^+ cap and the channel.

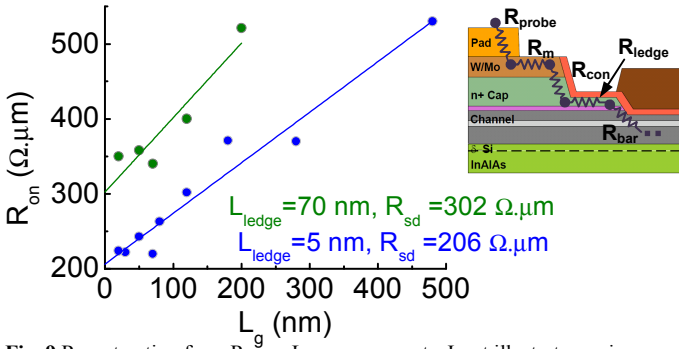

Fig. 9 R_{sd} extraction from R_{on} *vs.* L_g measurements. Inset illustrates main components of R_s.

		L_{ledge}	
Label	Resistance component	5 nm	70 nm
R_{probe}	Probing to Au pad	5	5
R_m	Metal lateral resistance	5	5
R_{con}	Mo/cap contact resistance	50	50
R_{ledge}	Ledge lateral resistance	3	51
R_{bar}	Remaining barrier to channel	40	40
R_s	Total source resistance	103	151

Table I: Estimated values of main R_s components in units of Ω.µm.

Benchmarking with recently published III-V MOSFETs and HEMTs **[2-6, 9-16]** is shown in **Figs. 10,11.** I_{on} is defined at constant I_{off}=100 nA/µm and V_{dd}=0.5 V (**Fig. 5**). The L_{ledge}=70 nm device shows the highest I_{on} ever demonstrated in a III-V MOSFET and closely approaches that of HEMTs. The L_{ledge}=5 nm device shows lower I_{on} because of the degradation of S at high V_{ds}. Thus, at shorter L_g, I_{off} of 100 nA/µm is not reached. A diagnosis and a solution to this problem are discussed below. The trade-off between transport and short-channel effects is clearly seen in **Fig. 12**. The devices demonstrated here offer the best balance between g_m and S of any III-V MOSFET technology demonstrated so far.

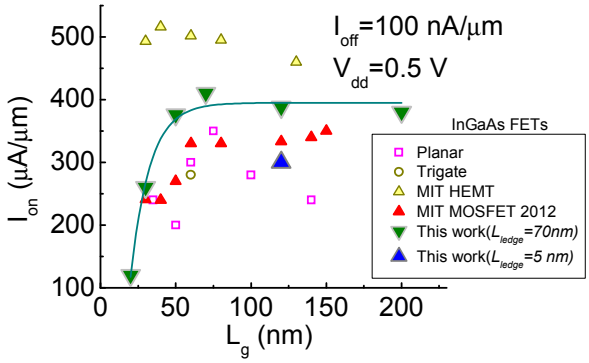

Fig.10 Benchmarking of I_{on} *vs.* L_g for this work and recently published III-V FETs. **[2-6, 9-16]**

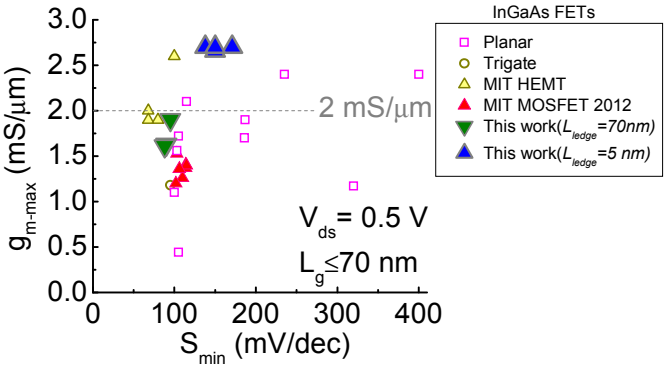

Fig.11 $g_{m,max}$ *vs.* S_{min} for recently published III-V FETs with L_g<70 nm. **[2-6, 9-16]**

Our shortest ledge design exhibits significant degradation of S under high V_{ds}. This is unrelated to gate length as shown in the characteristics of long L_g devices (**Figs. 12a, 12b**). Measurements at lower temperatures (**Figs. 12 c, 12d**) reveal a characteristic GIDL (Gate-Induced Drain Leakage) signature in the off-state I_d. At 77 K, I_d depends only on V_{dg} (**Fig. 13**). The temperature dependence that is observed comes from that of the bandgap (inset of **Fig. 13**). TCAD simulations in **Fig. 14** show band-to-band tunneling (BTBT) at the corner of the gate edge indeed causing appreciable carrier generation at V_{ds}= 0.5 V and V_{gs} - V_t = -0.1 V. BTBT takes place between the E_v of the top InGaAs sub-channel and E_c of the bottom InGaAs subchannel. We believe this is the first unambiguous observation of GIDL in III-V MOSFETs. GIDL can be mitigated by widening the channel bandgap by making it thinner and using a lower InAs composition, or redesigning the ledge to reduce the E-field at the gate edge.

Fig. 15 shows S against I_d at various temperatures for L_{ledge}=5 nm device. At 300 K and low V_{ds}, D_{it} results in S degradation, and n=1.26 (n=S_{min}/S_{ideal}). At 150 K, almost all D_{it} become frozen. As a result, at both 77 K and 150 K, subthreshold swings that approach ideal values (n =1.06) across many orders of magnitude of I_d are observed.

Conclusions

In this work, we demonstrate a novel self-aligned tight-pitch III-V MOSFET architecture with high scaling potential. A precisely controlled conducting ledge fabricated by a wet-etch free and lift-off free process enables low conductivity access regions. By varying the ledge length we can explore the balance of performance *vs.* short-channel effects. We demonstrate a fully working L_g=20 nm device with contact-gate spacing of 5 nm. The short-ledge devices demonstrate record g_m and very low R_{sd}. Long-ledge devices have outstanding short-channel effects and high I_{on} at fixed I_{off}. GIDL is observed in the short-ledge devices. Well-designed access regions are imperative in future III-V logic MOSFETs.

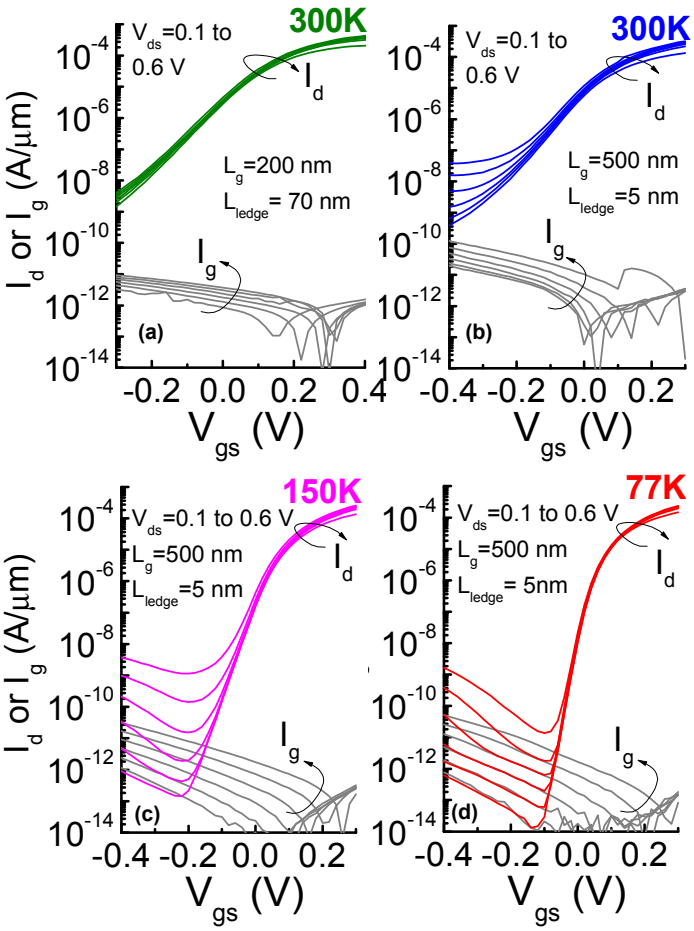

Fig. 12 Subthreshold characteristics of long-channel devices: (a) with long ledge (L_g=200 nm, L_{ledge}=70 nm) at 300 K; (b-d) with short ledge (L_g=500 nm, L_{ledge}=5 nm) at 300 K, 150 K, and 77 K.

$$J_{b2b} \propto \frac{qm^*}{2\pi^2\hbar^2}\exp\left(-\frac{\pi\sqrt{m^* E_g^3}}{2\sqrt{2}\hbar q|\vec{E}|}\right)$$

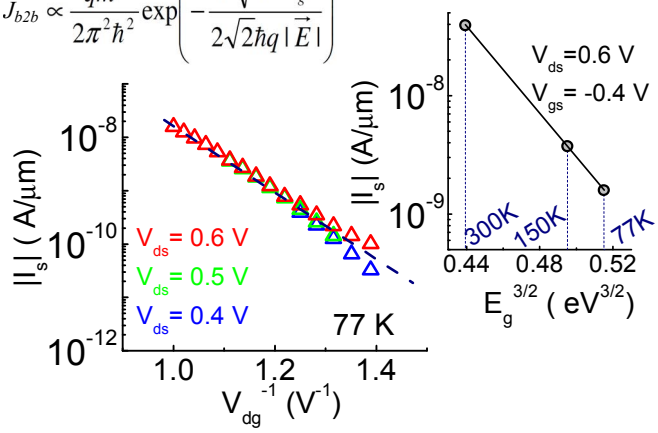

Fig. 13 I_s *vs.* V_{dg}^{-1} for short-ledge device at 77 K is consistent with BTBT. Inset: Low-temperature dependence of I_s in the off state is consistent with the temperature dependence of the $In_{0.7}Ga_{0.3}As$ bandgap and supports the BTBT hypothesis.

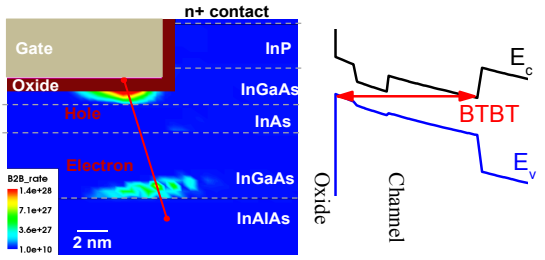

Fig. 14 BTBT generation rate ($cm^{-3}s^{-1}$) contours by Sentaurus simulation using Poisson and BTBT model under the gate edge in short L_{ledge} devices. Red line indicates the tunneling path. Hole generation mainly happens at the top InGaAs subchannel beneath the gate while electrons are generated at the bottom InGaAs subchannel. On the right: schematic of band structure along the tunneling path.

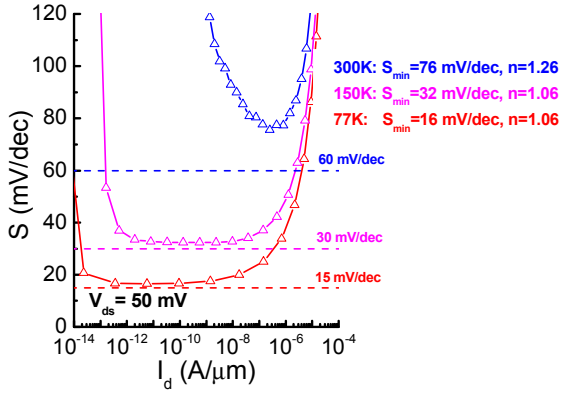

Fig. 15 Subthreshold swing of L_g=500 nm MOSFETs with L_{ledge} =5 nm *vs.* I_d at various temperatures. n=S_{min}/S_{ideal}. Almost ideal S indicates traps are frozen under T= 150 K.

Acknowledgements

This work is sponsored by FCRP-MSD Center, Intel, NSF Award 0939514 (E3S STC), MIT SMA and SMART programs. Device fabrication was carried out at the Microsystems Technology Laboratories (MTL) and SEBL of MIT. MBE growth is provided by IntelliEpi.

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