InGaAs MOSFETs for CMOS:

Recent Advances in Process Technology

J. A. del Alamo, D. Antoniadis, A. Guo, D.-H. Kim[1],
T.-W. Kim[2], J. Lin, W. Lu, A. Vardi and X. Zhao

Microsystems Technology Laboratories, MIT
[1]Global Foundries
[2]Sematech

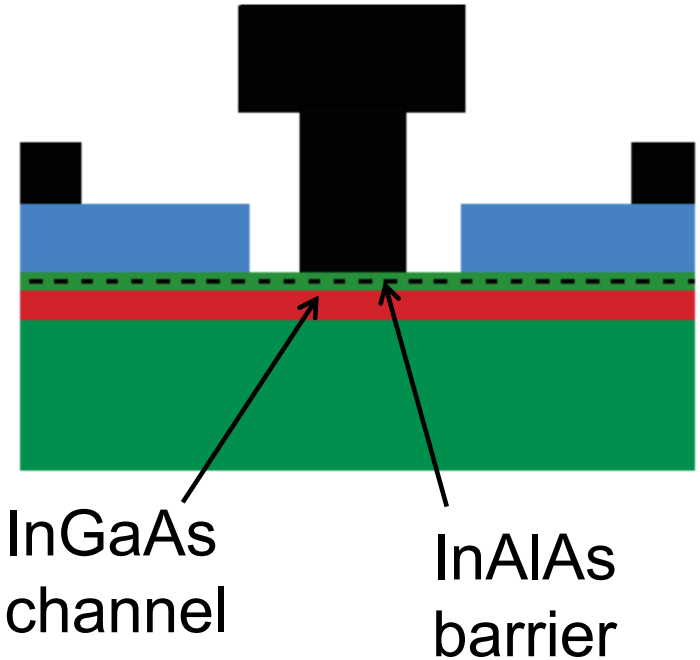
International Electron Devices Meeting 2013

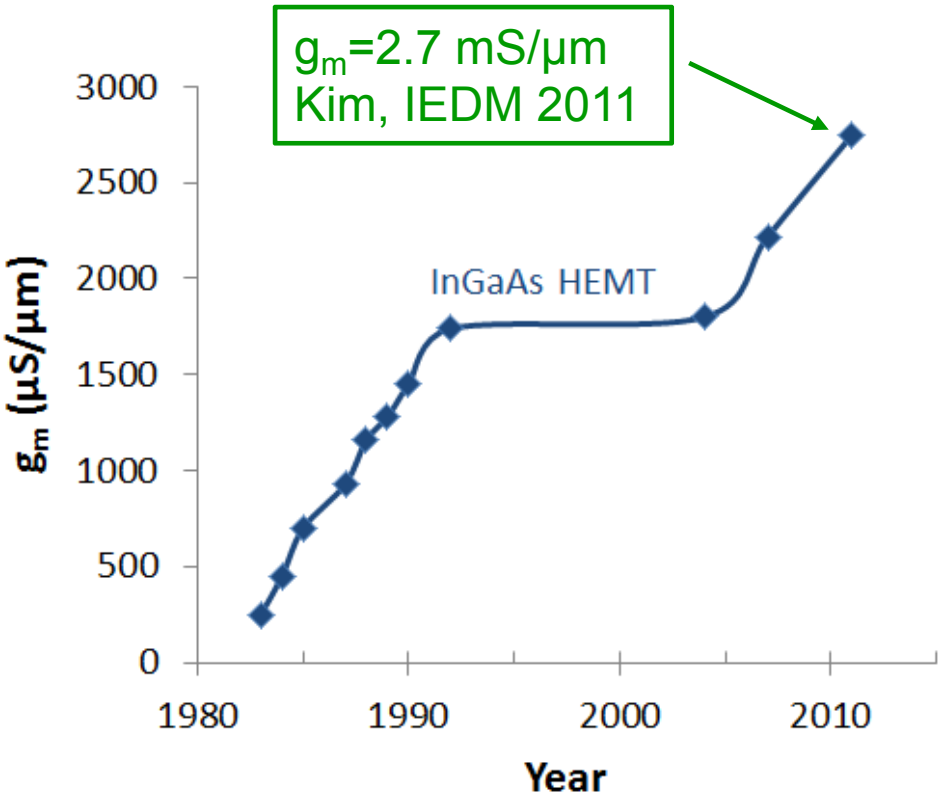
Washington D.C., December 9, 2013

Acknowledgements:

- Sponsors: Intel, FCRP-MSD, Sematech, NSF, SMA, MIT-Technion
- Labs at MIT: MTL, NSL, SEBL

InGaAs
High Electron Mobility Transistors

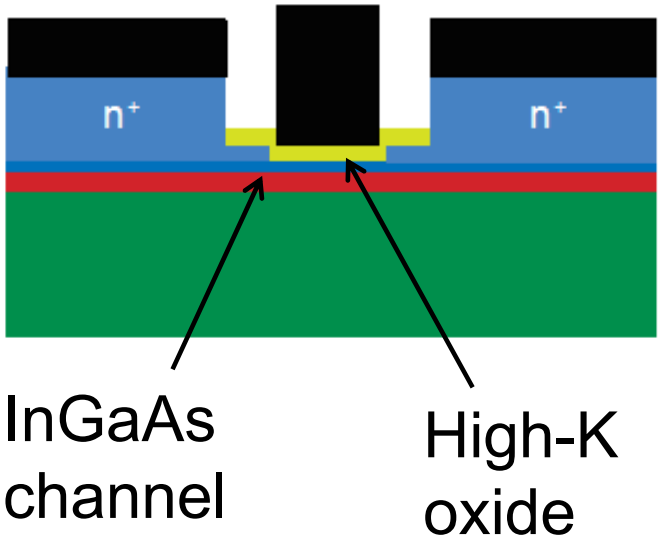


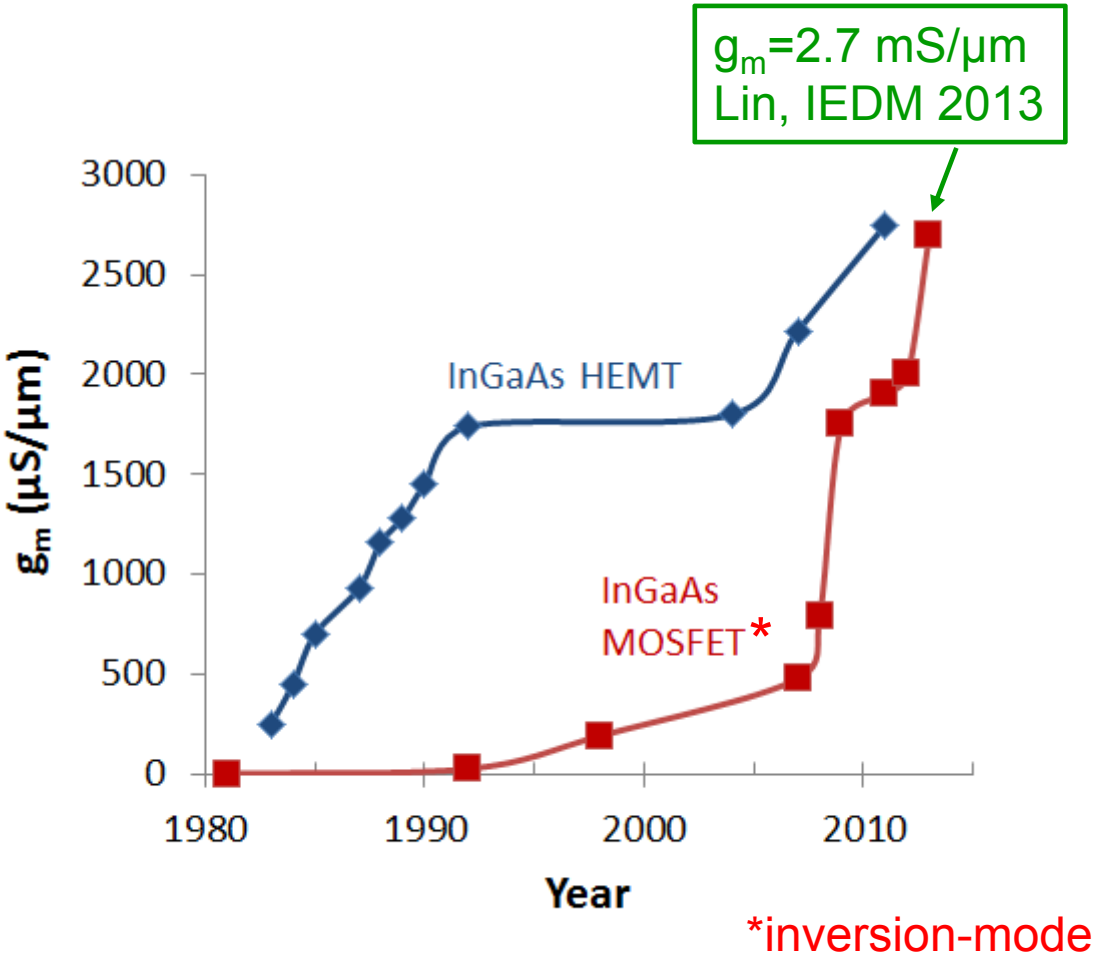


Main attractions of InGaAs:

- μ_e = 6,000 - 30,000 $cm^2/V.s$ @ 300K
- v_{inj} = 2.5 - 3.7x10^7 cm/s @ 300 K

InGaAs MOSFETs



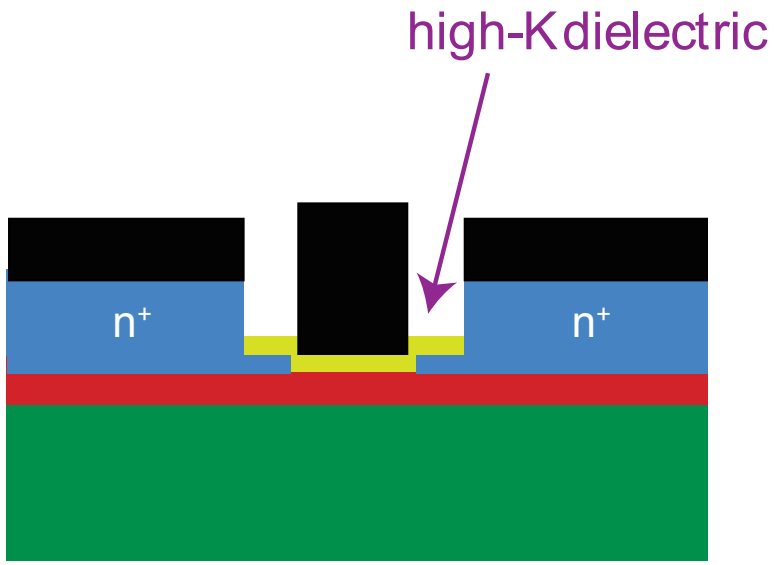


Extraordinary recent progress of InGaAs MOSFETs

Technology issue #1: MOS gate stack

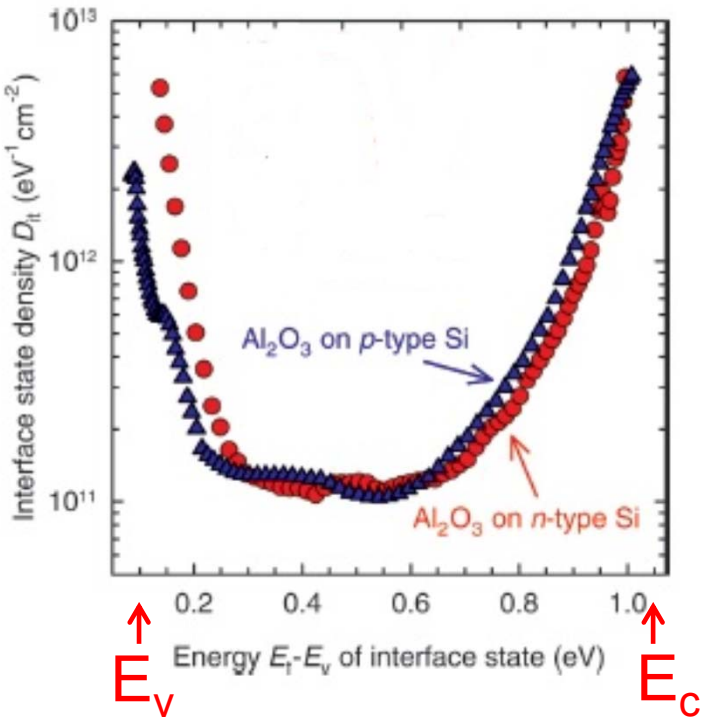
Challenge: metal/high-K oxide gate stack

- Fabricated through *ex-situ* process
- Very thin barrier (EOT ~ 0.5 nm)
- Low gate leakage (I_G<1 A/cm^2 at V_{GS}=0.5 V)
- Low D_{it} (<3x10^{12} eV^{-1}.cm^{-2} in top ~0.3 eV of bandgap and inside CB)
- Reliable



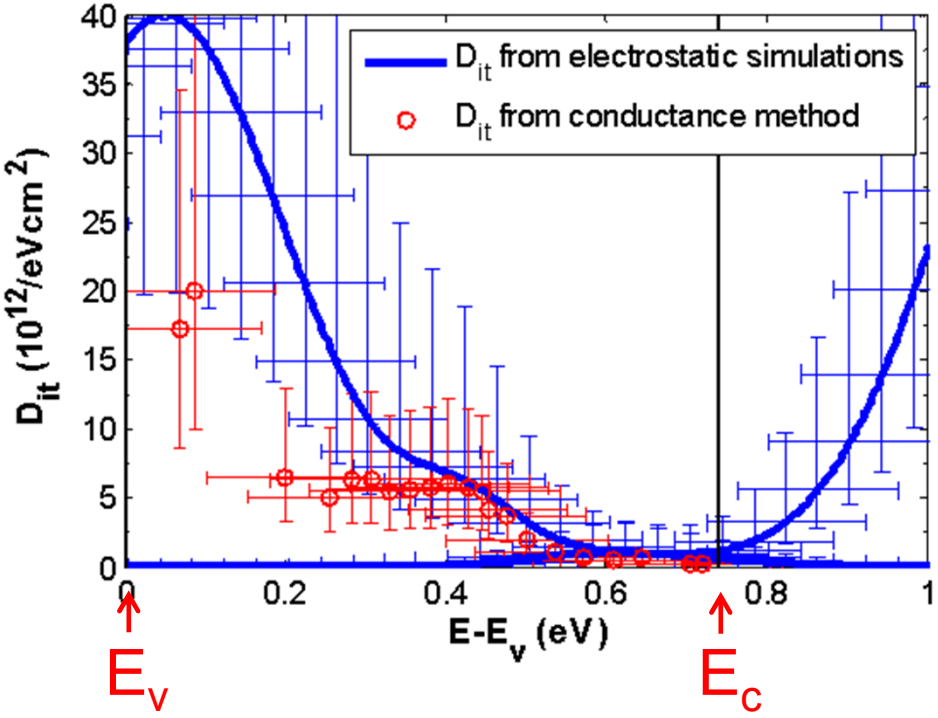
Interface quality: Al_2O_3 / InGaAs vs. Al_2O_3 / Si

Al_2O_3/Si



Werner, JAP 2011

Al_2O_3/InGaAs



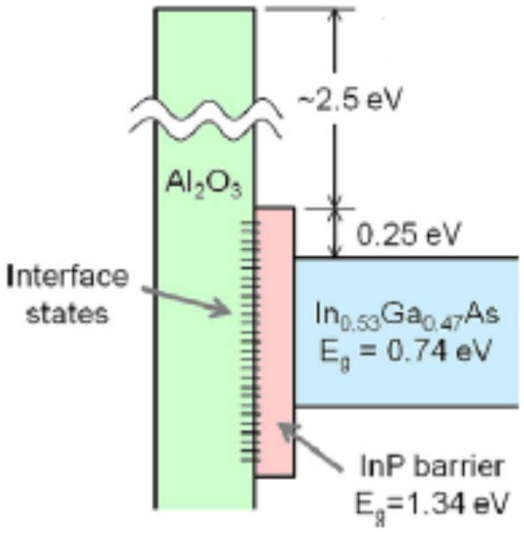
Brammertz, APL 2009

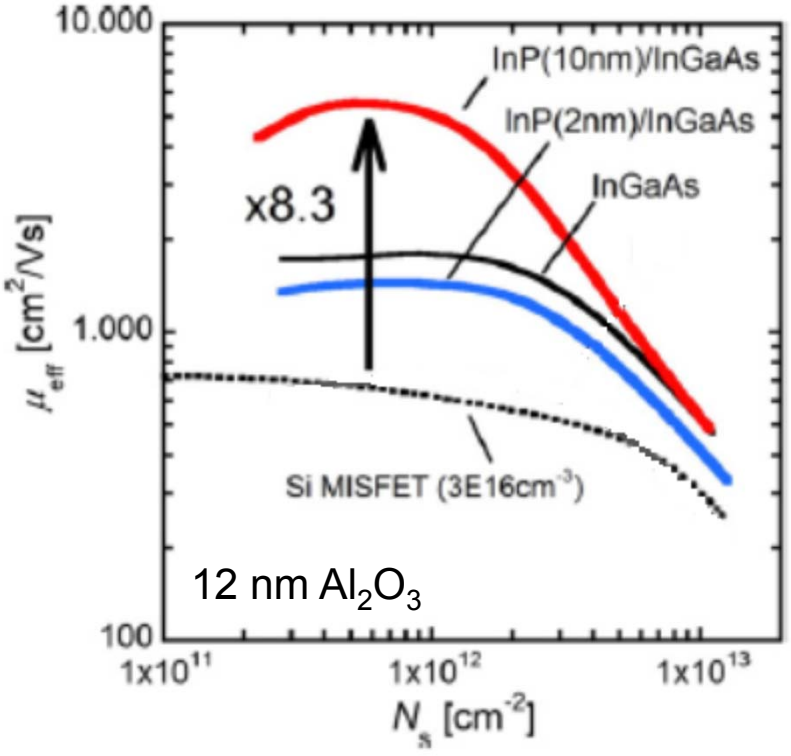
Close to E_c, Al_2O_3/InGaAs comparable D_{it} to Al_2O_3/Si interface

Buried-channel *vs.* surface channel?

Classic trade-off:

- Surface channel: high scalability but low mobility (μ_e<2,000 cm^2/V.s)
- Buried channel: high mobility but high EOT and t_{barr} ↓ → μ_e ↓



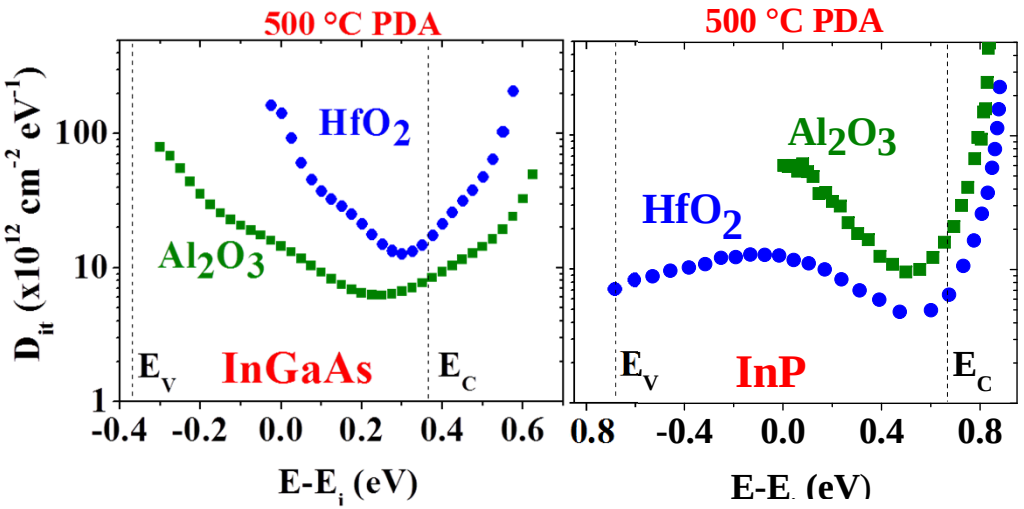


InP good choice for barrier:

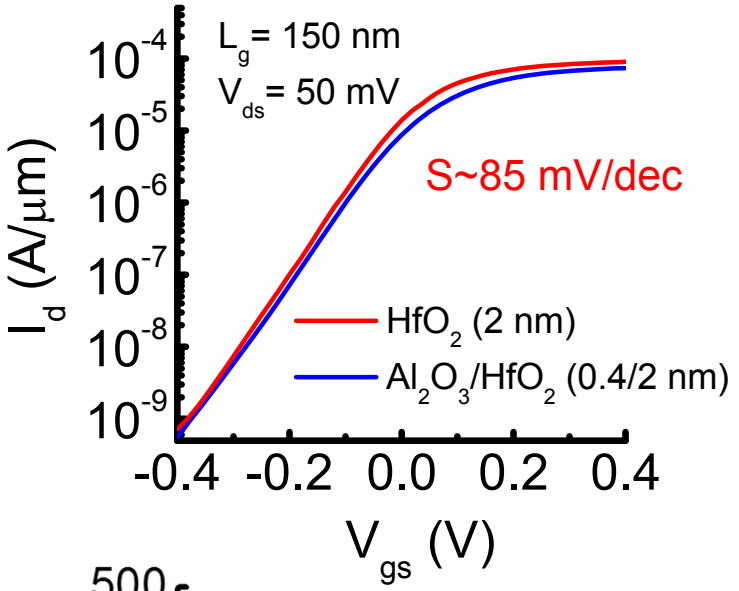
→ wide E_g, lattice matched to $In_{0.53}Ga_{0.47}As$

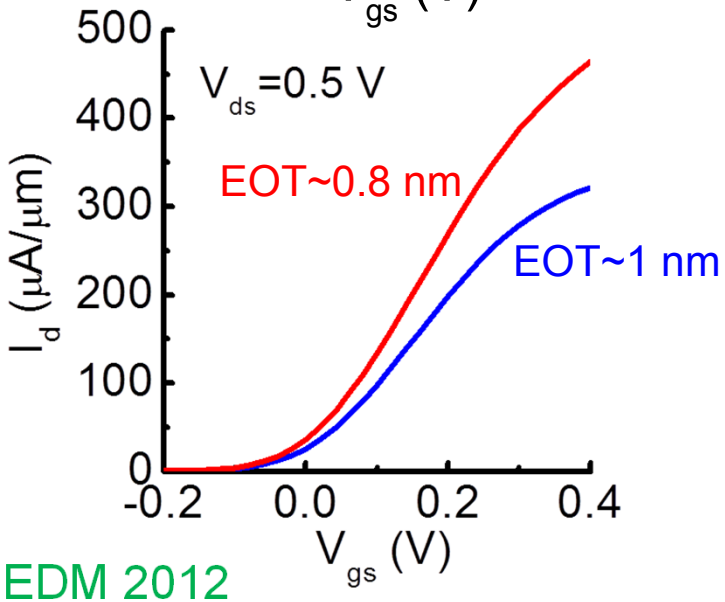
Urabe, ME 2011

HfO_2 vs. Al_2O_3 in buried-channel MOSFETs



Galatage - UT Dallas, 2012



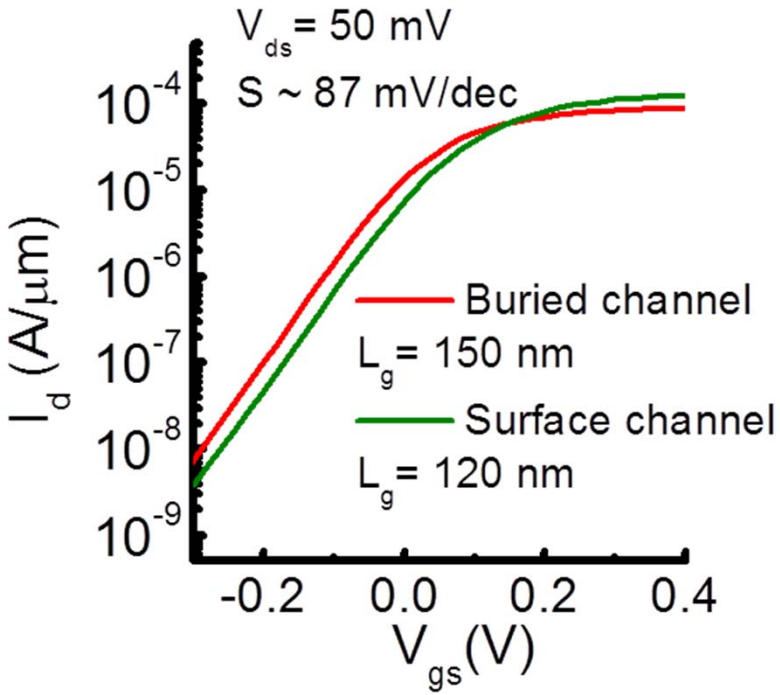


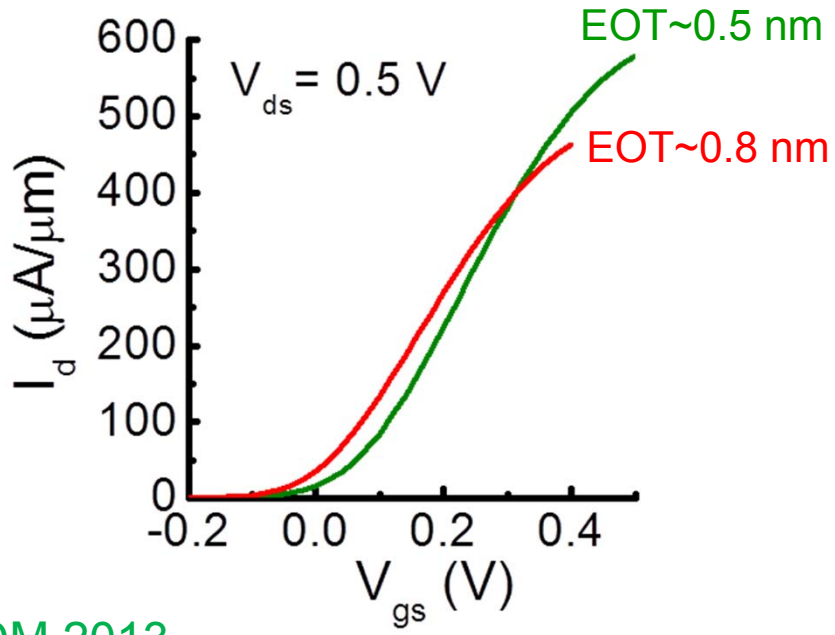
Lin, IEDM 2012

HfO_2 (2 nm) directly on InP (1 nm):

- Low D_{it} close to E_c
- Steep subthreshold swing
- Low I_{off} (nA/μm range)

HfO_2 in surface-channel MOSFETs

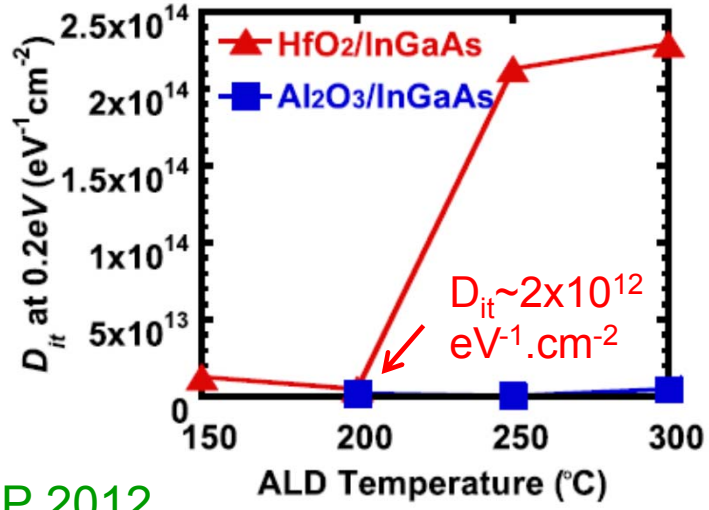




Lin, IEDM 2013

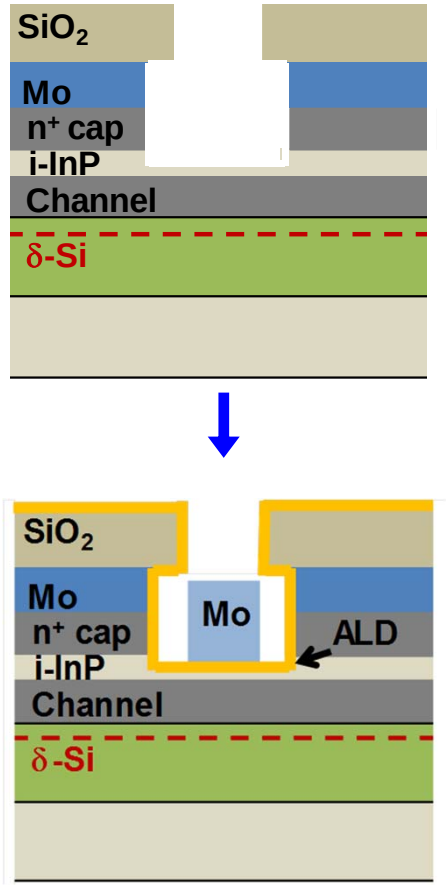
HfO_2 (2.5 nm) directly on InGaAs:

- Comparable S as buried-channel device
- EOT ↓ → I_d ↑
- Low ALD temperature key

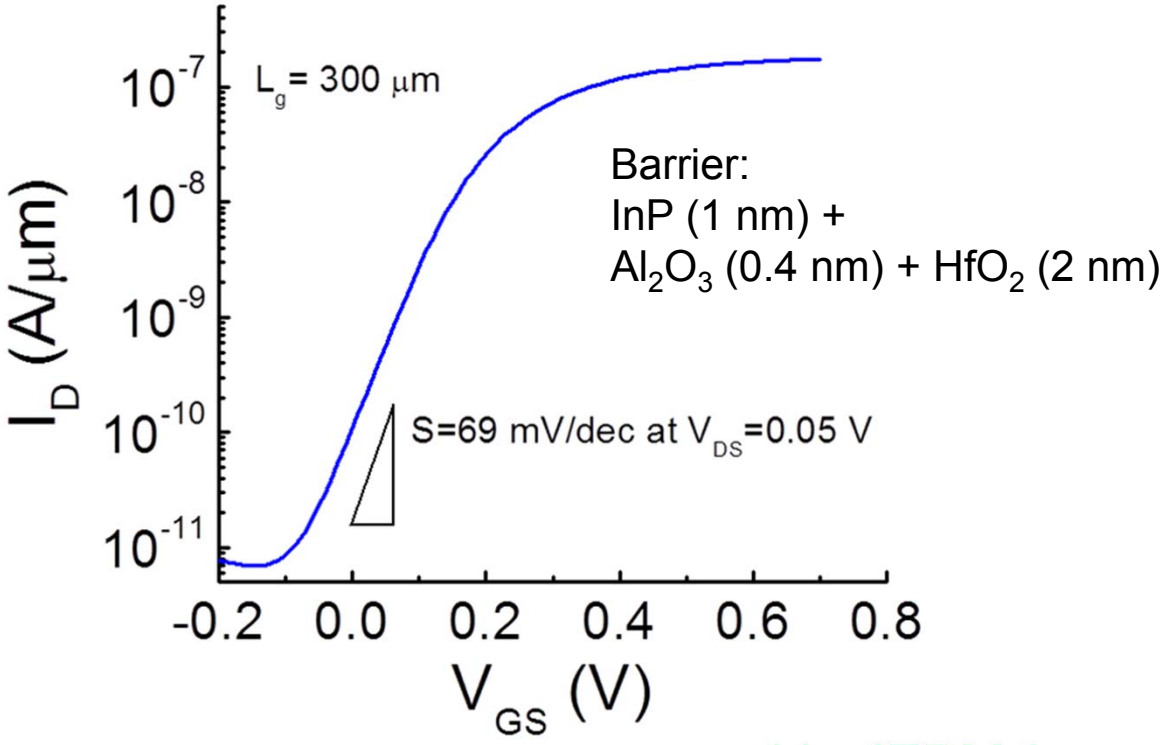


Suzuki, JAP 2012

Pristine interface for high MOS quality



Semiconductor surface exposed immediately before MOS formation



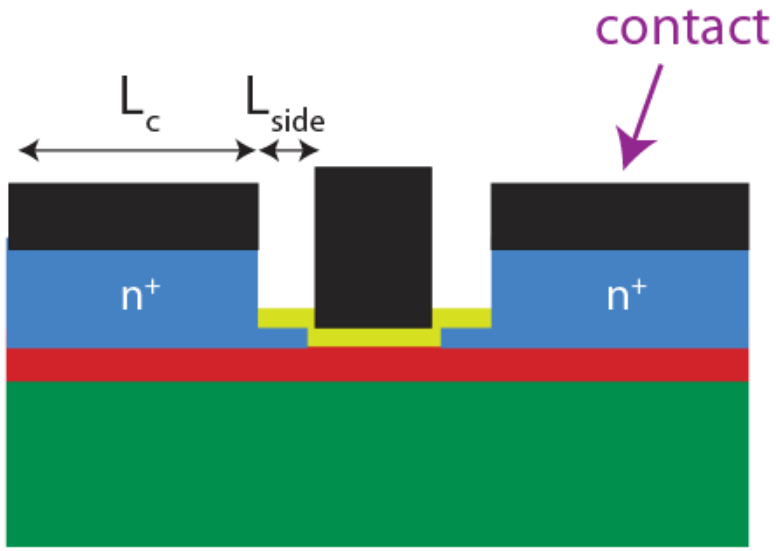
Lin, IEDM 2012

- S = 69 mV/dec at V_{DS} = 50 mV
- Close to lowest S reported in any III-V MOSFET: 66 mV/dec [Radosavljevic, IEDM 2011]

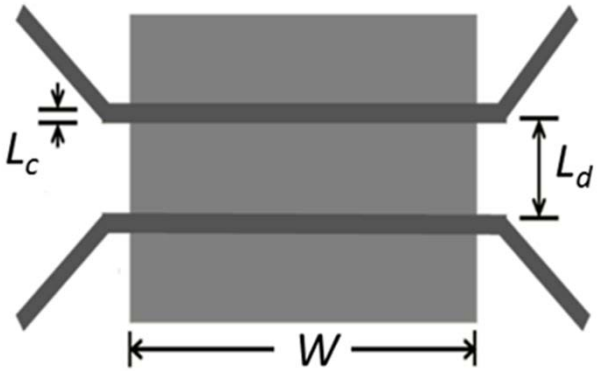
Technology issue #2: ohmic contacts

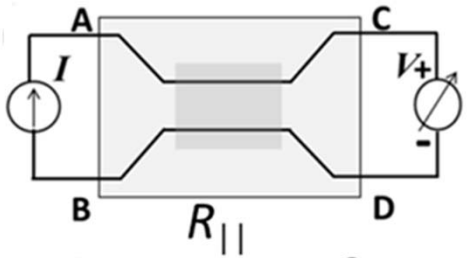
Challenge: nanometer-scale ohmic contacts with low R_c

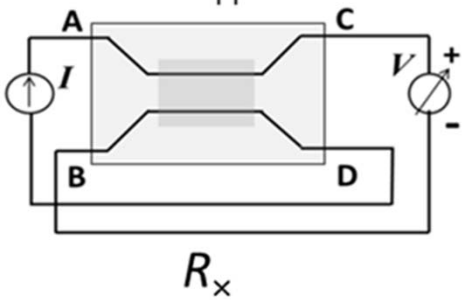
- Tiny (L_c < 30 nm)
- Low contact resistance (R_c < 50 Ω.μm)
- Self-aligned to gate (L_{side} < 10 nm)

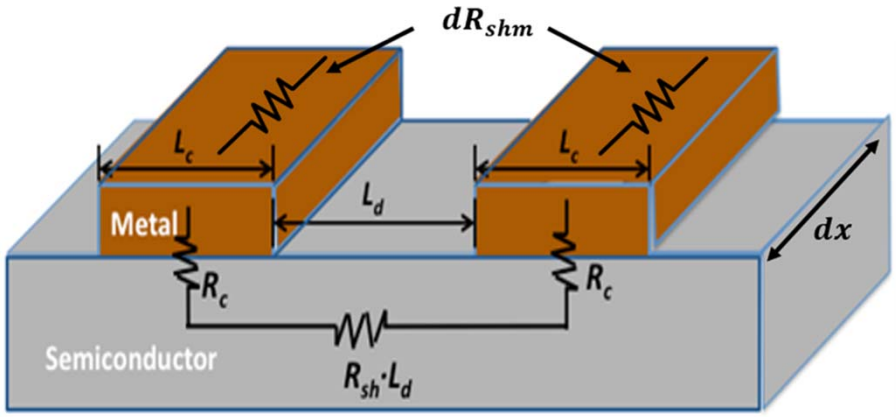


New “nano-TLM” test structure to characterize short contacts









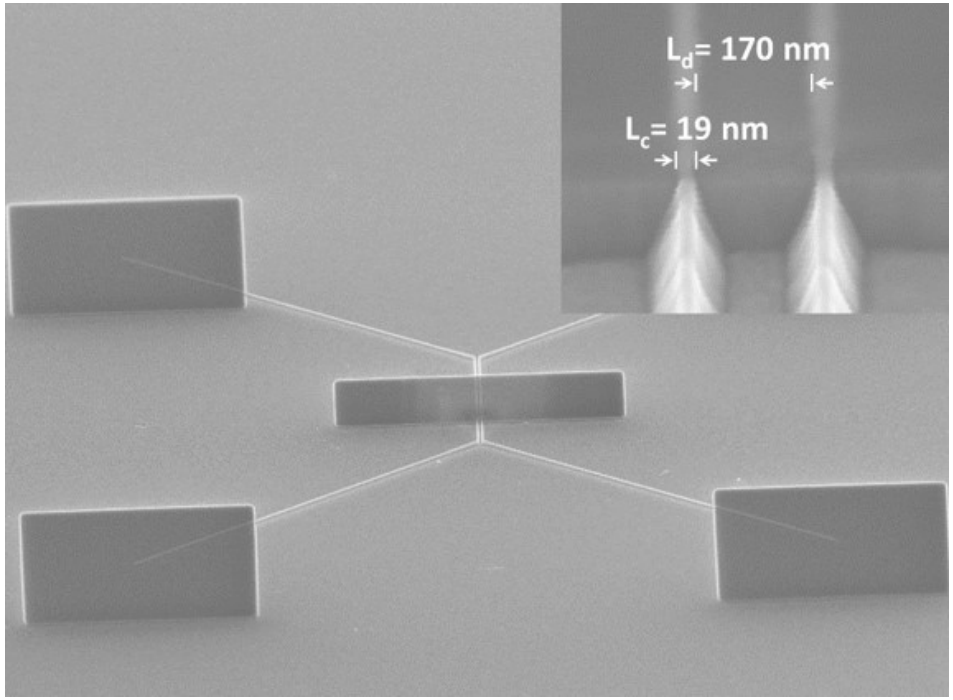
$$R_{||} = \frac{R_{TLM}}{L_{Tx}} \operatorname{csch}\left(\frac{W}{L_{Tx}}\right)$$

$$R_{\times} = \frac{R_{TLM}}{2L_{Tx}}\left[\operatorname{csch}\left(\frac{W}{L_{Tx}}\right) + \coth\left(\frac{W}{L_{Tx}}\right)\right] - \frac{R_{shm}W}{2L_c}$$

Lu, EDL (submitted)

Decouples impact of metal resistance on short contacts

Contact-first process for Mo-InGaAs ohmic contacts



Lu, EDL (submitted)

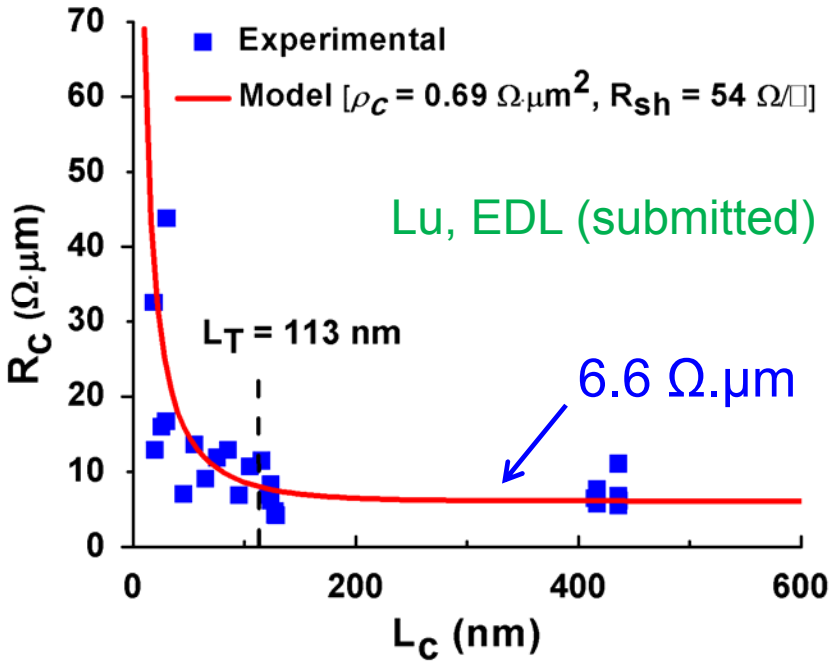
Fabrication process:

- Surface cleaning
- Mo deposition
- E-beam lithography
- Mo RIE
- Mesa isolation
- Pad metallization
- Contact anneal

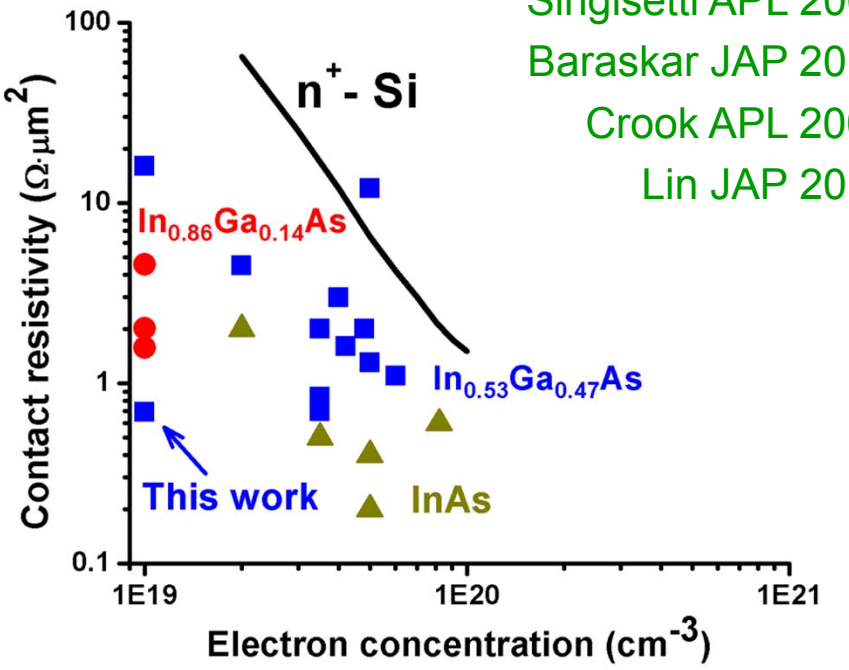
- Achieved contacts with length down to 19 nm
- Contact-first process preserves high-quality interface

Nanometer-scale Mo-InGaAs contacts

Mo on n^+-$In_{0.53}Ga_{0.47}As$:

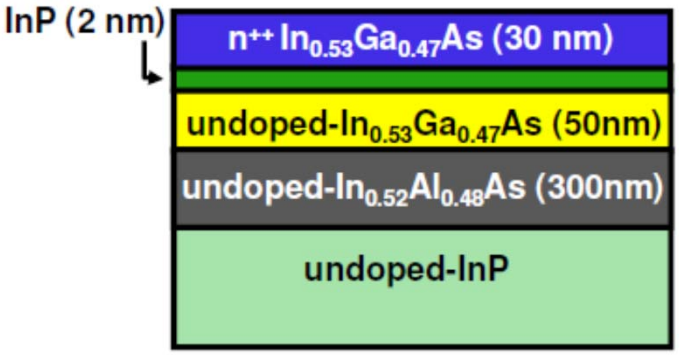


Dormaier JVSTB 2012
Singisetti APL 2008
Baraskar JAP 2013
Crook APL 2007
Lin JAP 2013

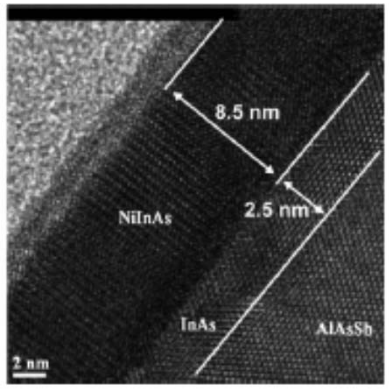


- R_c blows up for very small contacts with $L_c < L_t$ = 113 nm
- R_c ~ 40 Ω.μm for L_c ~ 20 nm
- Average ρ_c = 0.69 Ω.μm^2
- Contacts thermally stable up to 400^{o}C

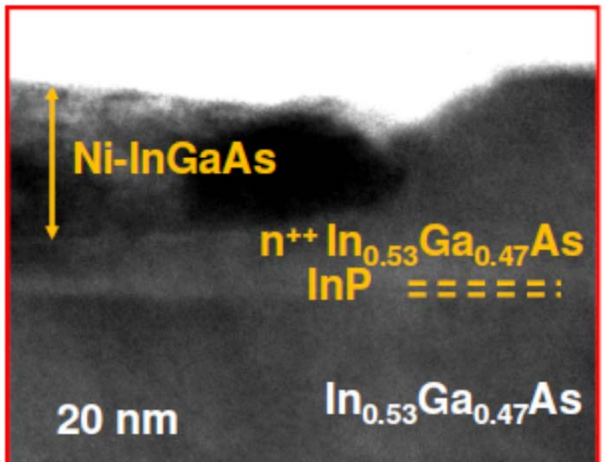
Ni-InGaAs ohmic contact

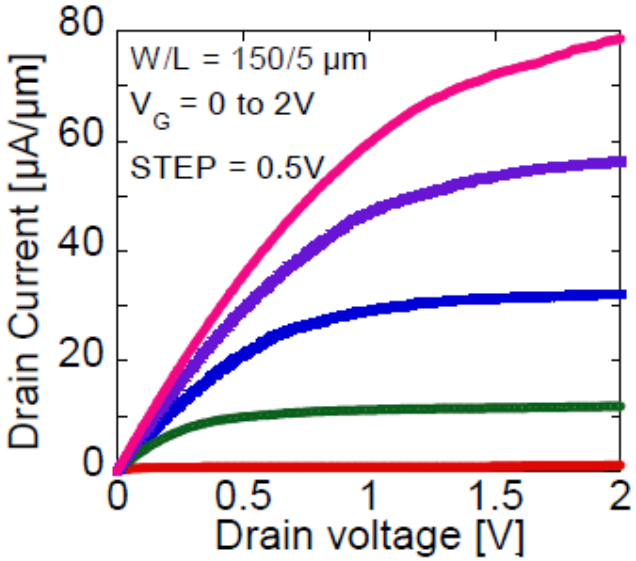


Subramanian, JES 2012



Oxland, EDL 2012





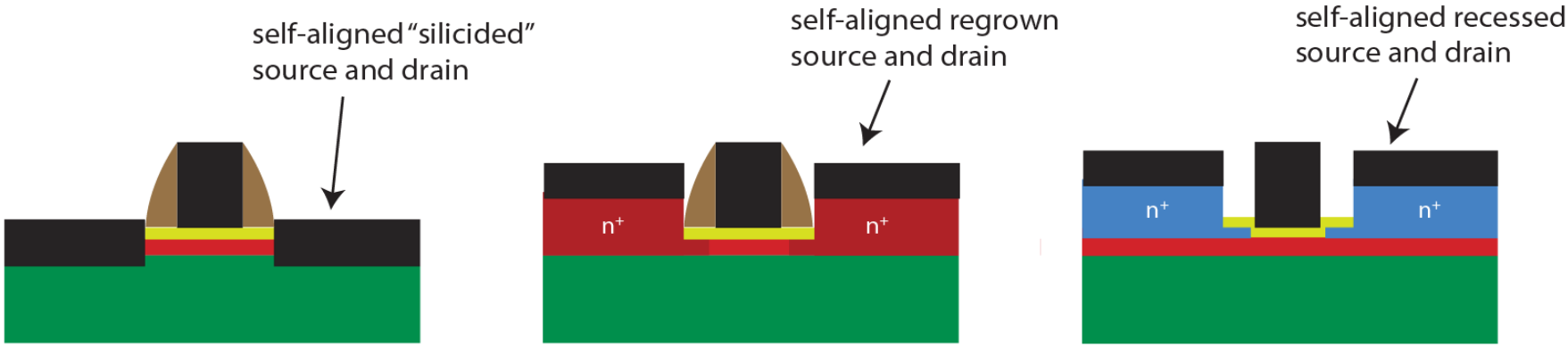
Kim, IEDM 2010

- Ni diffused into InGaAs at 250°C
- Ni-InGaAs formed
- Unreacted Ni removed using HCl-based selective etchant
- R_c ~ 50 Ω.µm demonstrated [Kim VLSI Tech 2013]

Technology issue #3: self-aligned MOSFET architectures

Challenge: ohmic contacts very closely spaced from gate

- Design of access region
- Must maintain high-quality MOS interface and low R_c



Gate-first process: "silicided" S/D

Hill, IEDM 2010
Kim, VLSI Tech 2013

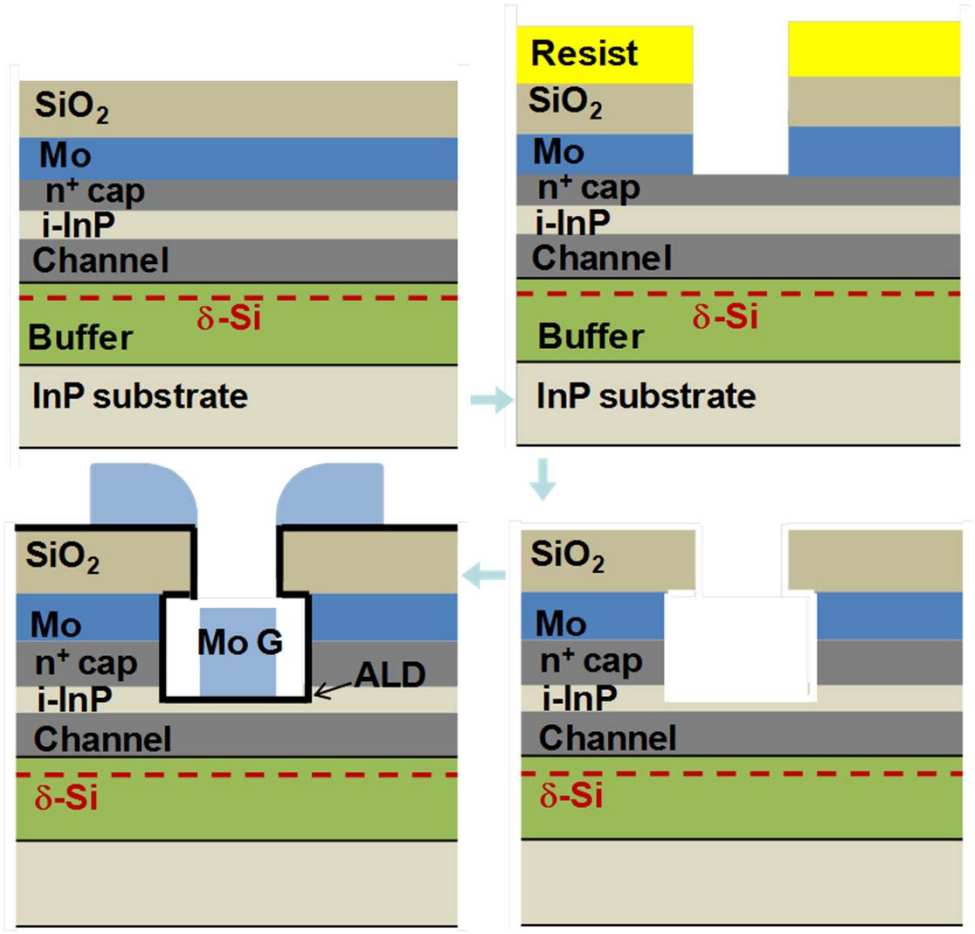
Gate-first process: regrown S/D

Egard, IEDM 2011
Zhou, IEDM 2012
Lee, VLSI Tech 2013

Gate-last process: recessed S/D

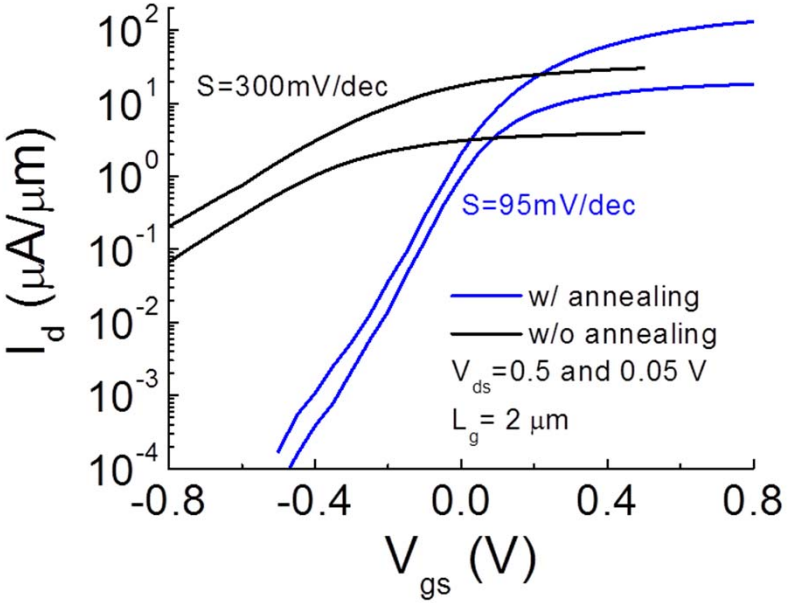
Radosavljevic, IEDM 2009
Lin, IEDM 2012

Gate-last self-aligned InGaAs MOSFETs



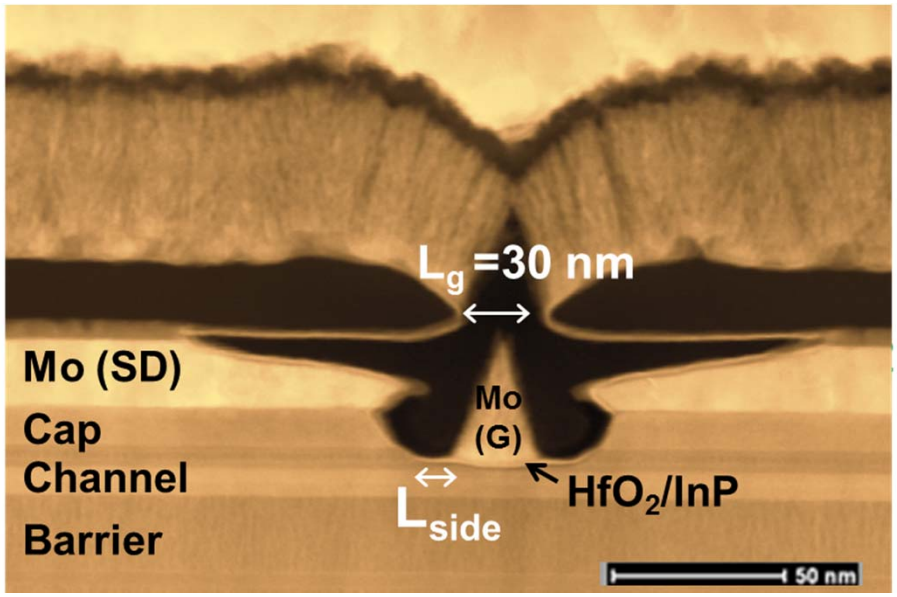
Lin, IEDM 2012

- Ohmic contact first (Mo)
- Extensive RIE (F-based)
- Interface exposed immediately before gate stack formation
- Process designed to be compatible with Si fab
- RIE damage annealed at 340°C:



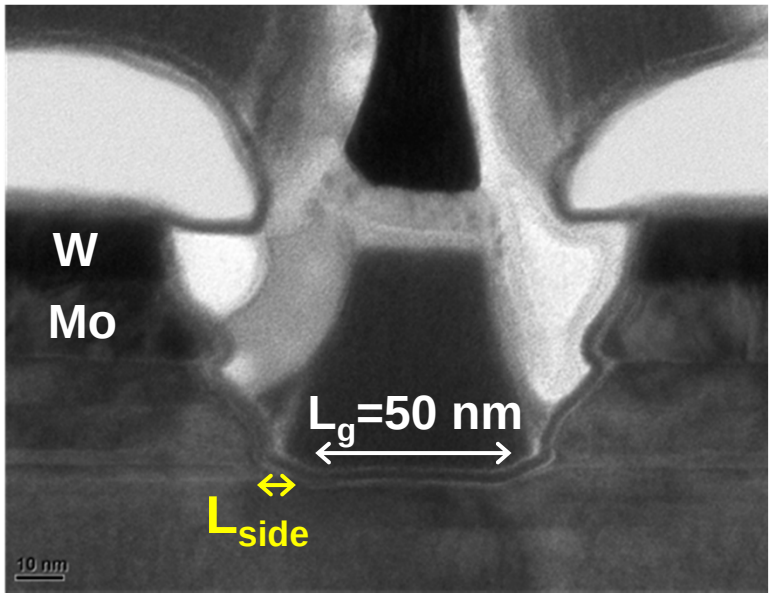
Gate-last self-aligned InGaAs MOSFETs

Lin, IEDM 2012



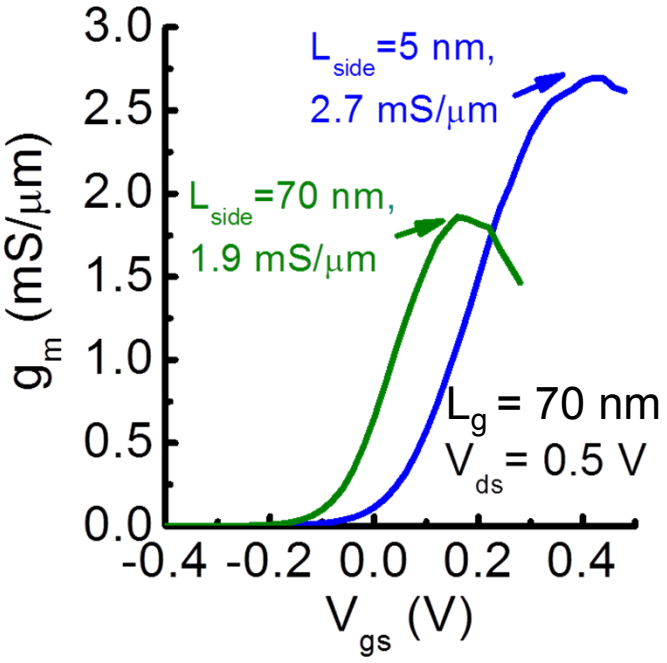
- Buried-channel (EOT~0.8 nm)
- Wet semiconductor etch
- L_{side} ~ 30 nm

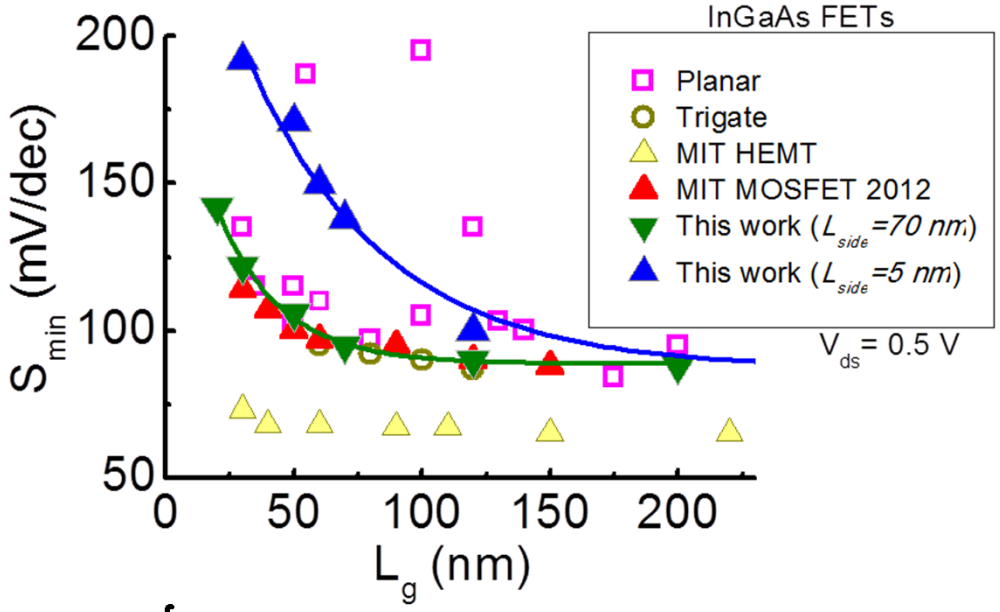
Lin, IEDM 2013



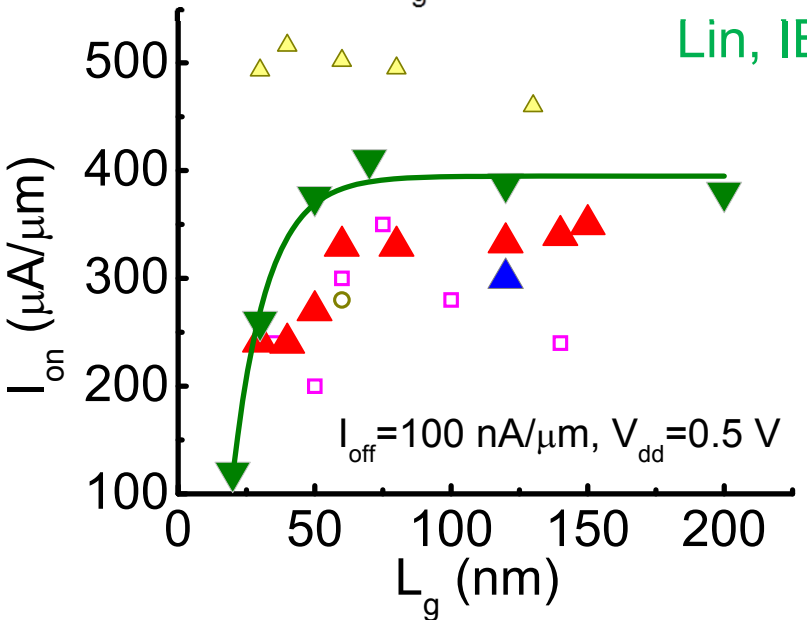
- Surface-channel (EOT~0.5 nm)
- Dry semiconductor etch + digital etch of cap
- L_{side} ~ 5 nm

Impact of L_{side}





L_{side} ↓
→ g_m ↑
→ S ↑
→ I_{on} at fixed I_{off} ↓
→ GIDL ↑



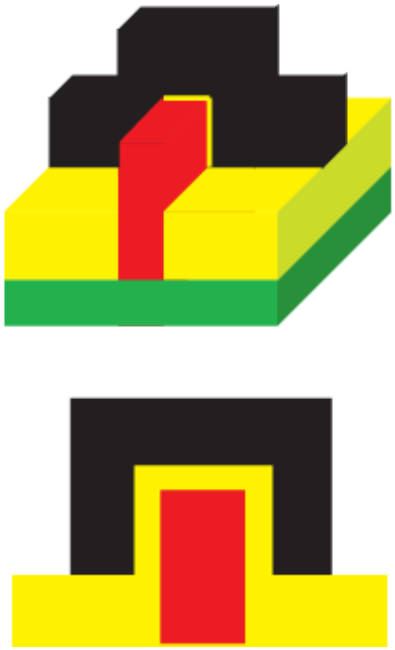
Lin, IEDM 2013

Technology issue #4: Tri-gate MOSFET

Challenge: acceptable I_{ON} and SCE on a small-footprint

- Planar design does not provide enough "electrostatic integrity"
- Need tighter channel control through 3D device design

Planar MOSFET

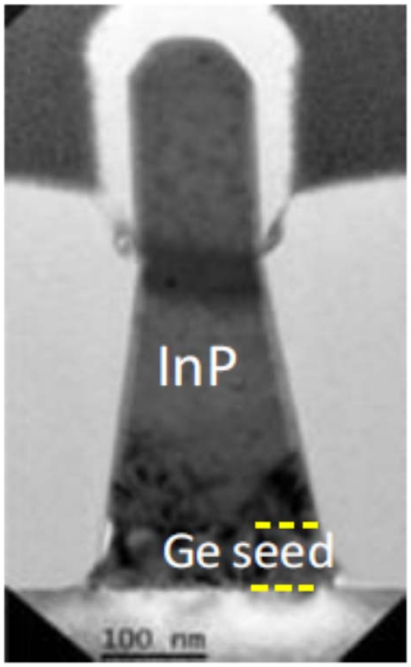


Tri-gate MOSFET

Wu, IEDM 2009
Radosavljevic, IEDM 2010
Chin, EDL 2011
Radosavljevic, IEDM 2011

Fin formation

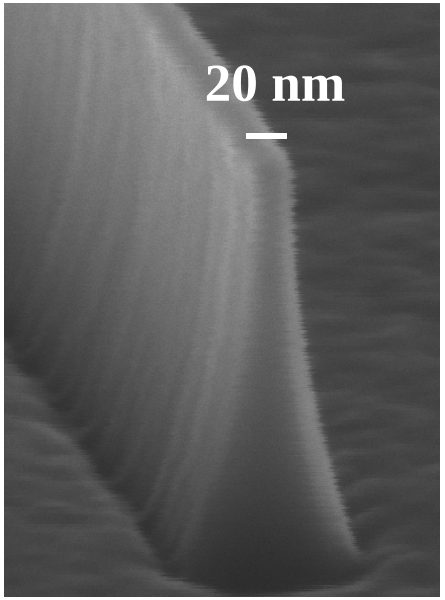
Direct fin growth by Aspect Ratio Trapping



- Some defects reach surface
- Inter-diffusion of dopant species

Fiorenza, ECST 2010
Waldron, ECST 2012

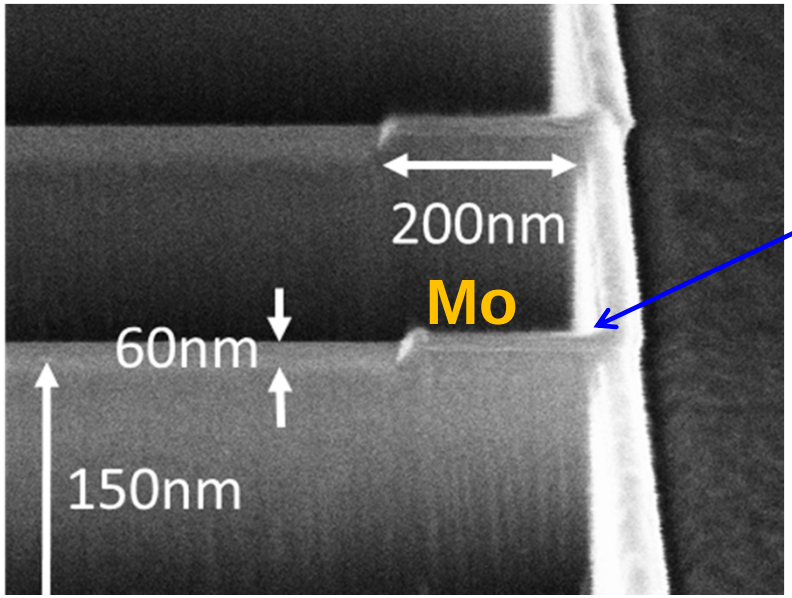
Fin etch by RIE + digital etch



- $BCl_3/SiCl_4/Ar$ RIE chemistry
- Digital etch: self-limiting (2 nm/cycle)
- No notching in heterostructures

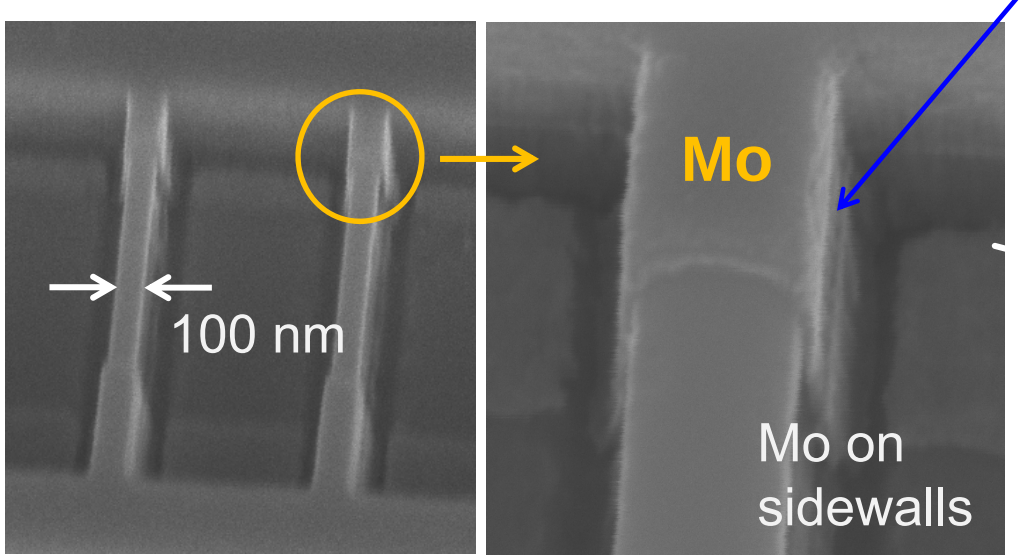
Zhao, IEDM 2013

Mo contacts to fin



- Mo-first process
- Mo used as mask for fin etch

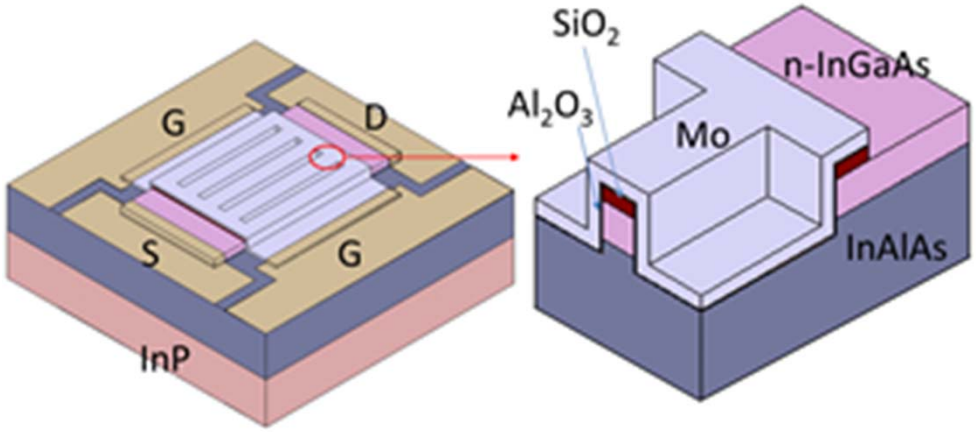
Mo sidewall contacts

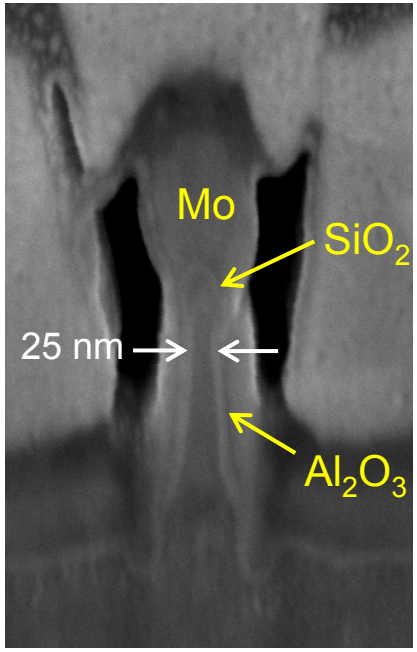


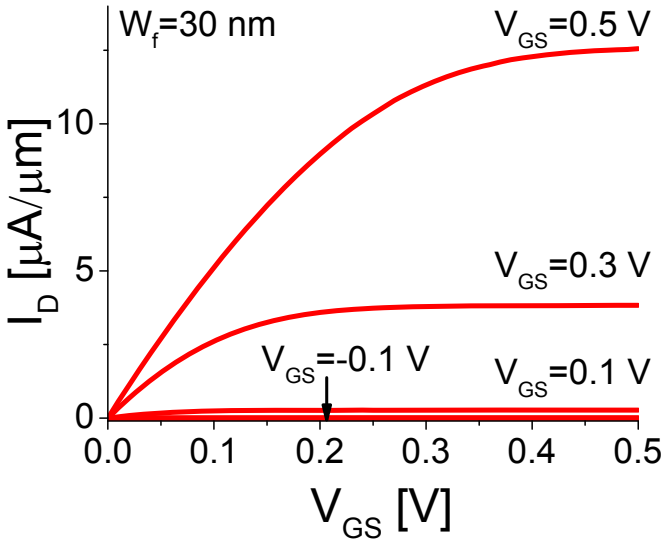
- With top Mo contact:
  - R_c ~ 7 Ω.μm
- With sidewall contact:
  - R_c ~ 12 Ω.μm

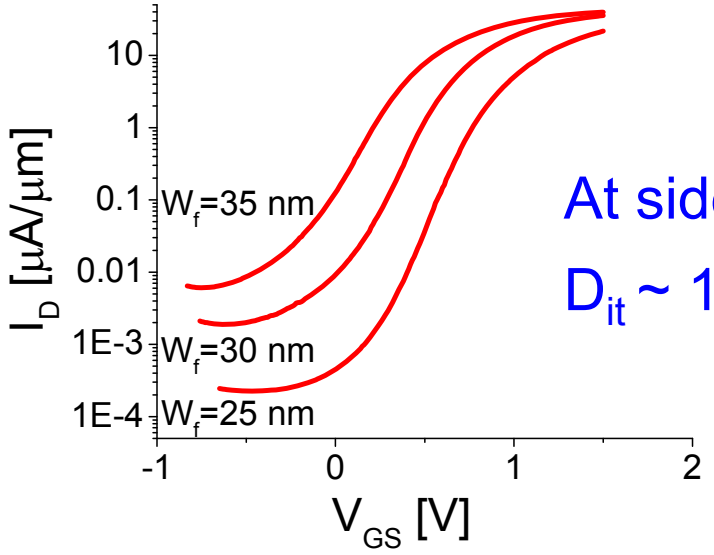
Fin sidewall MOS

Double-gate sidewall MOSFET to study sidewall MOS quality







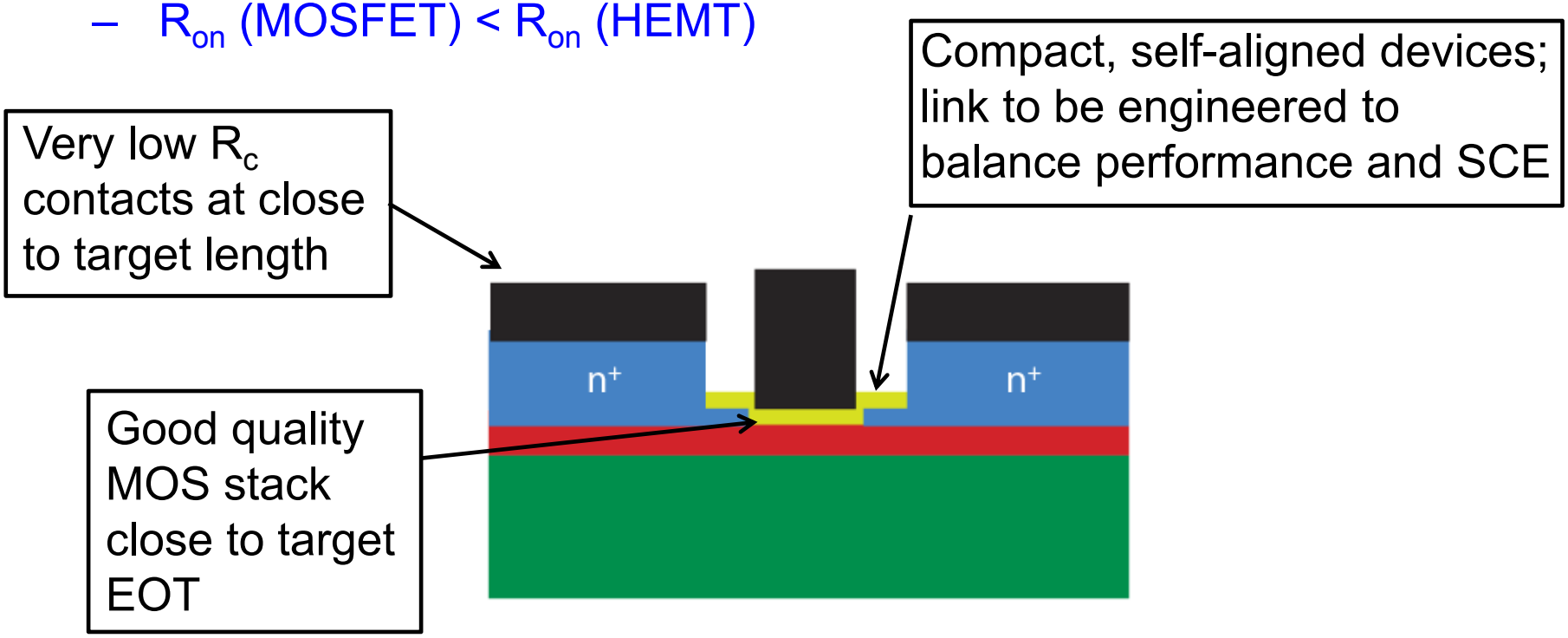


At sidewall:

$D_{it} \sim 1.4 \times 10^{13}\ eV^{-1}.cm^{-2}$

Conclusions

- Remarkable recent progress in InGaAs MOSFETs
  - g_m (MOSFET) = g_m (HEMT)
  - R_{on} (MOSFET) < R_{on} (HEMT)



- Many issues to investigate:
  - Tri-gate technology, integration with p-MOSFETs on Si, reliability