InGaAs MOSFETs for CMOS: Recent Advances in Process Technology

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Abstract— InGaAs has recently emerged as the most attractive non-Si n-channel material for future nano-scale CMOS. InGaAs n-channel MOSFETs promise to advance Moore's Law by allowing continued scaling through a reduction in footprint and operating voltage without compromising performance. This paper reviews recent advances in some of the key enabling process technology of InGaAs MOSFETs. It also outlines some of the challenges that need to be overcome before this new device family can become a reality.

I. Introduction

As Si CMOS faces mounting difficulties to maintain its historical density scaling path, InGaAs-channel MOSFETs have recently become as a credible alternative for mainstream logic technology capable of scaling to the 10 nm node and below [1]. The emergence of InGaAs hinges on two factors. First are the outstanding electron transport characteristics of InGaAs, particularly as the InAs composition increases [2]. In addition, high-K dielectrics deposited by Atomic-Layer Deposition (ALD), an ex-situ manufacturable technique, have shown to yield excellent interfacial quality with InGaAs and barrier materials lattice-matched to InGaAs such as InP [3].

The remarkable recent progress in inversion-type InGaAs MOSFETs (with InAs composition between 0 and 1) can be best appreciated by contrasting it with the relatively well established InGaAs High-Electron Mobility Transistors (HEMTs). InGaAs MOSFETs have now matched the transconductance of HEMTs [4] (Fig. 1a). This stems from the excellent scalability of the effective oxide thickness in the InGaAs MOS gate stack and to the superior source resistance of MOSFETs. In fact, the absence of a semiconductor barrier under the contacts as recently yielded InGaAs MOSFETs with better ON-resistance than HEMTs (Fig. 1b). Today's HEMTs still enjoy an edge over MOSFETs in current-gain cut-off frequency (Fig. 1c). It is only a matter of time before low parasitic capacitance MOSFET designs are developed and improved high-frequency characteristics are demonstrated.

In spite of the relative maturity of InGaAs HEMTs, a logic InGaAs MOSFET technology for integration in a sub-10 nm CMOS node faces numerous challenges. The device architecture is necessarily very different with an overriding demand for ultra-small footprint, self-aligned designs, tiny contacts and 3D device structures. At the process level, a great deal of work still needs to be carried out to shed the relics of traditional III-V device processing, such as Au-based metallization, wet etching and lift-off, and make room to VLSI-grade manufacturable processes involving Si compatible metals and dry etching. This paper discusses some

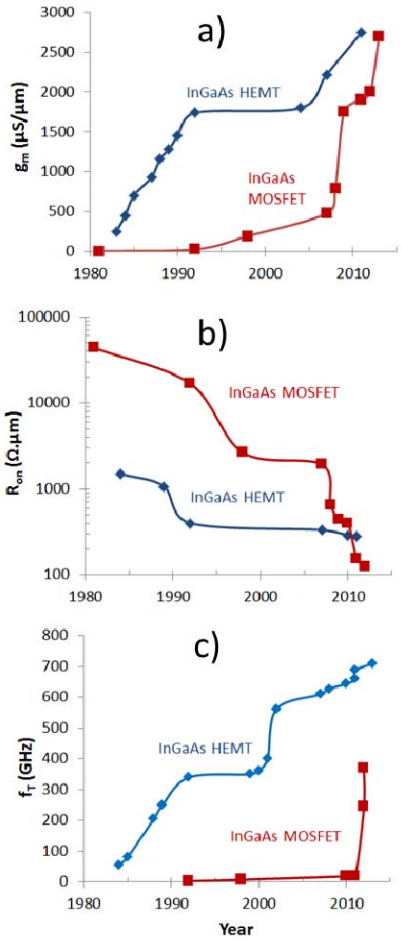

Fig. 1. Performance comparison of inversion-type InGaAs MOSFETs and HEMTs (with InAs composition between 0 and 1) vs. year: a) transconductance, b) ON resistance, c) current-gain cut-off frequency, f_T.

of the most pressing issues. Not discussed here is device integration on a Si substrate, a topic that has not received enough attention to date in the open literature.

II. InGaAs MOSFET: Process Challenges and Opportunities

One of the most critical elements in a logic transistor is the contact resistance (R_c) of nanometer-scale contacts. Mo is a refractory material with great potential for nanocontacts to n^+-InGaAs. Mo can be dry etched and serve as a mask for semiconductor dry etching. Mo also yields outstanding contact resistance. Our group has been working for some time in the development of Mo ohmic contacts in which Mo deposition is the very first step of the device fabrication process [5]. This

insures a pristine unblemished interface that yields excellent contact resistance.

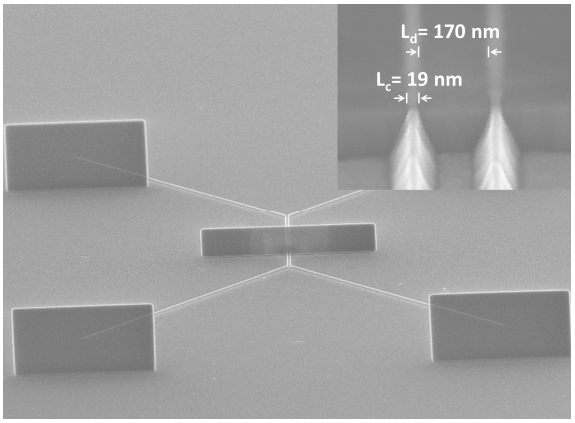

Fig. 2. Nano-TLM test structure to measure the contact resistance of nanoscale contacts to InGaAs. Inset: 19 nm long Mo contacts to InGaAs.

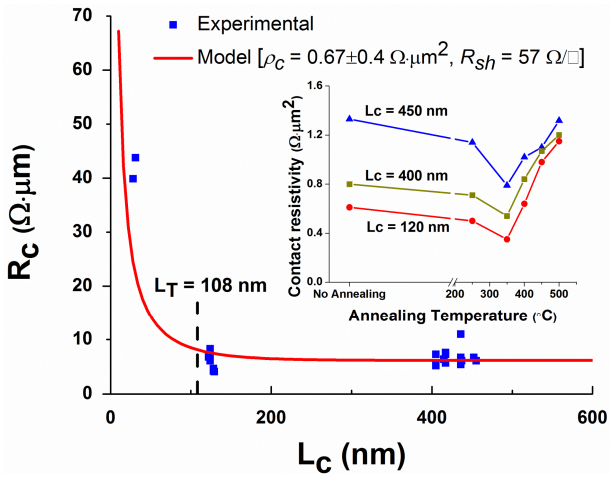

Fig. 3. Contact resistance vs. contact length for nanoscale Mo/n+-InGaAs contacts. The data is consistent with a contact resistivity of 0.67 Ω.μm^2. Inset: illustration of thermal stability of Mo/n$^+$-InGaAs contacts

To characterize nano-scale contacts, we have designed a new "nano-TLM" test structure. Fig. 2 shows an SEM picture of a nano-TLM with 19 nm long Mo contacts. Fig. 3 shows R_c measurements vs. contact length. An average contact resistivity of 0.67 Ω·μm^2 is demonstrated. This yields extremely small R_c in relatively long contacts (~6.6 Ω.μm), but R_c shoots up when the contact length becomes shorter than the transfer length (~110 nm). Further work is required to address this problem. Mo contacts are thermally stable up to about 400°C (inset of Fig. 3). Other silicide-like contacts based on Ni, Co or Pd are being investigated elsewhere [6,7]. At the moment, these alternative approaches yield inferior values for the contact resistance.

The key enabling technology for InGaAs MOSFETs is a high-quality oxide/semiconductor interface by ALD. Many groups have demonstrated excellent Al_2O_3/InGaAs interfaces and surface-channel transistors. This is insufficient for future scaled CMOS. First, a higher permittivity dielectric is required. Also, in a surface-channel design, interface roughness scattering severely degrades the mobility (Fig. 4). The pressing need is for an ultra-scaled buried-channel design with a total EOT well below 1 nm. We are investigating a composite HfO_2/InP MOS barrier without intermediate Al_2O_3 passivation [5]. This is predicated on research that shows that HfO_2 gives lower D_{it} on InP than Al_2O_3 [8]. Our device results confirm that Al_2O_3 passivation is not needed (Fig. 5). Using a HfO_2/InP composite gate barrier with sub-1 nm EOT, we have obtained L_g=50 nm MOSFETs with a subthreshold swing of 95 mV/dec at V_{dd}=0.5 V. This nearly matches the characteristics of InGaAs Trigate FETs of identical gate length even though the Trigate MOSFET has intrinsically better short-channel effects [9]. In our approach, the MOS interface is formed late in the process and is completely finished immediately after the InP barrier is exposed [5]. This yields nearly ideal S=69 mV/dec on long-channel transistors [5]. Higher K dielectrics are being investigated by other groups and show promise [10,11].

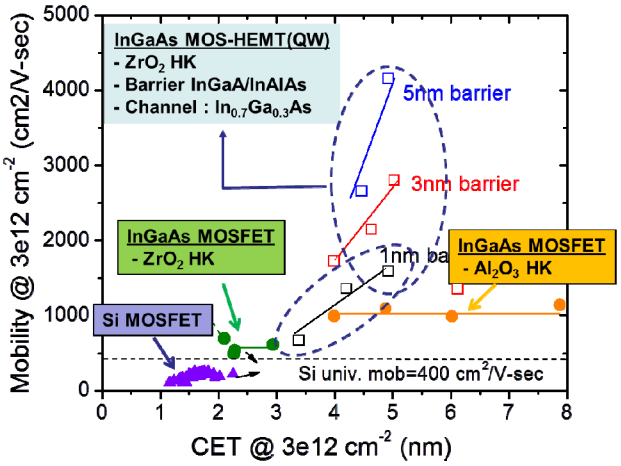

Fig. 4. Electron mobility in InGaAs channel MOS structures as a function of Capacitance-Equivalent Thickness (CET) at a sheet electron concentration of 3x10^{12} cm^{-2} for surface-channel and buried-channel MOSFETs using ZrO_2 as gate dielectric.

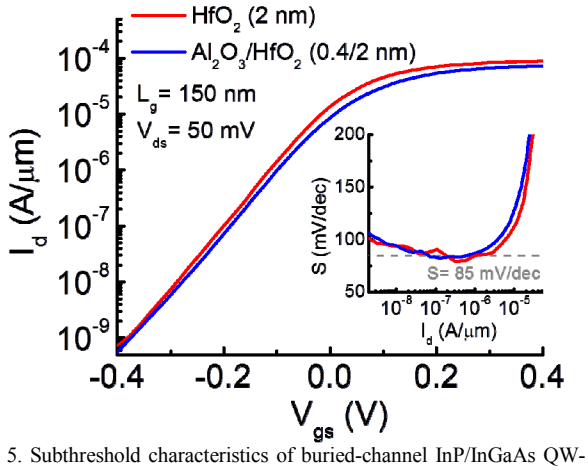

Fig. 5. Subthreshold characteristics of buried-channel InP/InGaAs QW-MOSFETs with different gate dielectrics. The InP cap is about 1 nm thick. A pure HfO_2 gate dielectric without Al_2O_3 passivation gives excellent results [5]. The total EOT of this gate barrier is about 0.8 nm.

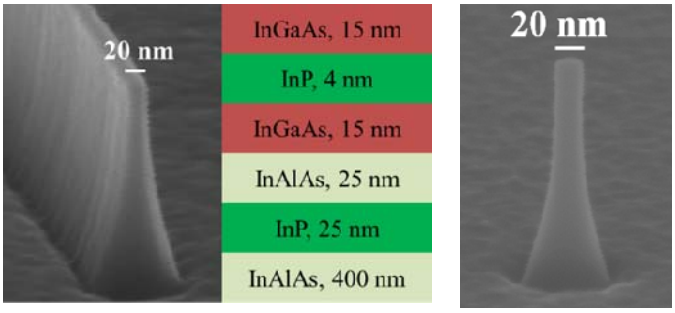

Fig. 6. Dry-etched III-V structures using a $BCl_3/SiCl_4/Ar$ chemistry [12]. Left: 20 nm wide fin on an InGaAs/InAlAs/InP heterostructure (middle). Right: 20 nm diameter InGaAs nanowire with aspect ratio greater than 10.

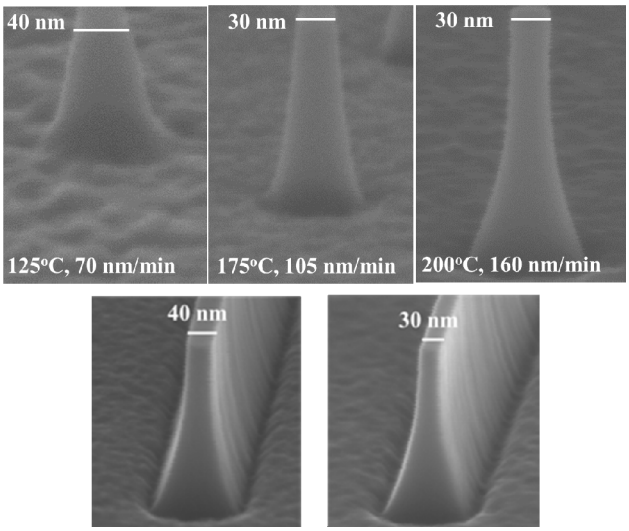

Fig. 7. Top: Impact of dry etch temperature on etching rate, profile, trenching and surface roughness of InGaAs nanowires. Bottom: Impact of digital etch on InGaAs fin. Left: immediately after dry etch; right: after 5 subsequent cycles of digital etch. The sidewalls become considerably smoother [12].

Precision III-V dry etching is another key enabling technology for InGaAs MOSFETs. HEMTs utilize wet etch techniques that are not suitable for VLSI. Dry etching of In-containing compounds is notoriously difficult. We are developing a novel ICP RIE process based on $BCl_3/SiCl_4/Ar$ chemistry [12]. When combined with digital etching, we have realized 20 nm fins and pillars on InGaAs/InAlAs/InP heterostructures without notching and minimum footing and trenching (Fig. 6) [12]. Etching temperature plays a key role: sidewall profile, surface roughness and etch rate improve as etch temperature increases to 200°C (Fig. 7 top). In our process, RIE is followed by a non-selective digital etch. This separates the etch chemistry into its two constitutive components: surface oxidation (in O_2 plasma in our case) and oxide removal (in H_2SO_4), both of which are self-limiting. Digital etch enables precise removal of material at an etch rate of ~0.9 nm/cycle. We use dry etch + digital etch to recess the cap of InGaAs MOSFETs and to smooth the sidewalls of fins and narrow their width while preserving a high aspect ratio (Fig. 7 bottom).

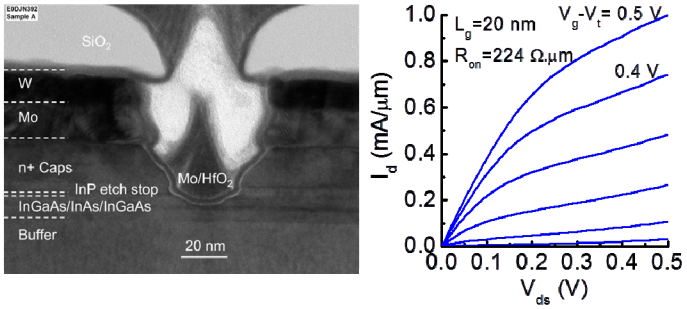

Fig. 8. TEM and output characteristics of a L_g=20 nm self-aligned QW-MOSFET with a contact to gate spacing of 5 nm [4].

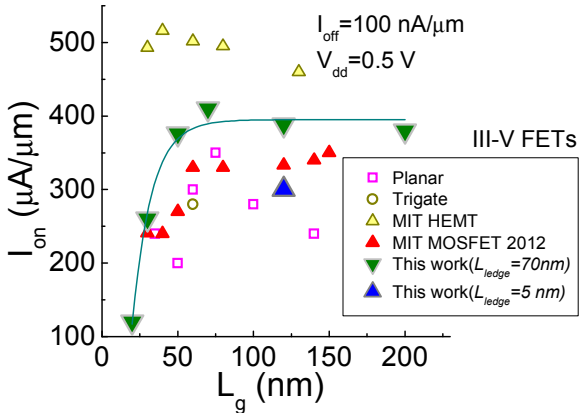

Fig. 9. Benchmarking of I_{on} *vs.* L_g for self-aligned InGaAs QW-MOSFETs and recently published III-V FETs. For all devices I_{off}=100 nA/μm and V_{dd}=0.5 V. "This work" refers to [4].

Process integration of Mo contacts, RIE and digital etch enable a self-aligned, recessed, gate-last process that showcases the remarkable potential of InGaAs [4,5]. MOSFETs with 20 nm gate length and 5 nm gate-contact separation have been demonstrated (Fig. 8) [4]. Longer L_g devices exhibit a record peak transconductance of 2.7 μS/μm which nearly matches that of the best HEMTs (Fig. 1a). Other designs yield a record I_{ON}>400 μA/μm at an I_{off}=100 nA/μm and V_{dd}=0.5 V (Fig. 9). A concern with processes involving extensive dry etching is RIE damage. This severely degrades mobility and subthreshold characteristics [13]. The damage probably consists of ion incorporation, dopant passivation and interface state generation. Fortunately, effective damage repair is possible using relatively benign thermal treatments [13].

Alternative MOSFET designs are being pursued. Epitaxial selectively-regrown contacts have yielded the recent record R_{on} values shown in Fig. 1b [14]. Epi-grown contacts are also interesting because they allow the introduction of tensile strain in the channel to boost performance [15]. Sub-10 nm MOSFETs will require 3D device architectures such as Trigate FETs [9] or Gate-All-Around Nanowire FETs [12,16]. In Trigate FETs, fin formation is a major concern. Direct epitaxial growth of the fin through Aspect Ratio Trapping [17,18] is attractive but working transistors have yet to be demonstrated. At MIT, we are investigating RIE in combination with digital etch (Fig. 7 bottom). In our approach, we use Mo as an RIE mask. This yields self-aligned ohmic

contacts with excellent contact resistance (~7.7 Ω·µm for long fin contacts) (Fig. 10 top). We are also investigating sputtered-Mo conformal contacts which should exhibit even better contact resistance (Fig. 10 bottom).

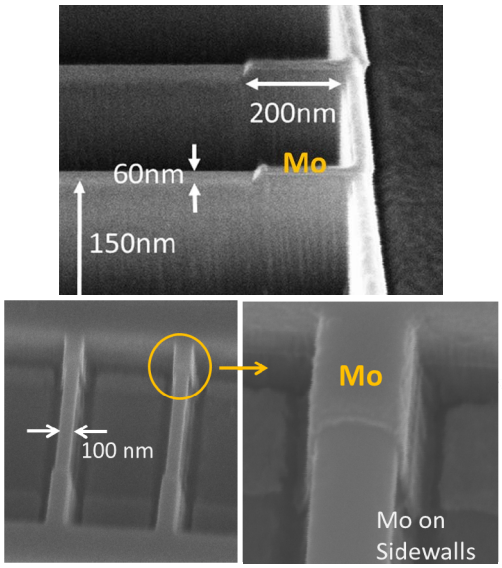

Fig. 10. Top: Fin structure with Mo ohmic contacts (the Mo contact is part of the mask structure that defines de fin during RIE). Bottom: Conformal Mo ohmic contacts to InGaAs fins.

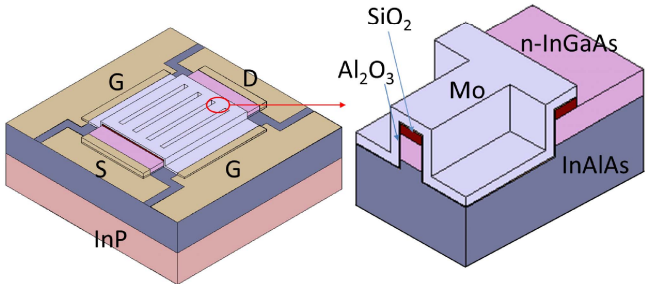

Fig. 11. Sketches depicting a double-gate sidewall MOSFET designed to characterize the sidewall MOS gate stack of Trigate FETs. The device is designed to avoid gate action at the top of the fin.

A concern in Trigate FETs with fins fabricated by RIE is the sidewall MOS interface. We are characterizing this through a double-gate sidewall MOSFET test structure in which there is no gate action at the top of the fin (Fig. 11). From the subthreshold characteristics of these devices (Fig. 12), we preliminary extract D_{it}~$1.4x10^{13}$ $eV^{-1}\cdot cm^{-2}$ at the Al_2O_3–covered sidewalls. Digital etching, appropriate surface treatments and alternative sidewall orientations should be explored to reduce this. Sidewall MOS physics and engineering in Trigate FETs is an area that demands urgent attention.

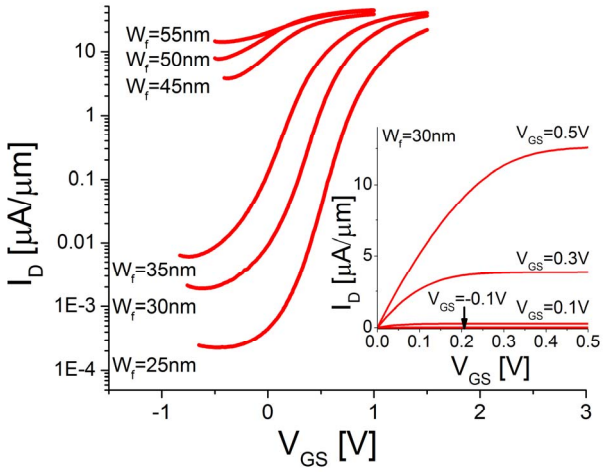

Fig. 12. Subthreshold characteristics of double-gate sidewall n-InGaAs MOSFETs with different fin widths. Inset: output characteristics of a device with fin width of 30 nm.

III. CONCLUSIONS

After 40 years of scaling and an impressive record of innovation, CMOS might be about to take its most disruptive step to date: to get rid of Si in the channel. If and when this happens, InGaAs appears as the most promising new channel material to replace Si in n-MOSFETs. Remarkable progress has recently taken place but serious challenges remain before this technology can become a reality.

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