Nanometer-Scale InGaAs Field-Effect Transistors for THz and CMOS Technologies

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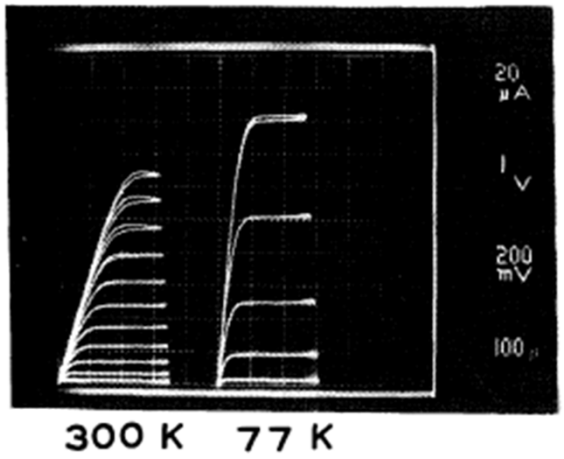
- Labs at MIT: MTL, NSL, SEBL

Outline

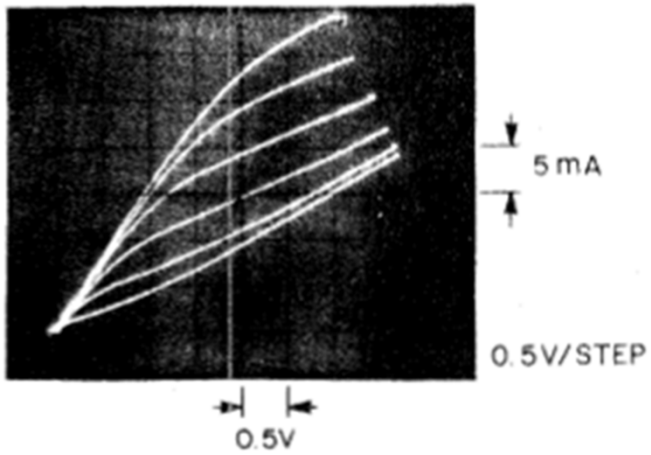
1. InGaAs HEMT today
2. InGaAs HEMTs towards THz operation
3. InGaAs MOSFETs: towards sub-10 nm CMOS

A bit of perspective…

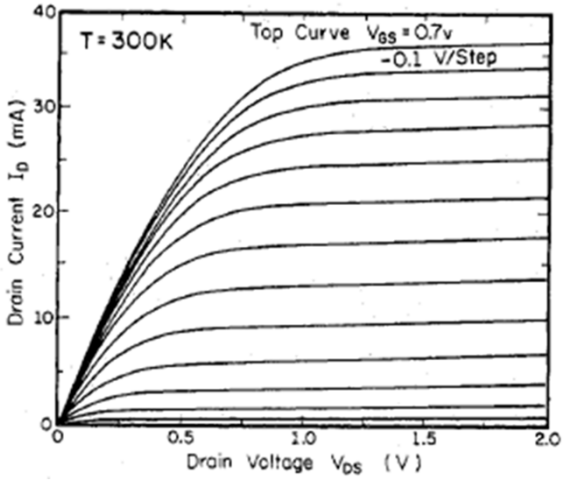
- Invention of AlGaAs/GaAs HEMT: Fujitsu Labs. 1980
- First InAlAs/InGaAs HEMT on InP: Bell Labs. 1982
- First AlGaAs/InGaAs Pseudomorphic HEMT: U. Illinois 1985
- Main attraction of InGaAs: RT μ_e = 6,000~30,000 $cm^2/V.s$



Mimura, JJAPL 1980



Chen, EDL 1982

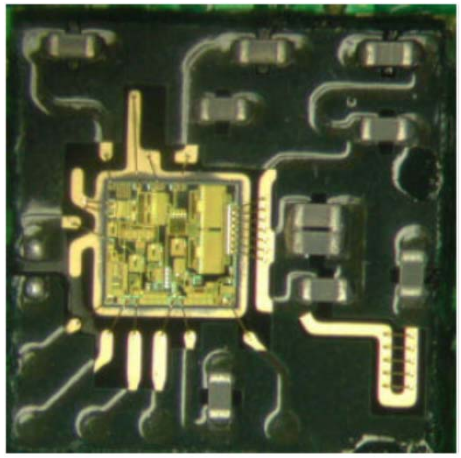


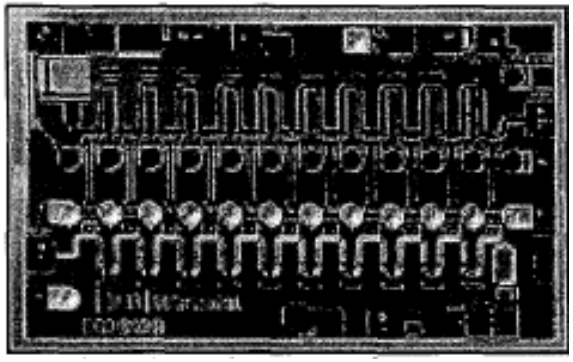
Ketterson, EDL 1985

InGaAs Electronics Today

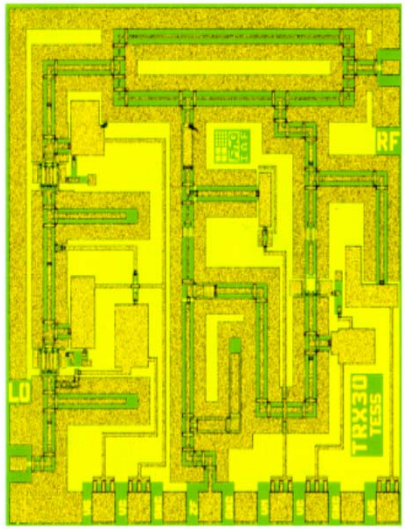
TriQuint and Skyworks Power iPhone 5

UMTS-LTE PA module
Chow, MTT-S 2008

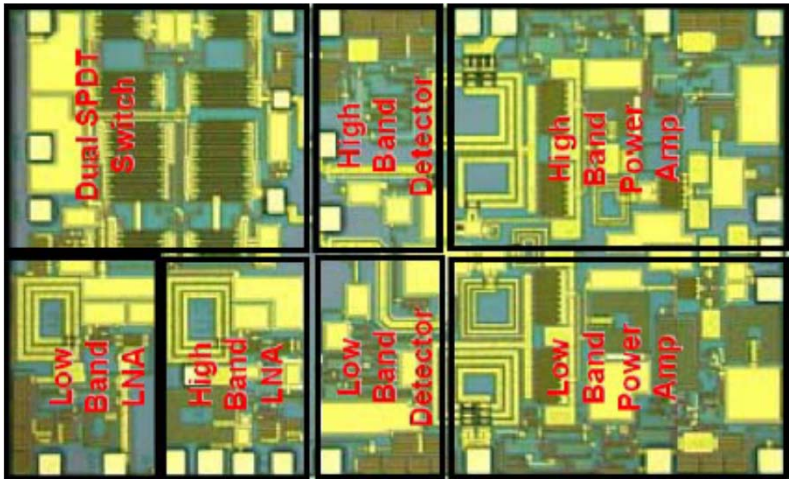




40 Gb/s modulator driver
Carroll, MTT-S 2002

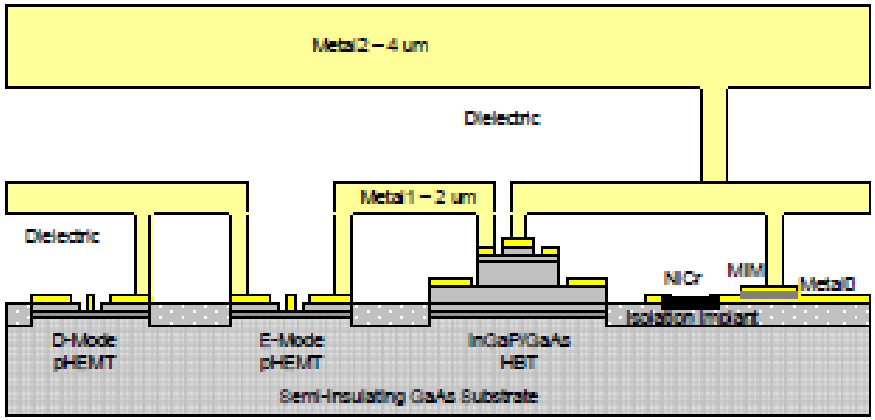


77 GHz transceiver
Tessmann, GaAs IC 1999



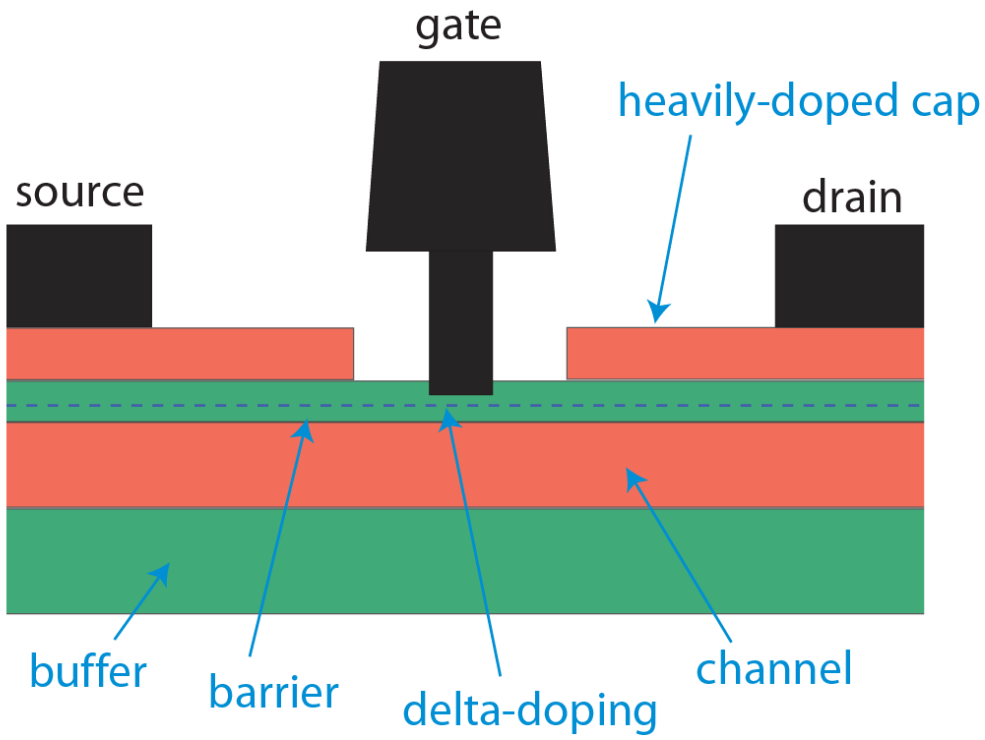
Single-chip WLAN MMIC, Morkner, RFIC 2007

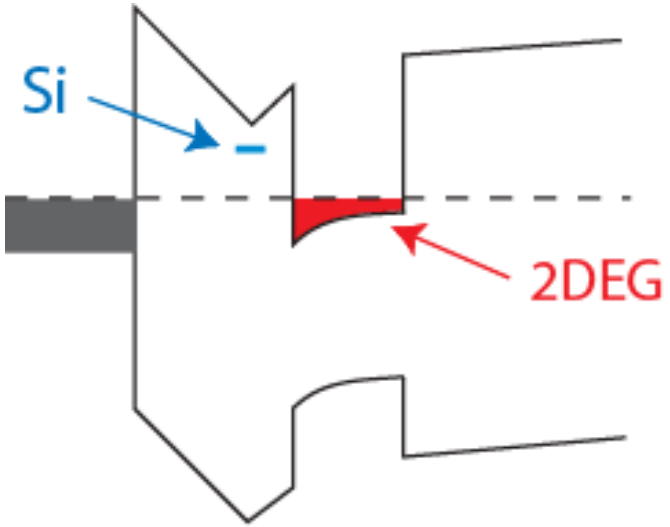
Bipolar/E-D PHEMT process



Henderson, Mantech 2007

InGaAs High Electron Mobility Transistor (HEMT)

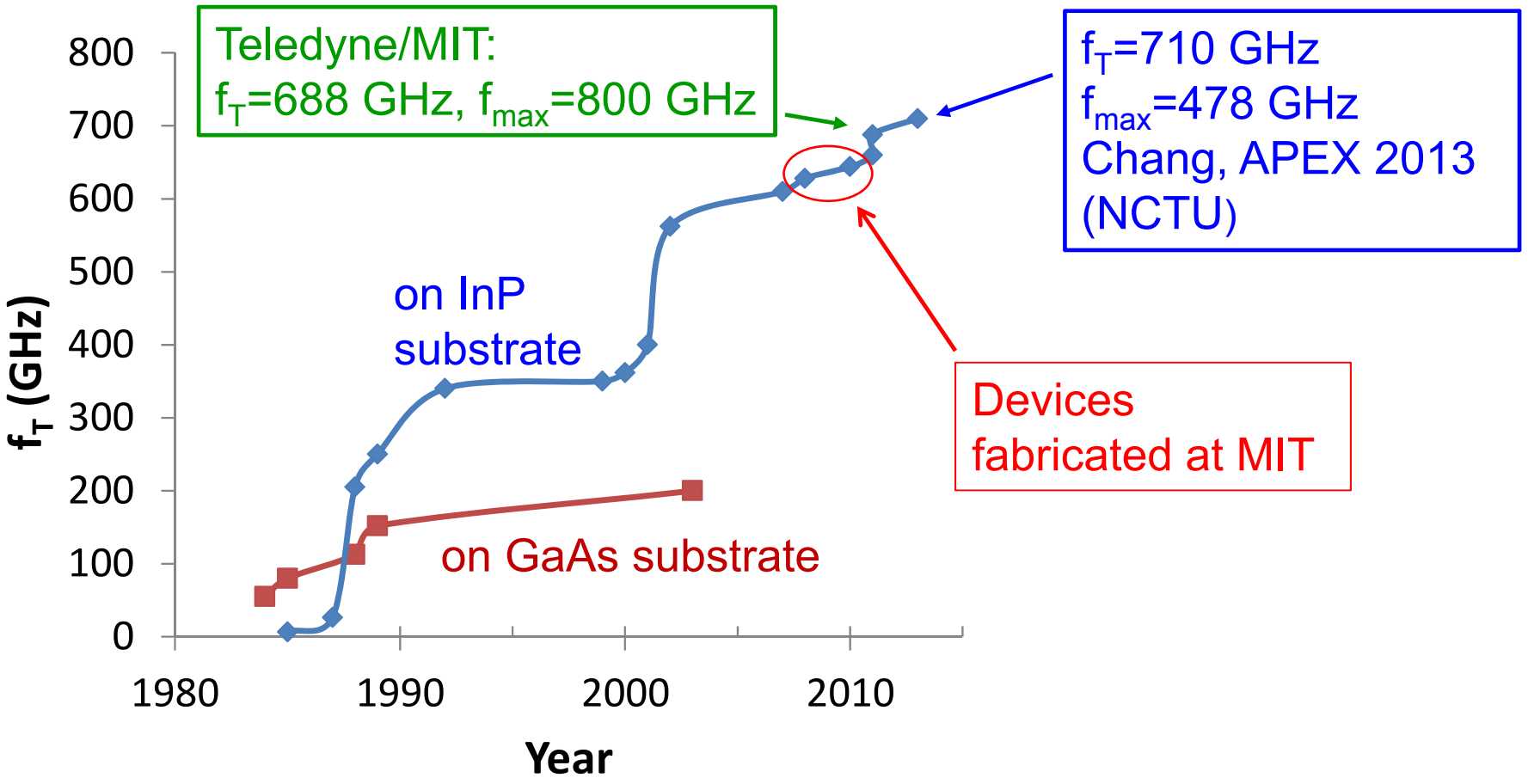




Modulation doping:

→ 2-Dimensional Electron Gas at InAlAs/InGaAs interface

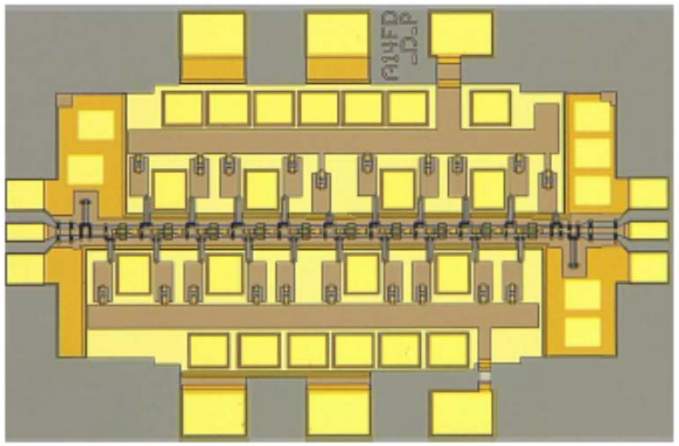
InGaAs HEMT: high-frequency record vs. time



- Highest f_T of any FET on any material system
- Best balanced f_T and f_{max} of any transistor on any material

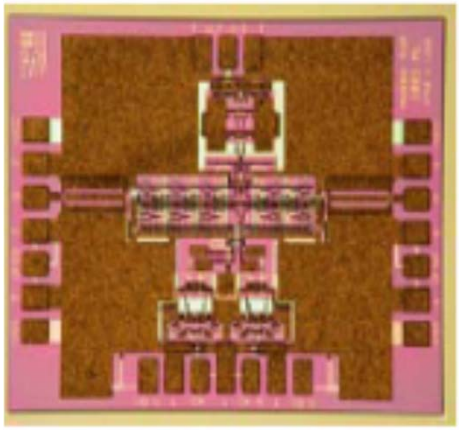
InGaAs HEMTs: circuit demonstrations

10-stage 670 GHz LNA

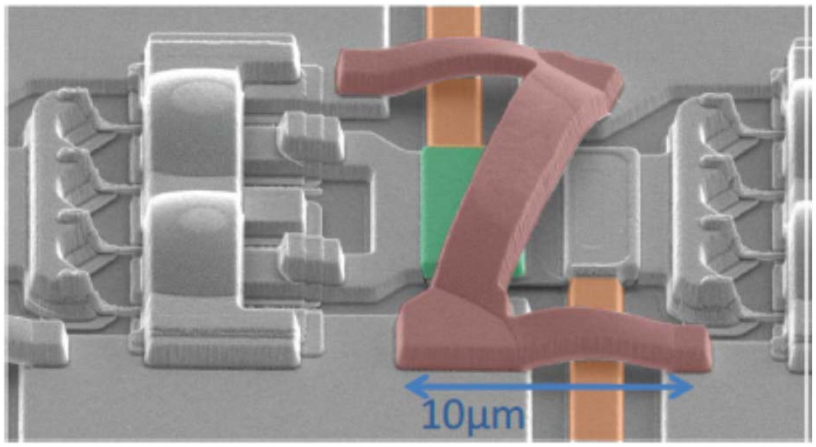


Leong, IPRM 2012

80 Gb/s multiplexer IC

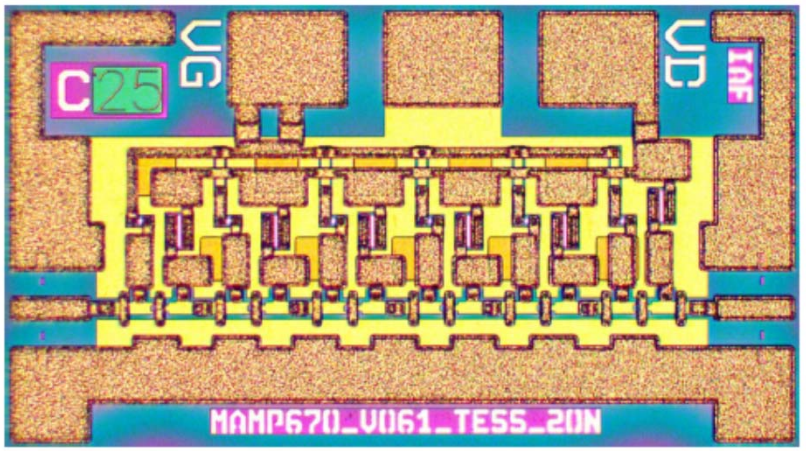


Wurfl, GAAS 2004



Sarkozy, IPRM 2013

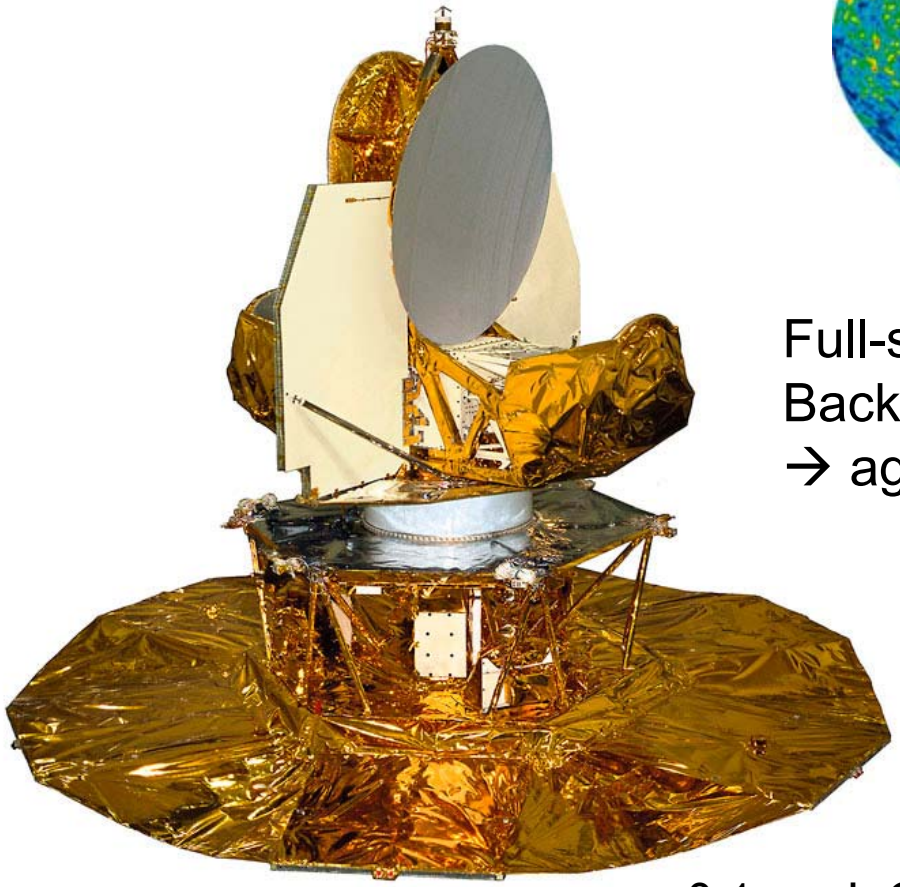
6-stage 600 GHz LNA



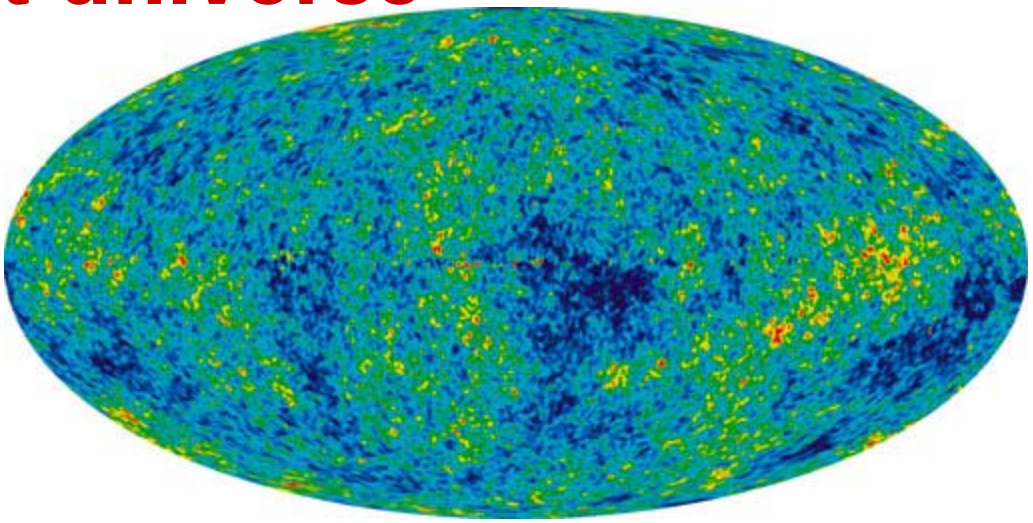
Tessmann, CSICS 2012

InGaAs HEMTs on InP used to map infant universe

WMAP=*Wilkinson Microwave Anisotropy Probe*
Launched 2001

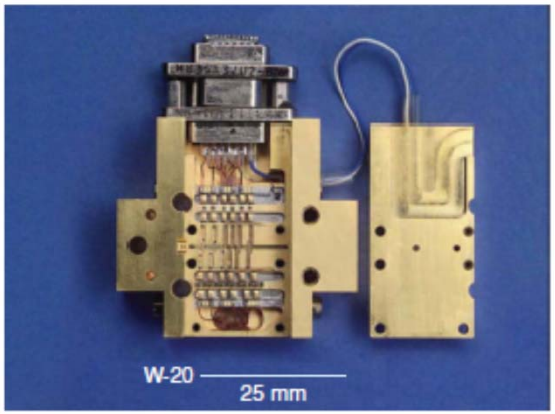


http://map.gsfc.nasa.gov/

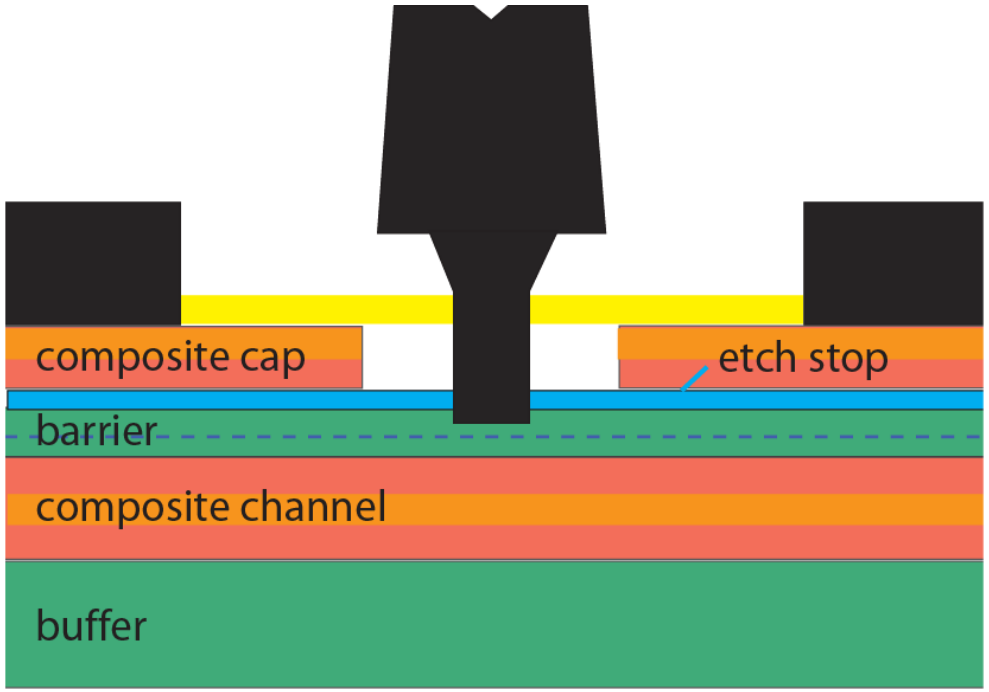


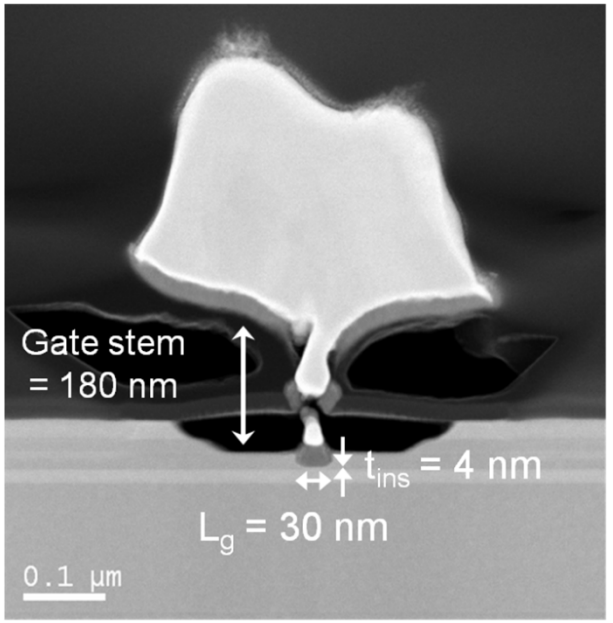
Full-sky map of Cosmic Microwave Background radiation (oldest light in Universe)
→ age of Universe: 13.73B years (±1%)

0.1 μm InGaAs HEMT LNA
Pospieszalski, MTT-S 2000



A closer look: InGaAs HEMTs at MIT





QW channel (t_{ch} = 10 nm):

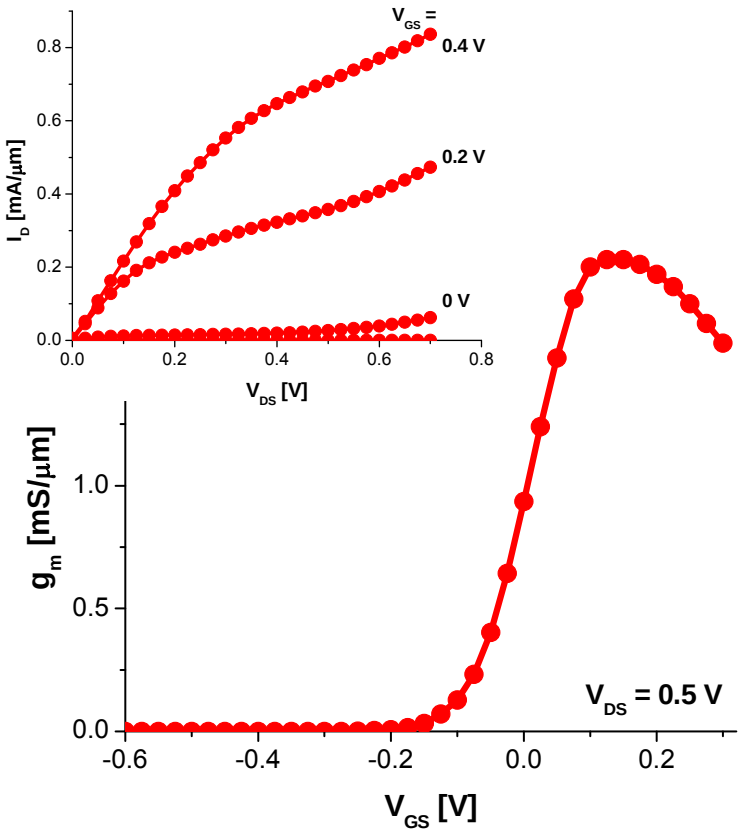
- InAs core
- InGaAs cladding

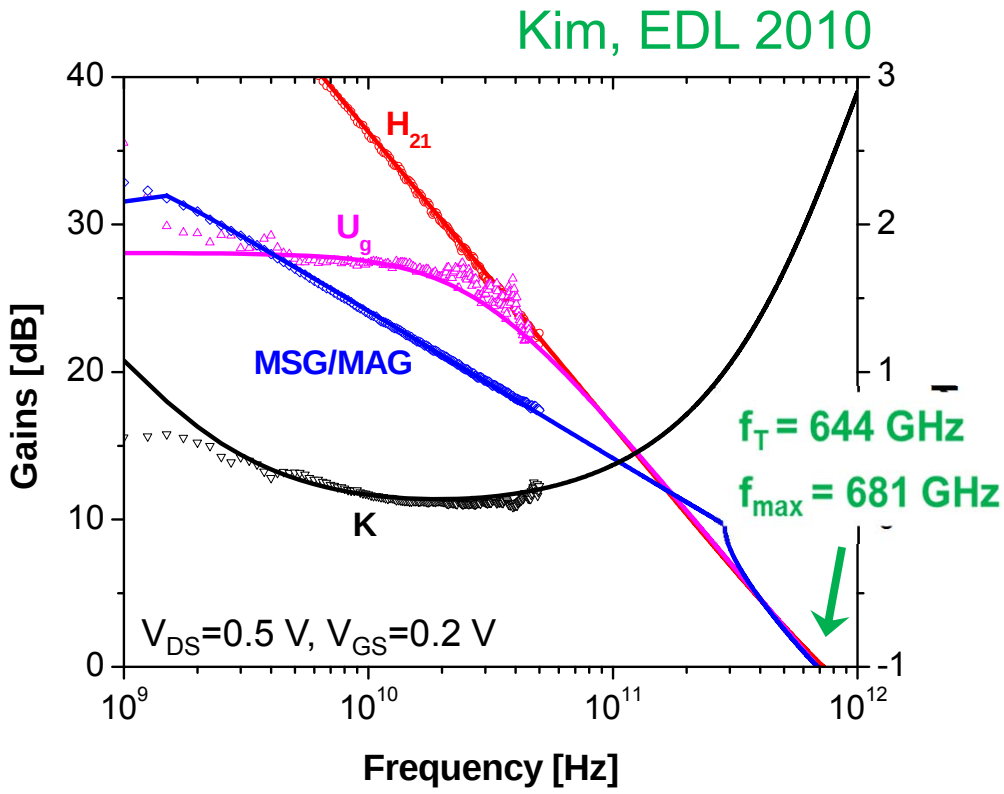
– μ_e = 13,200 cm^2/V-sec

- InAlAs barrier (t_{ins} = 4 nm)
- L_g = 30 nm

Kim, EDL 2010

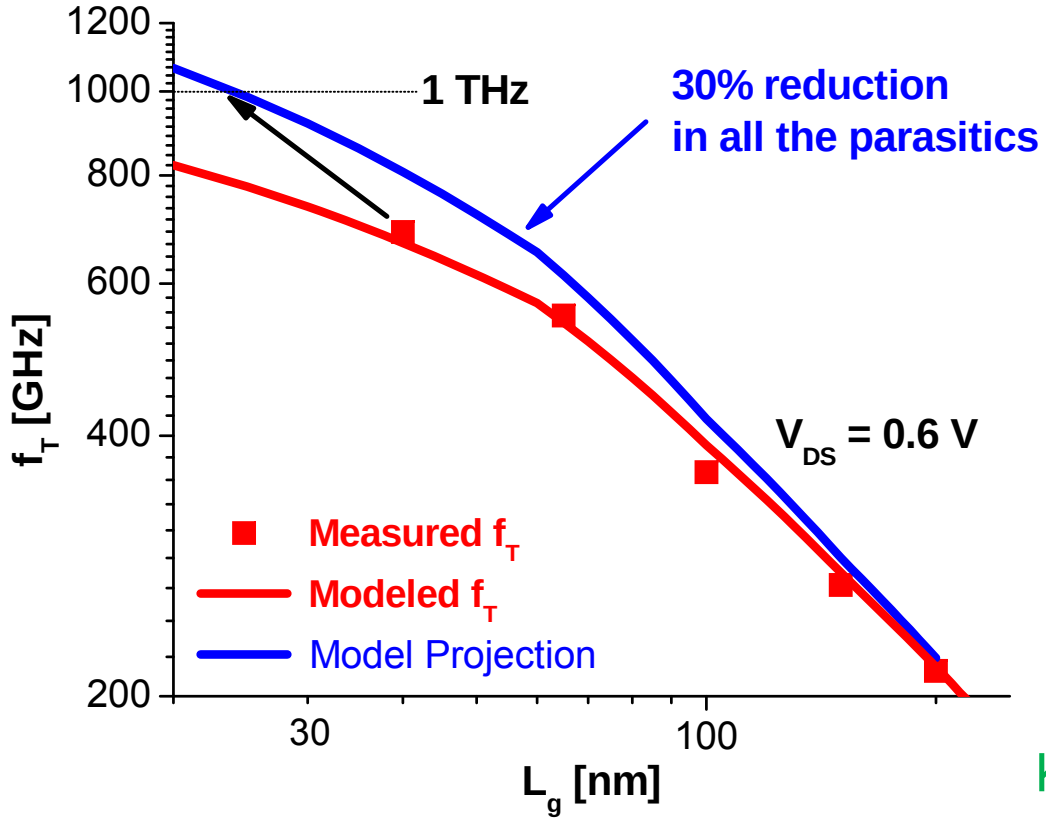
L_g = 30 nm InGaAs HEMT





- High transconductance: g_m= 1.9 mS/μm at V_{DD}=0.5 V
- First transistor of any kind with both f_T and f_{max} > 640 GHz

How to reach f_T = 1 THz?



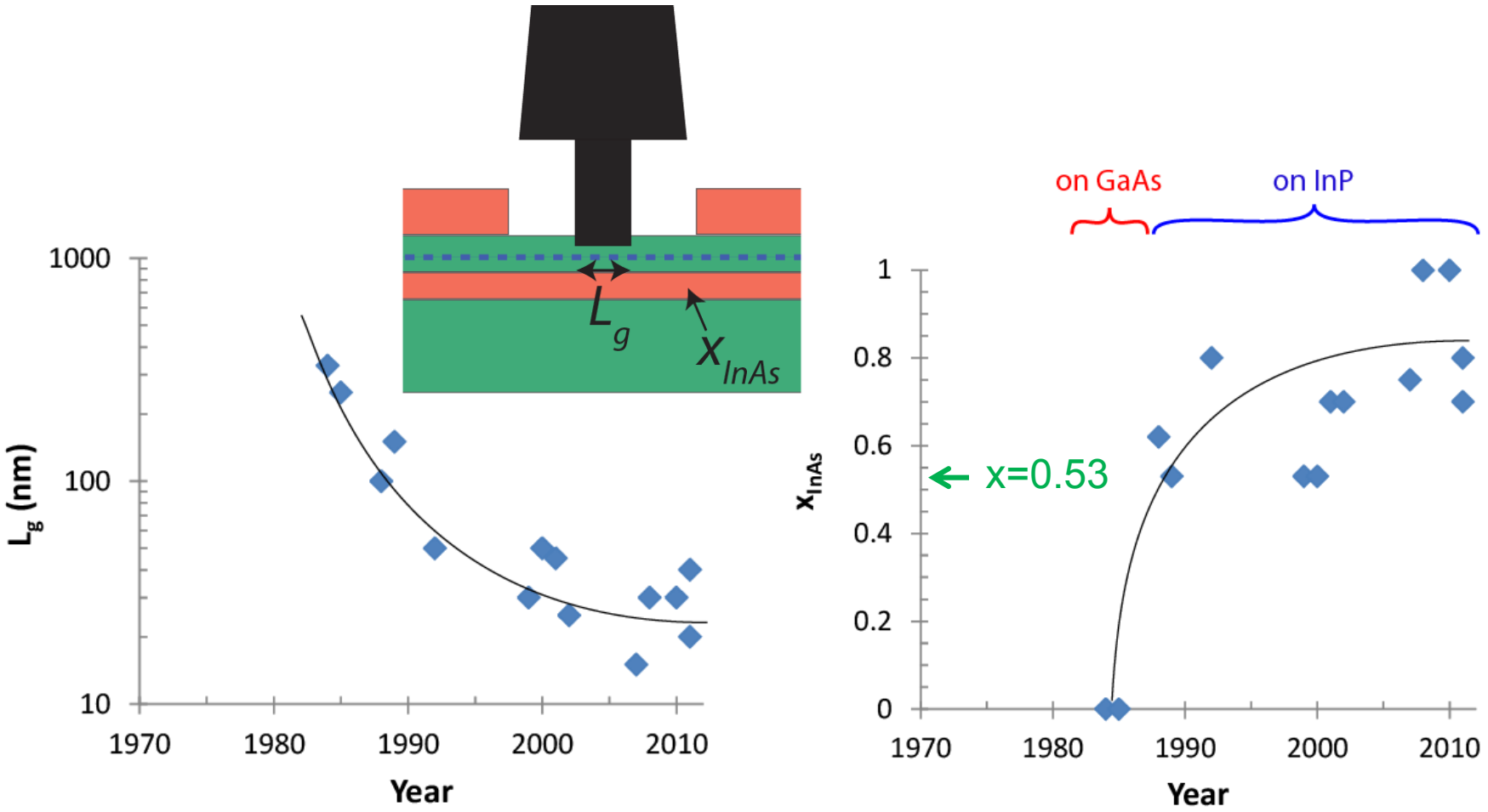
Kim, IEDM 2011

f_T = 1 THz feasible by:

→ scaling to $L_g \approx$ 25 nm

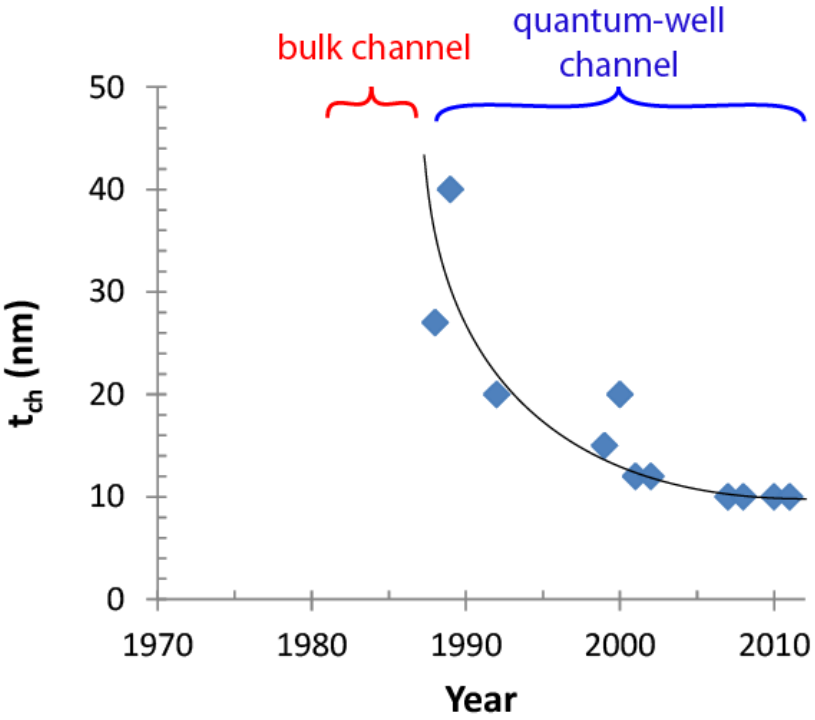
→ ~30% R and C parasitic reduction

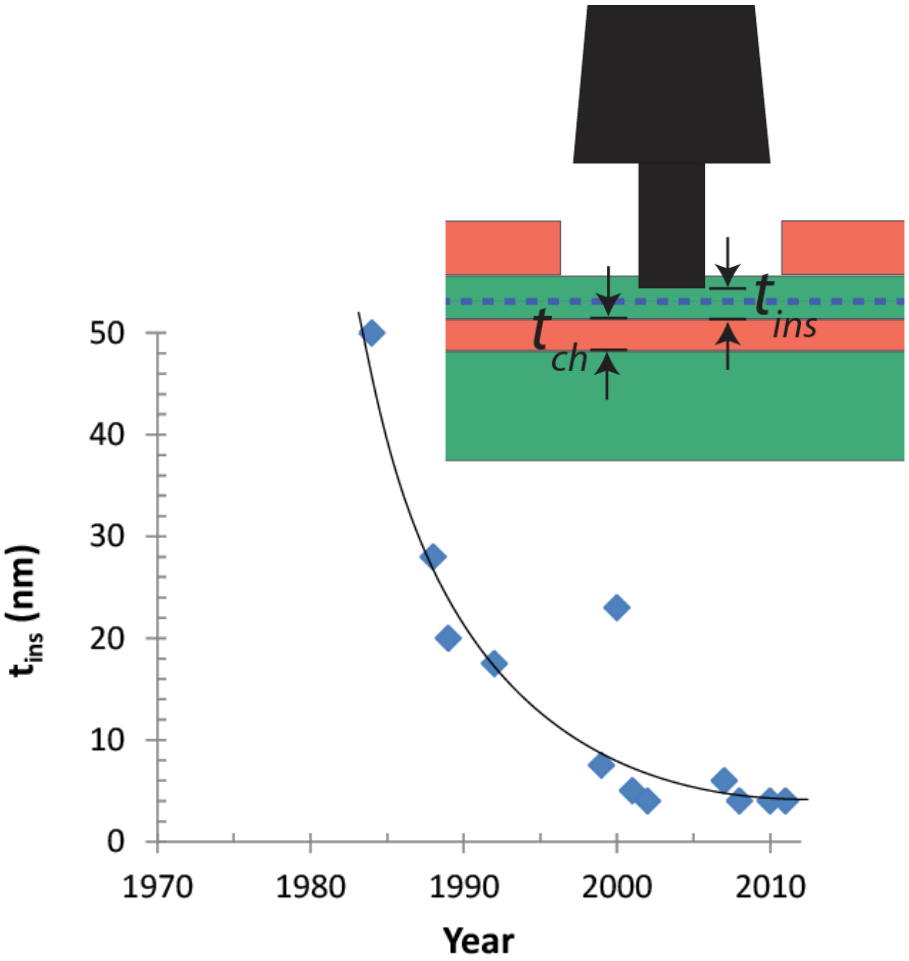
Record f_T InGaAs HEMTs: megatrends



- Over time: $L_g\downarrow$, $In_xGa_{1-x}As$ channel $x_{InAs}\uparrow$
- L_g, x_{InAs} saturated → no more progress possible?

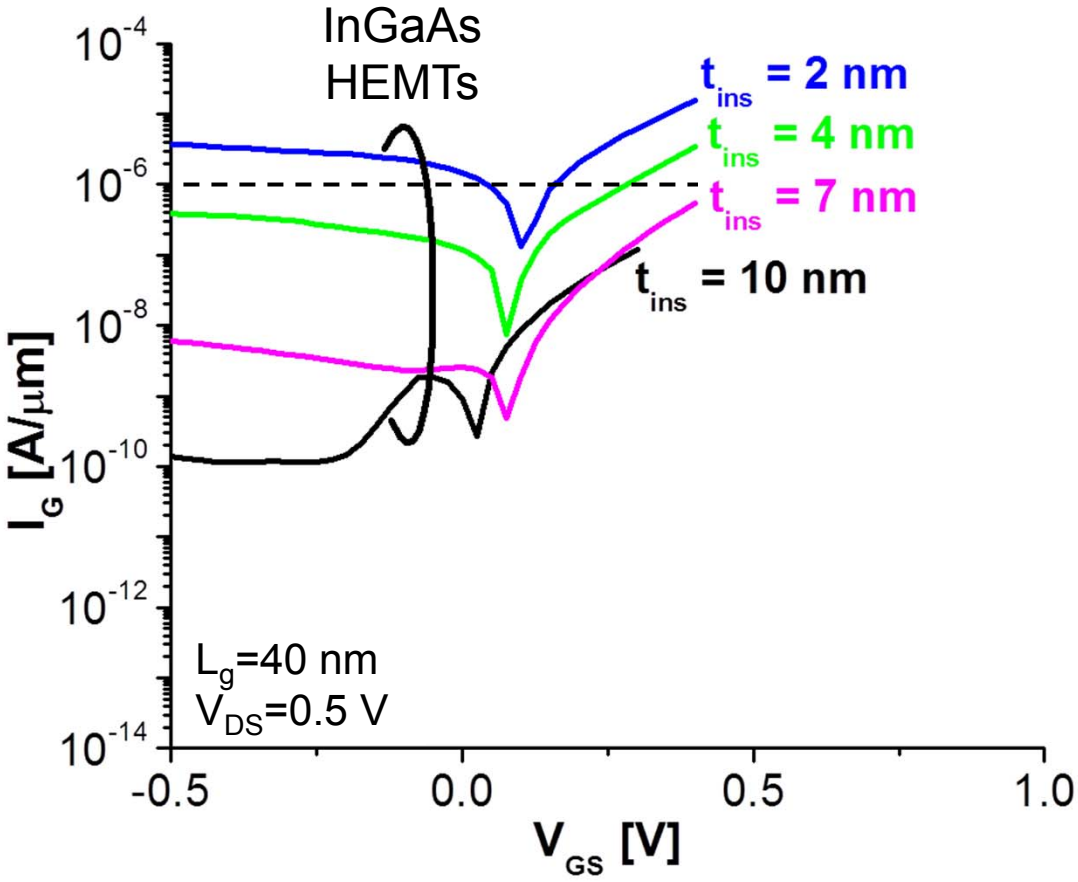
Record f_T InGaAs HEMTs: megatrends

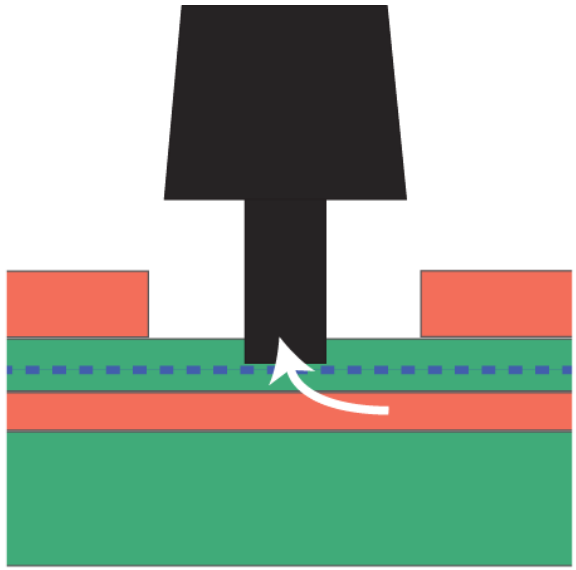




- Over time: $t_{ch}\downarrow$, $t_{ins}\downarrow$
- t_{ch}, t_{ins} saturated → no more progress possible?

Limit to HEMT barrier scaling: gate leakage current

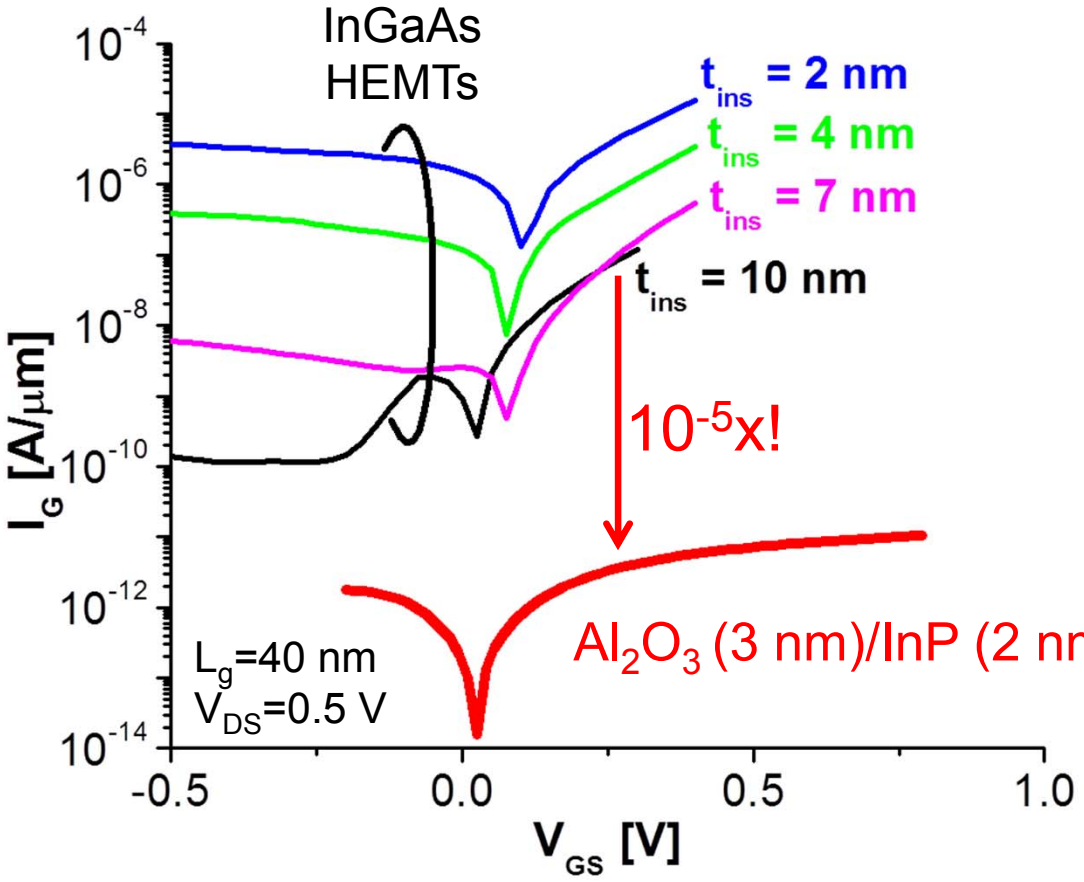


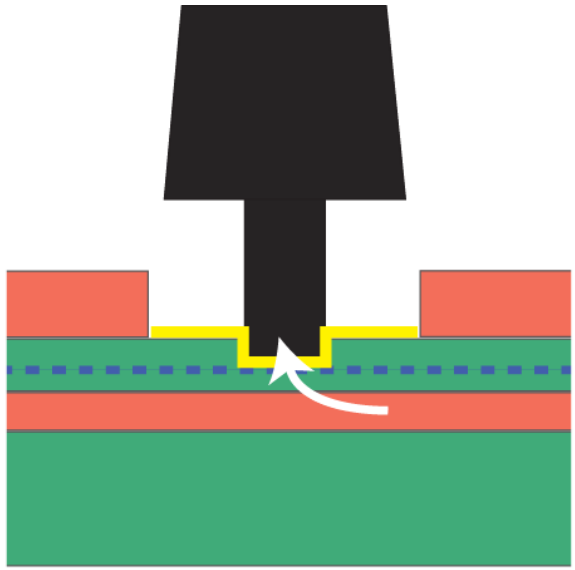


Kim, EDL 2013

At L_g=30-40 nm, modern HEMTs are at the limit of scaling!

Solution: MOS gate!





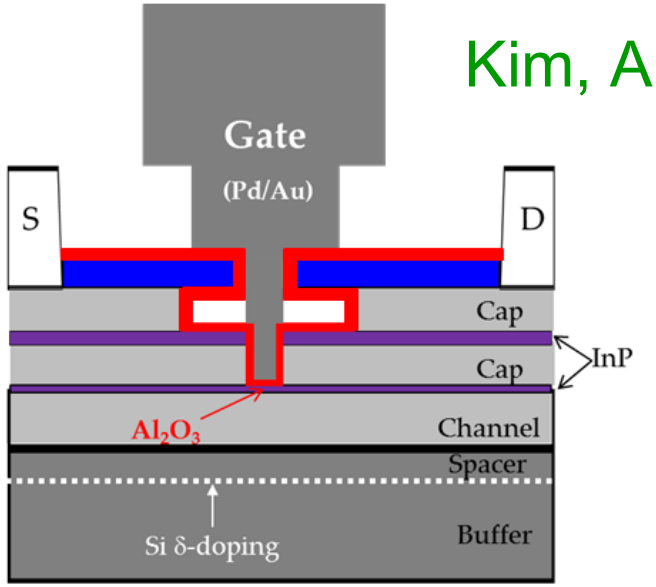
Al_2O_3 (3 nm)/InP (2 nm)/InGaAs MOSFET

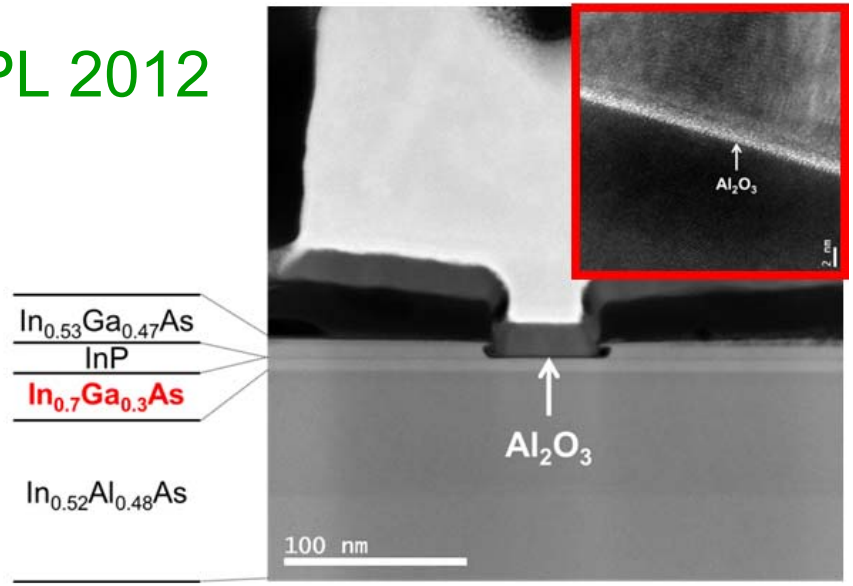
Kim, EDL 2013

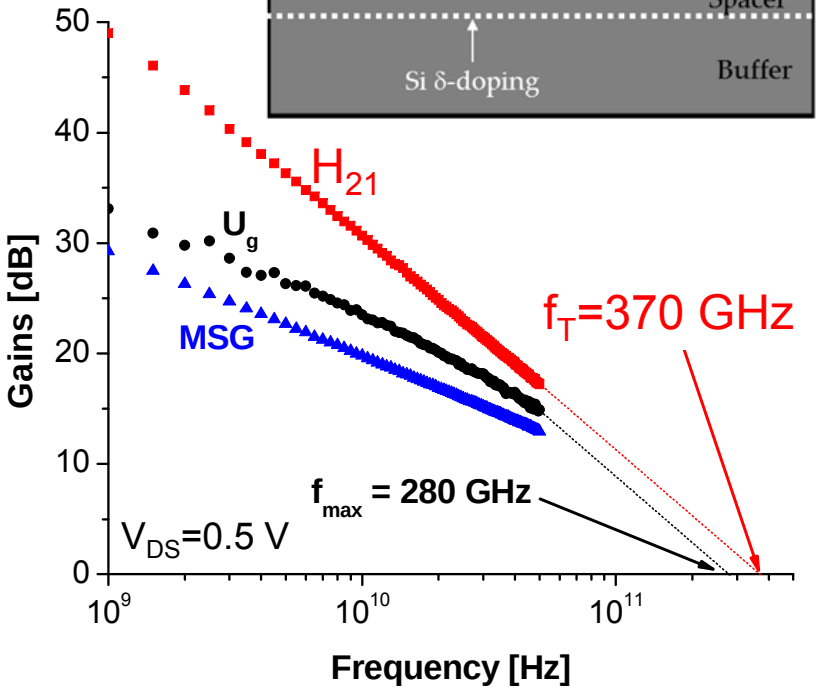
Need high-K gate dielectric: **HEMT → MOSFET!**

InGaAs MOSFETs with f_T=370 GHz
(Teledyne/MIT/IntelliEpi/Sematech)

Kim, APL 2012

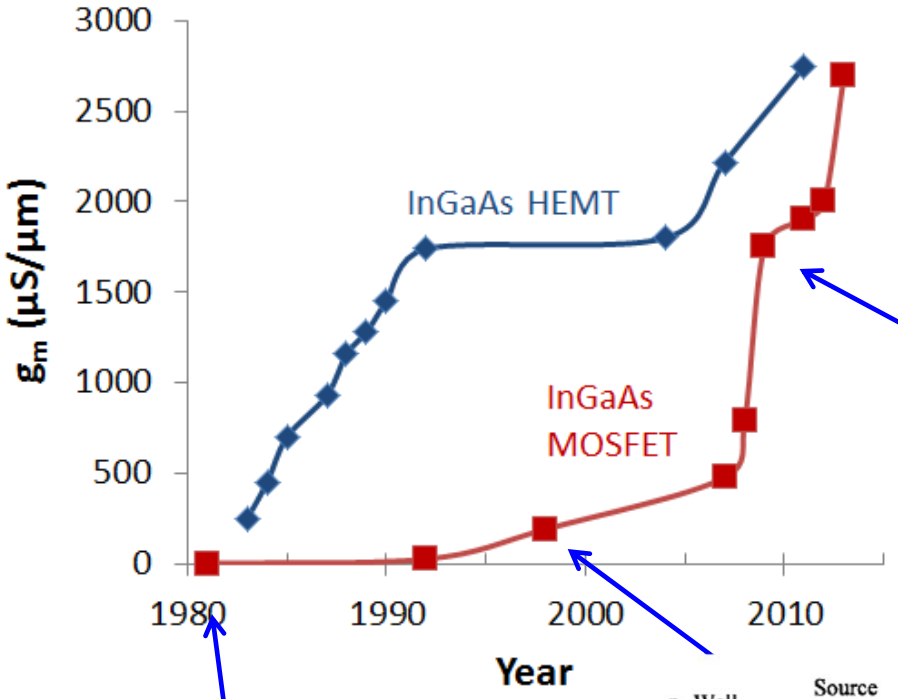


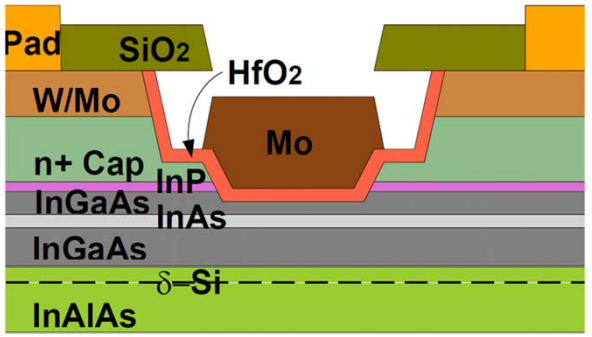




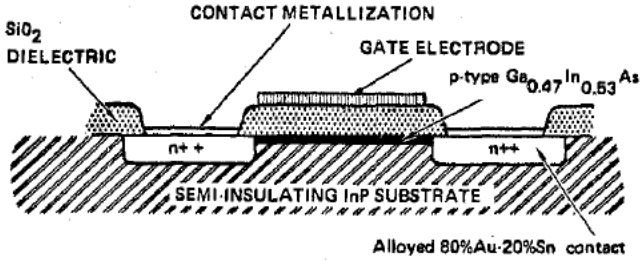
- Channel: 10 nm $In_{0.7}Ga_{0.3}As$
- Barrier: 1 nm InP + 2 nm Al_2O_3
- L_g = 60 nm
- g_m = 2 mS/μm
- R_{ON} = 220 Ω.μm

Historical evolution: InGaAs MOSFETs vs. HEMTs

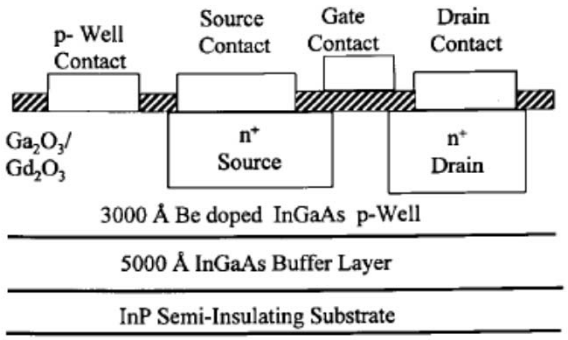




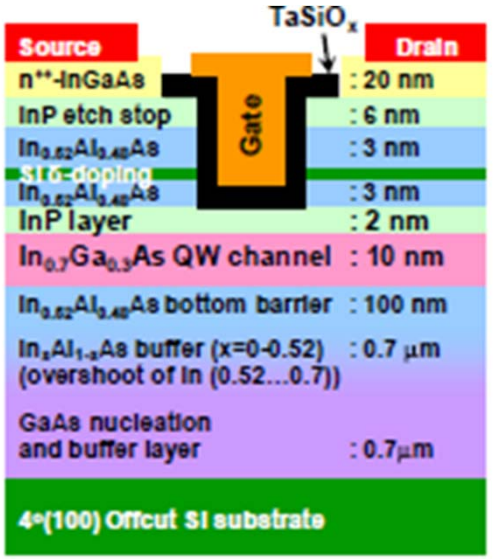
Lin, IEDM 2013



Wieder, EDL 1981



Ren, EDL 1998



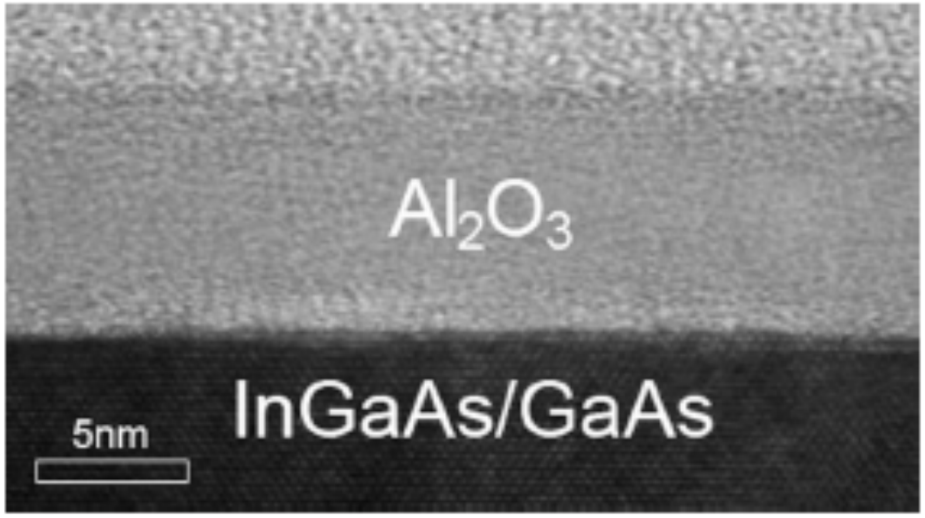
Radosavljevic, IEDM 2009

Progress reflects improvements in oxide/III-V interface

What made the difference? Oxide / III-V interfaces with unpinned Fermi level by ALD

ALD eliminates surface oxides that pin Fermi level:

- First observed with Al_2O_3, then with other high-K dielectrics
- First seen in GaAs, then in other III-Vs



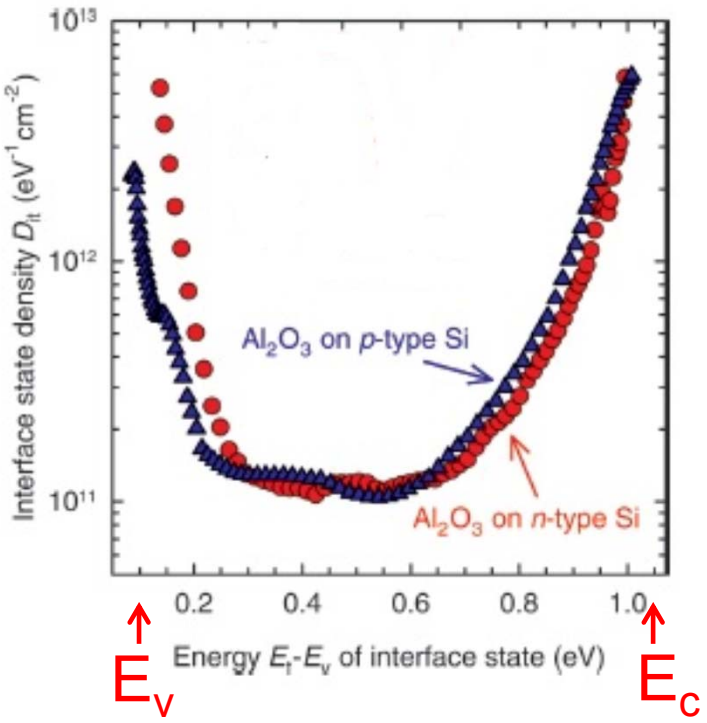
"Self cleaning"

← Clean, smooth interface without surface oxides

Huang, APL 2005

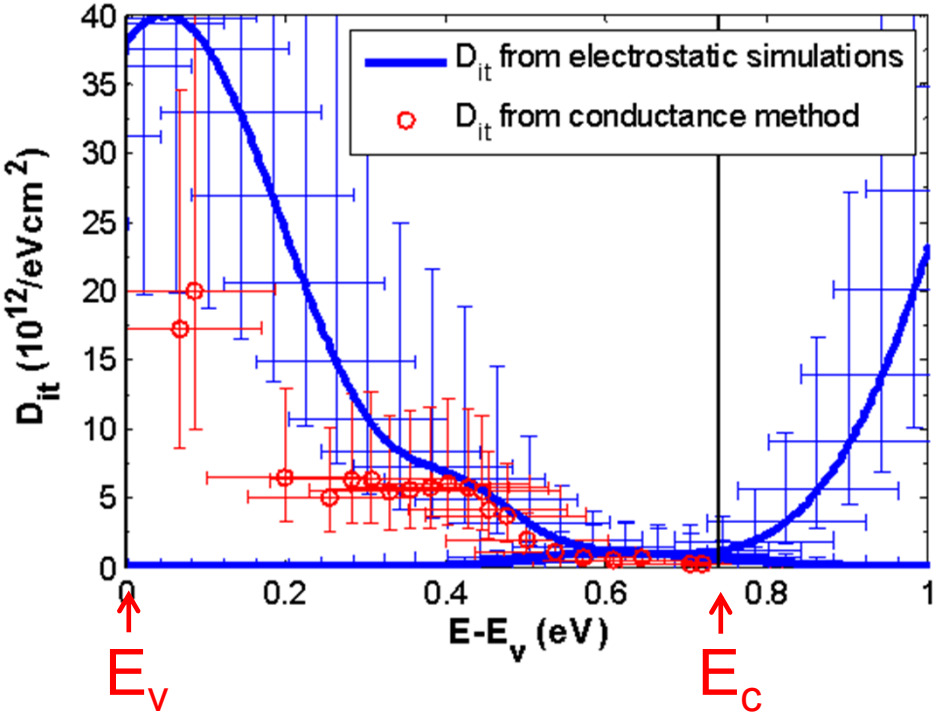
Interface quality: Al_2O_3 / InGaAs vs. Al_2O_3 / Si

Al_2O_3/Si



Werner, JAP 2011

Al_2O_3/InGaAs



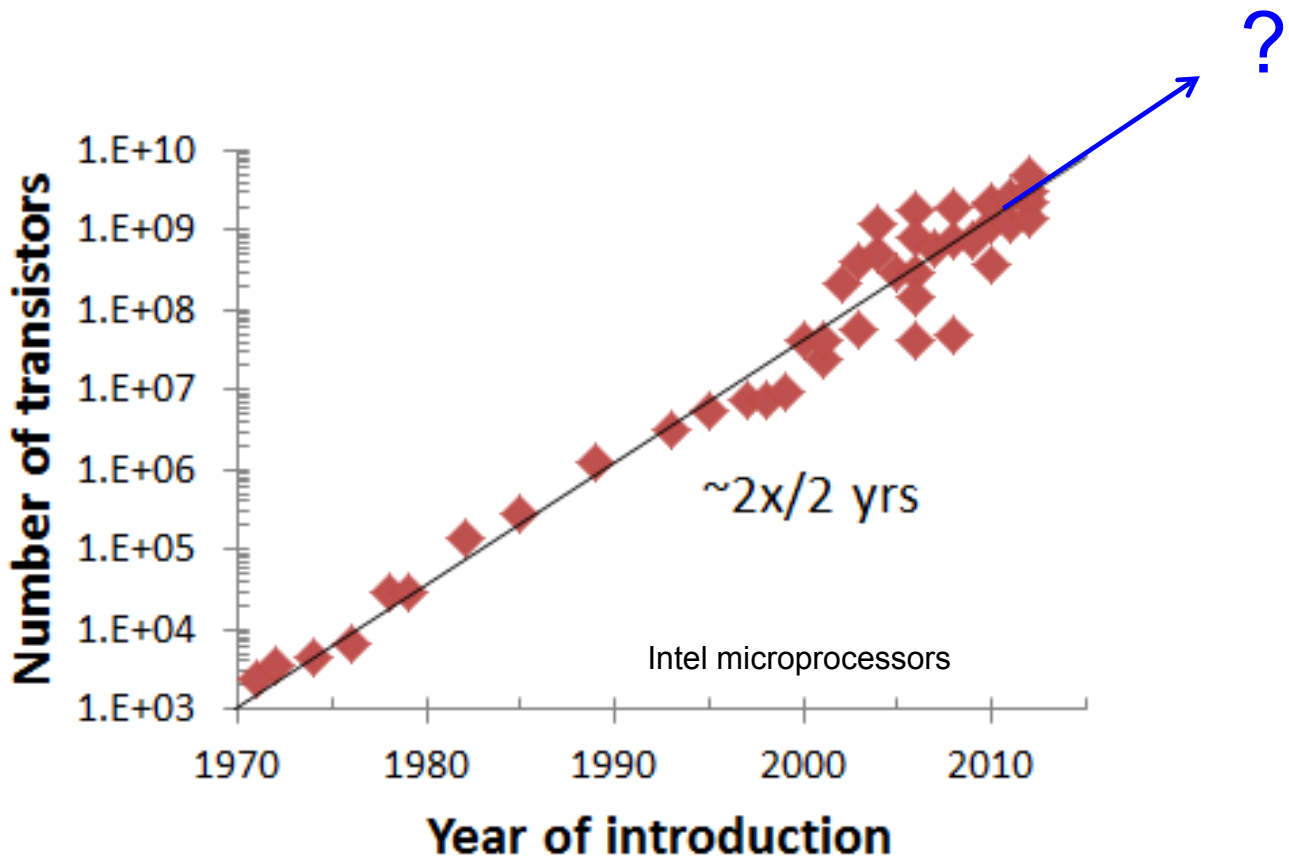
Brammertz, APL 2009

Close to E_c, Al_2O_3/InGaAs comparable D_{it} to Al_2O_3/Si interface

InGaAs n-MOSFET: best candidate for post-Si CMOS

Si CMOS scaling seriously stressed

→ Moore's law threatened

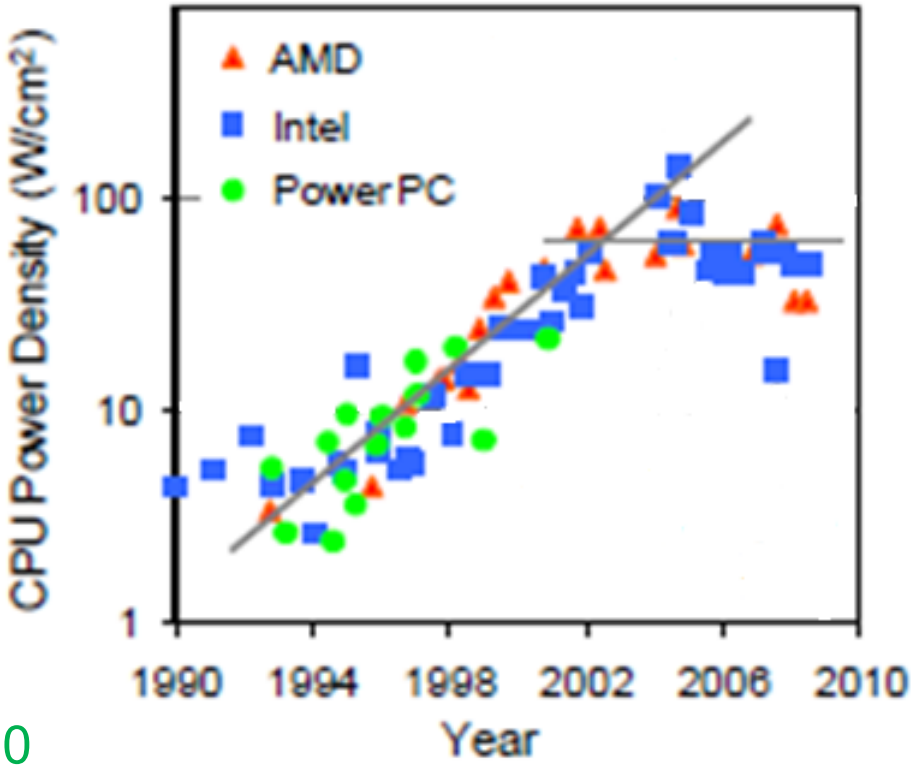



THE END IS NEAR.
YOU WISH.

CMOS scaling in the 21st century

Si CMOS has entered era of *"power-constrained scaling":*

→ Microprocessor power density saturated at ~100 W/cm^2

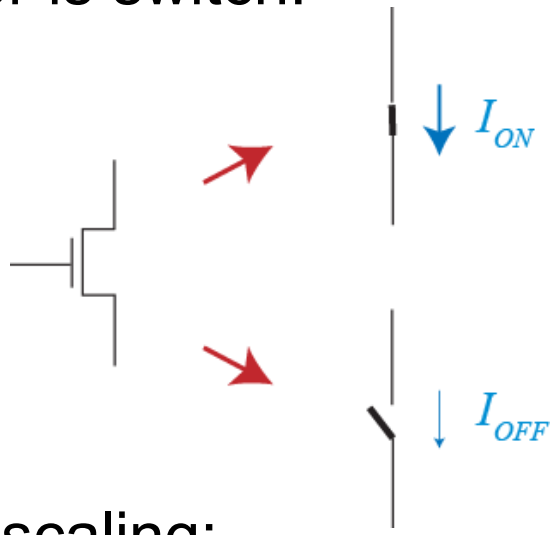


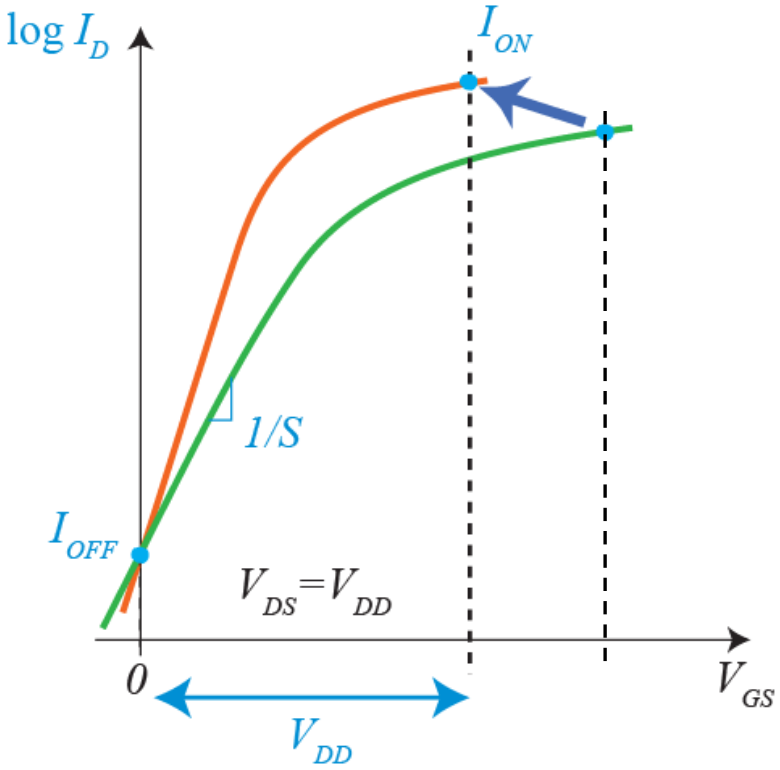
Pop, Nano Res 2010

Future scaling demands $V_{DD}\downarrow$

How to enable further V_{DD} reduction?

- Transistor is switch:





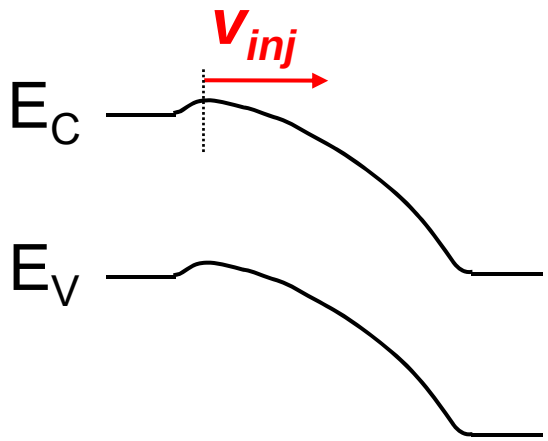
- Goals of scaling:
  - reduce transistor footprint
  - reduce V_{DD}
  - extract maximum I_{ON} for given I_{OFF}

- The path forward:
  - increase electron velocity → I_{ON} ↑
  - tighten electron confinement → S ↓

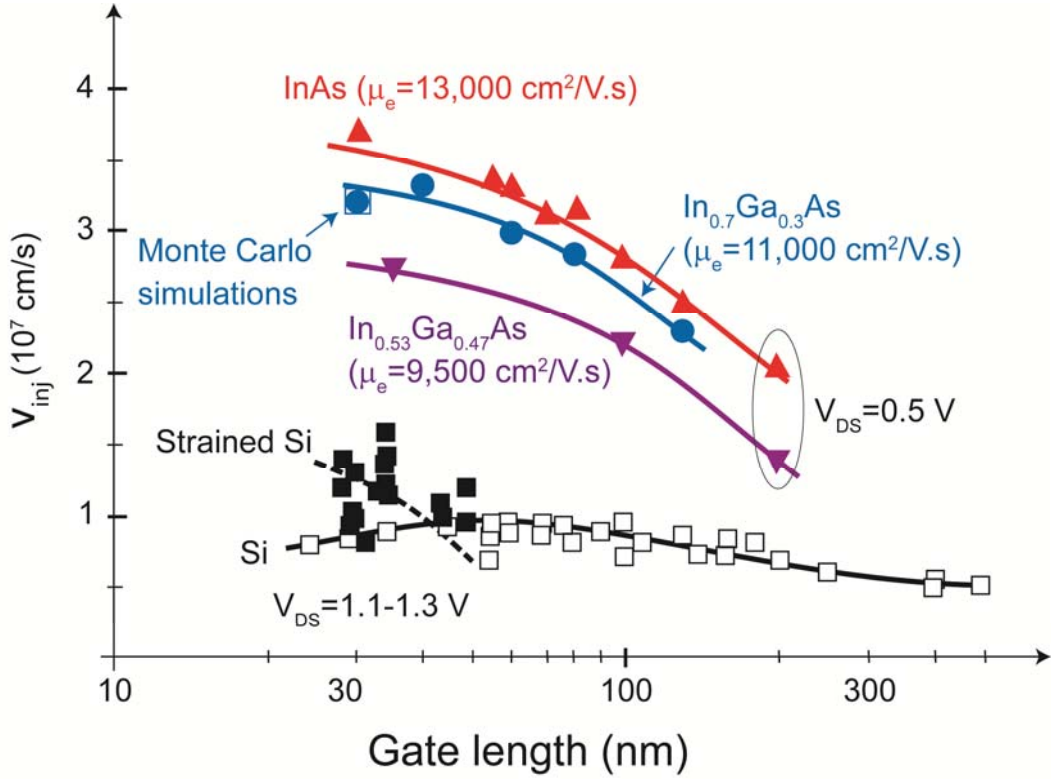
→ use InGaAs!

Electron injection velocity: InGaAs vs. Si

Measurements of electron injection velocity in HEMTs:



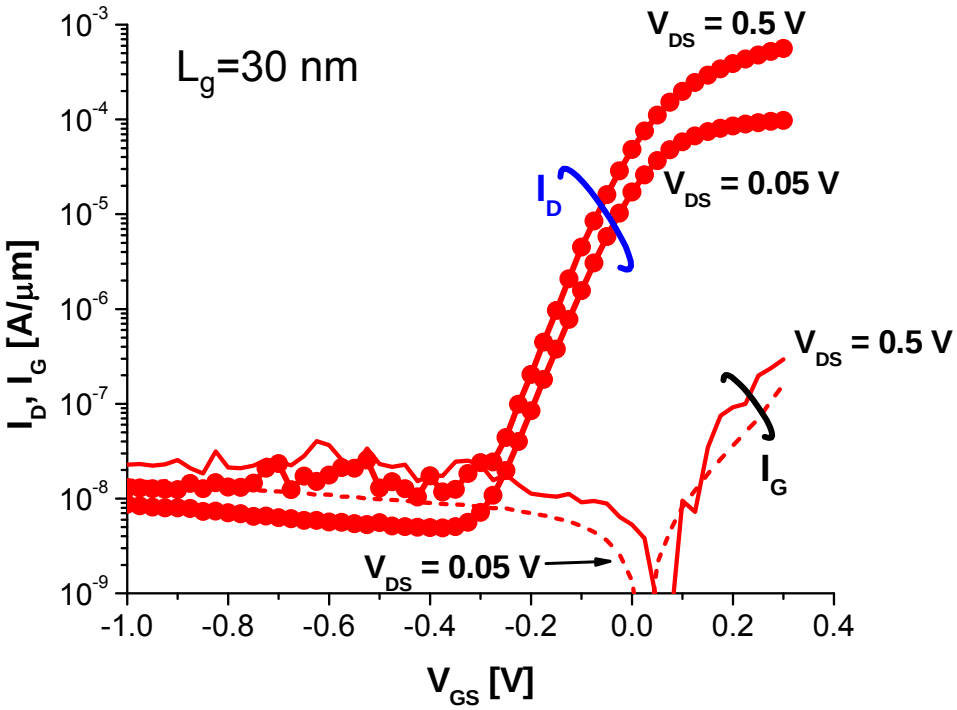
Kim, IEDM 2009
Liu, Springer 2010
Khakifirooz, TED 2008
del Alamo, Nature 2011



- v_{inj}(InGaAs) increases with InAs fraction in channel
- v_{inj}(InGaAs) > $2v_{inj}$(Si) at less than half V_{DD}
- ~100% ballistic transport at L_g~30 nm

L_g=30 nm InGaAs HEMT – Subthreshold characteristics

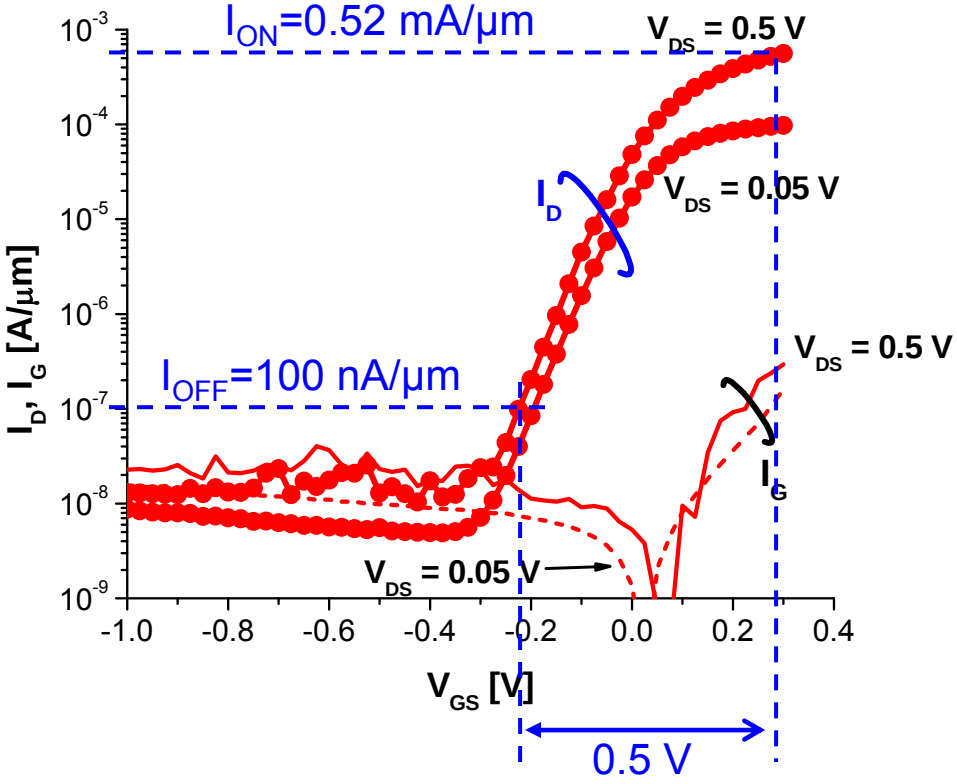
Kim, EDL 2010



- S = 74 mV/dec
- Sharp subthreshold behavior due to tight electron confinement in quantum well

L_g=30 nm InGaAs HEMT – Subthreshold characteristics

Kim, EDL 2010

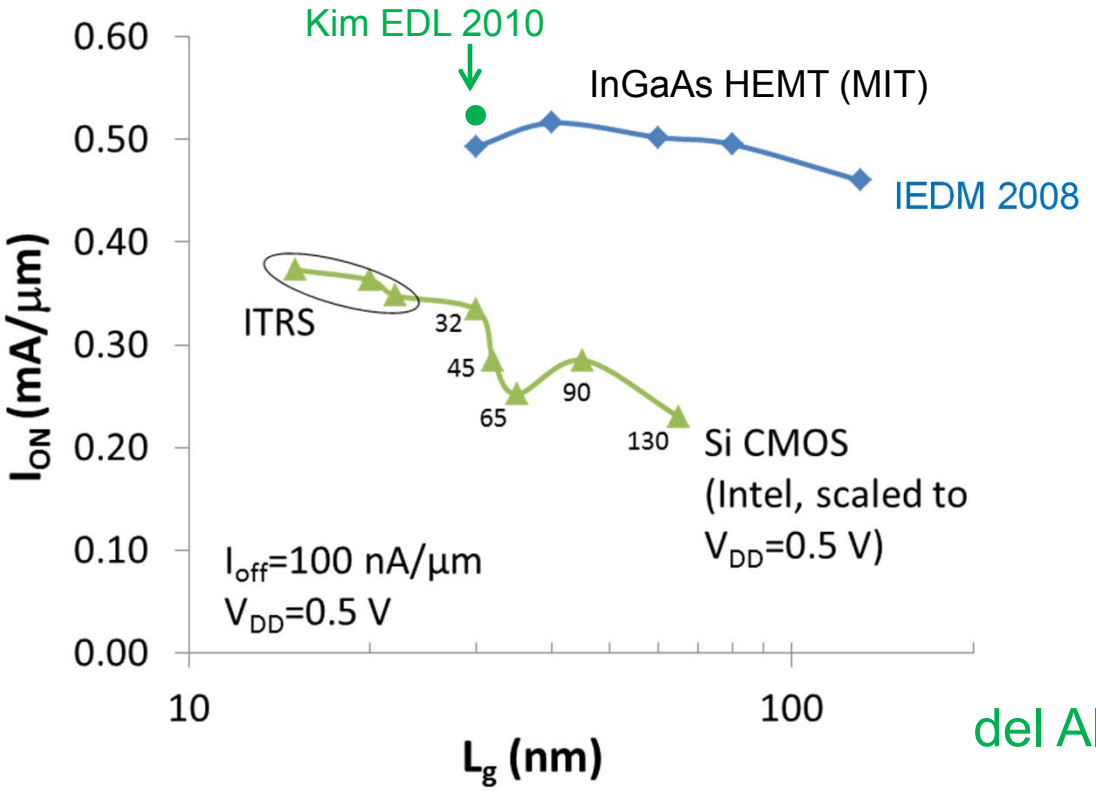


- S = 74 mV/dec
- At I_{OFF}=100 nA/μm and V_{DD}=0.5 V, I_{ON}=0.52 mA/μm

InGaAs HEMTs: Benchmarking with Si

FOM that integrates short-channel effects and transport:

I_{ON} @ I_{OFF}=100 nA/μm, V_{DD}=0.5 V



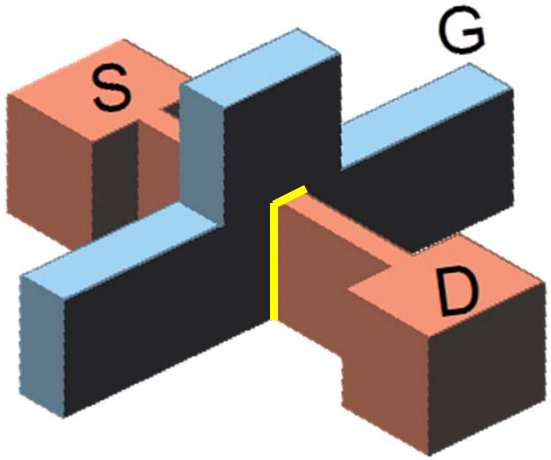
del Alamo, Nature 2011

InGaAs HEMTs: higher I_{ON} for same I_{OFF} than Si

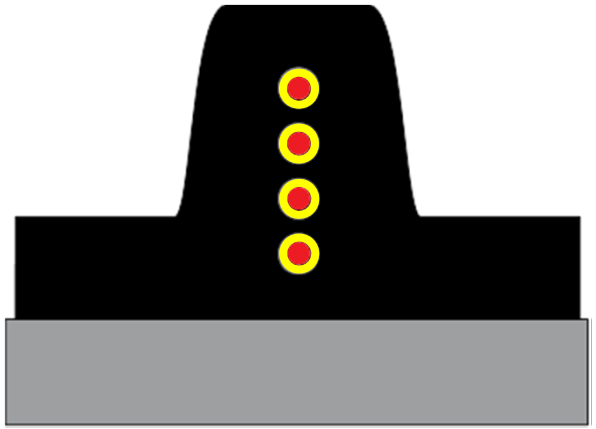
InGaAs MOSFET: possible designs

Recessed S/D QW-MOSFET

Regrown S/D QW-MOSFET



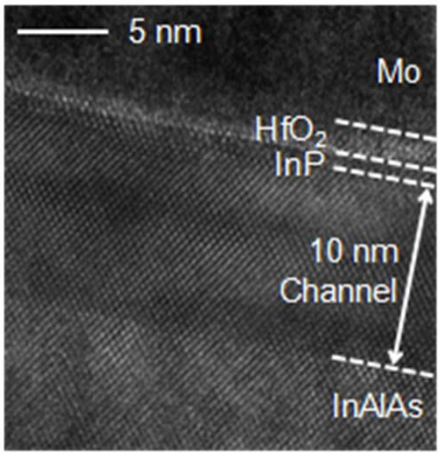
Trigate MOSFET

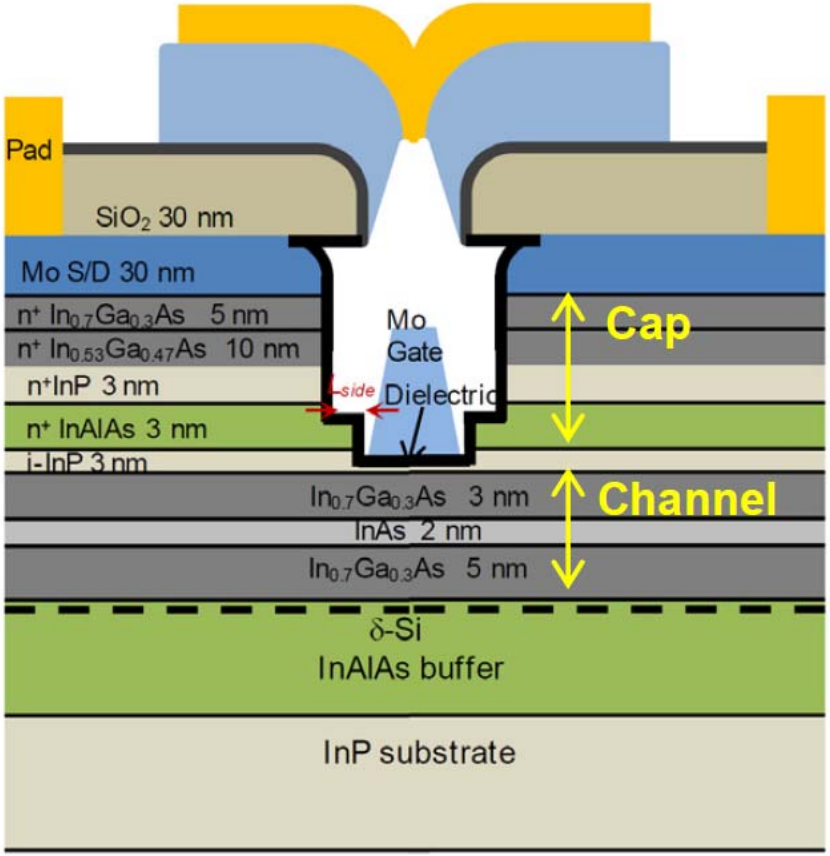


Nanowire MOSFET

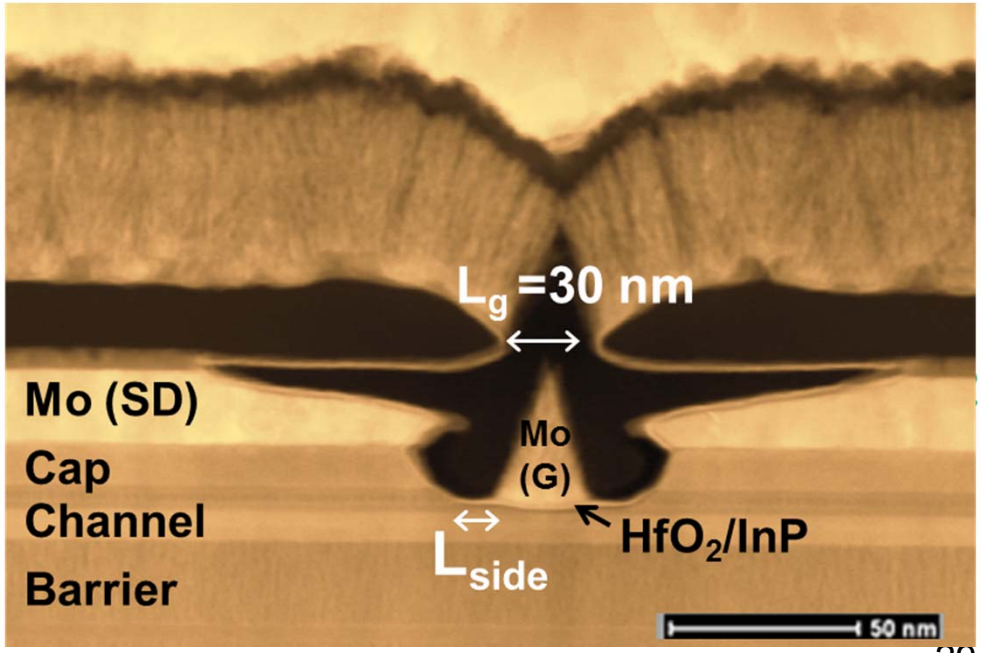
Self-Aligned InGaAs QW-MOSFETs (MIT)

- Scaled barrier (InP: 1 nm + HfO_2: 2 nm)
- 10 nm thick channel with InAs core
- Tight S/D spacing (L_{side}~30 nm)
- Process designed to be compatible with Si fab

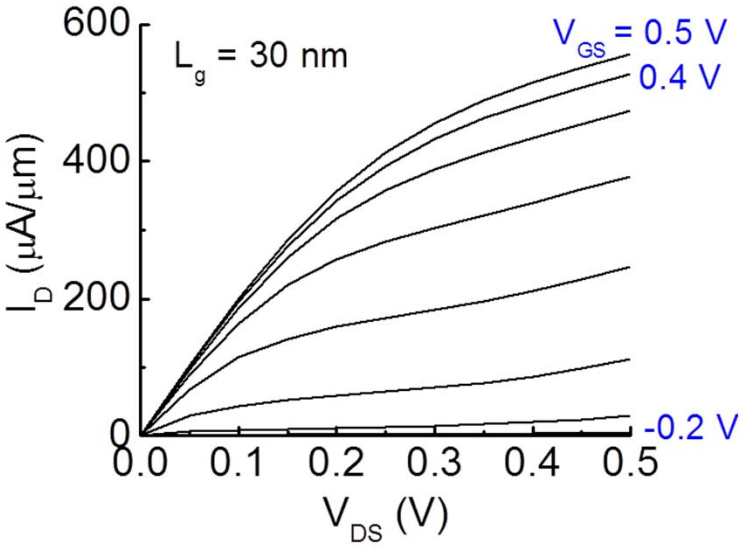


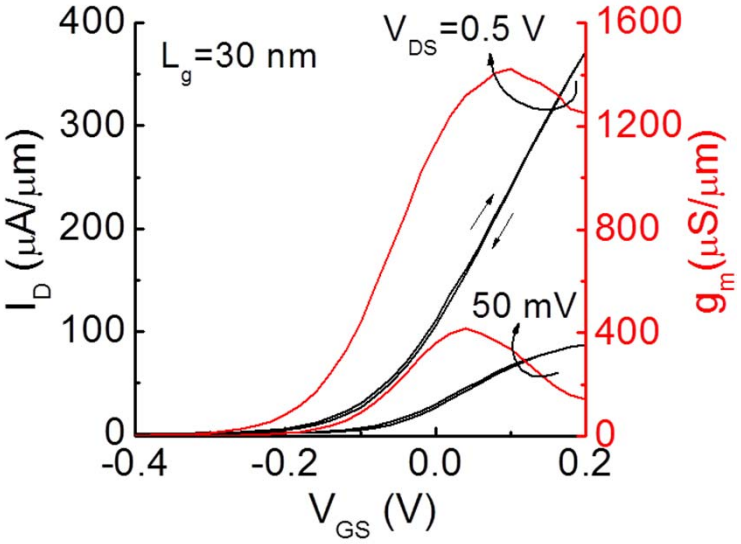


Lin, IEDM 2012



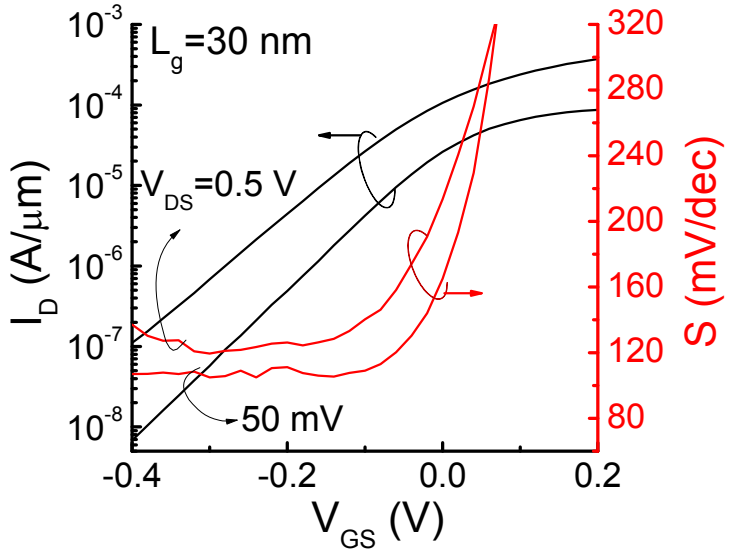
L_g = 30 nm Self-aligned QW-MOSFET





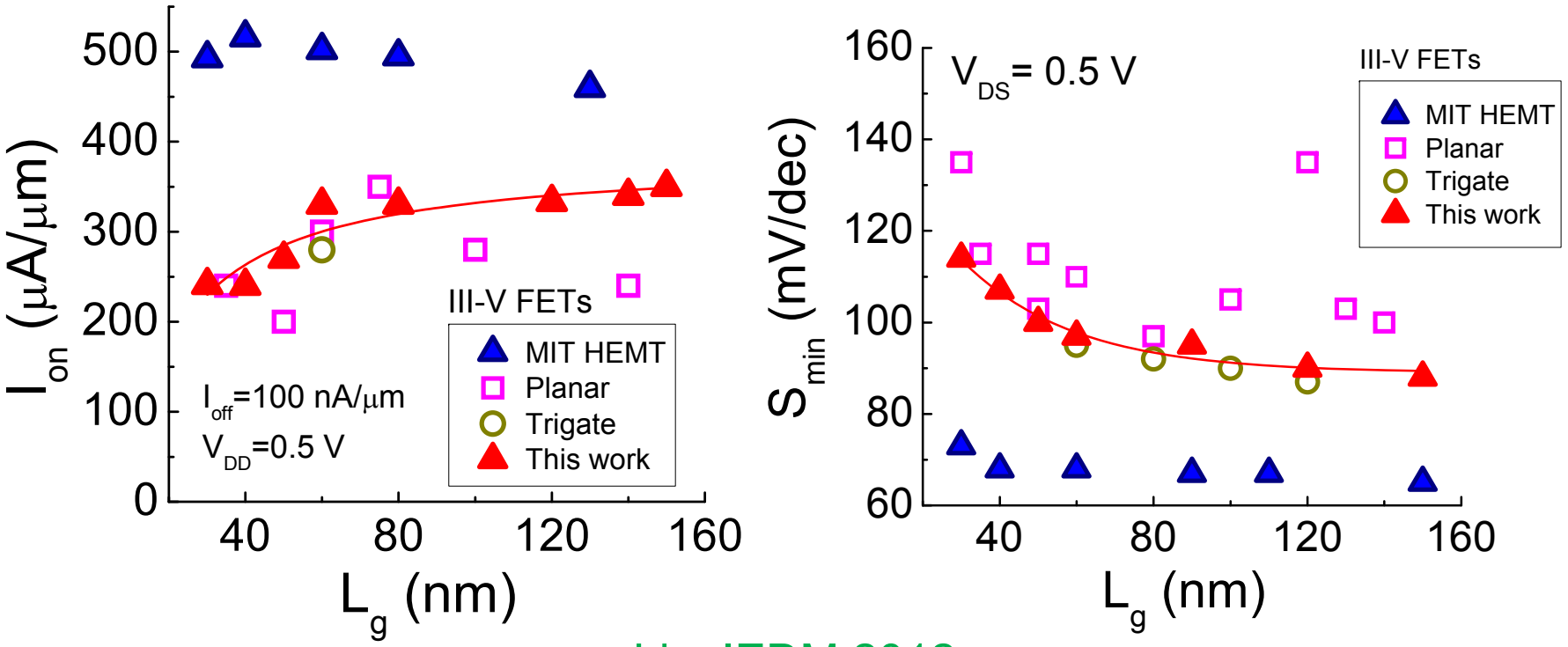
At V_{DS} = 0.5 V:

- g_m = 1.4 mS/μm
- S = 114 mV/dec
- R_{ON} = 470 Ω.μm



Lin, IEDM 2012

Scaling and benchmarking

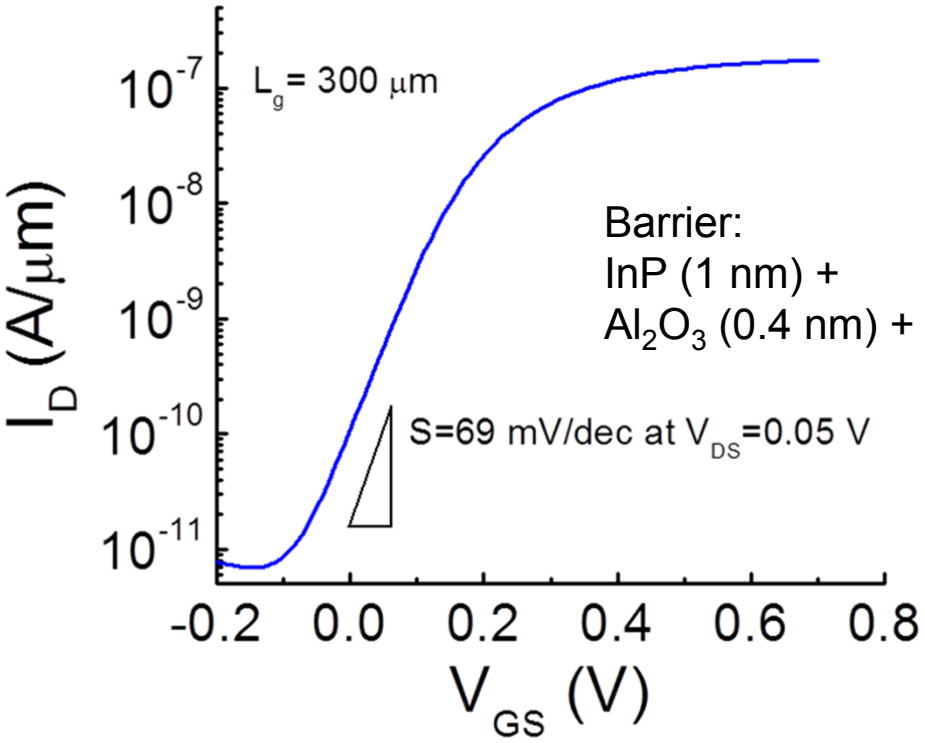


Lin, IEDM 2012

- Superior behavior to any planar III-V MOSFET to date
- Matches performance of Intel's InGaAs Trigate MOSFETs [Radosavljevic, IEDM 2011]

Sharp Subthreshold Characteristics

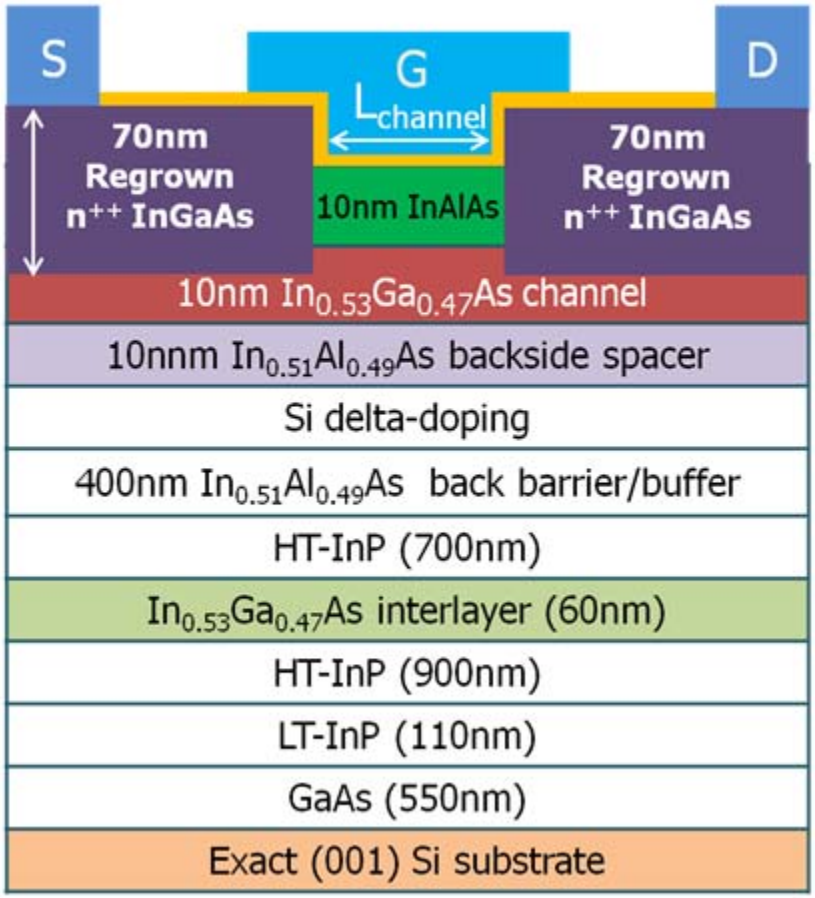
From:
- Aggressively scaled barrier
- High quality interface: gate last process

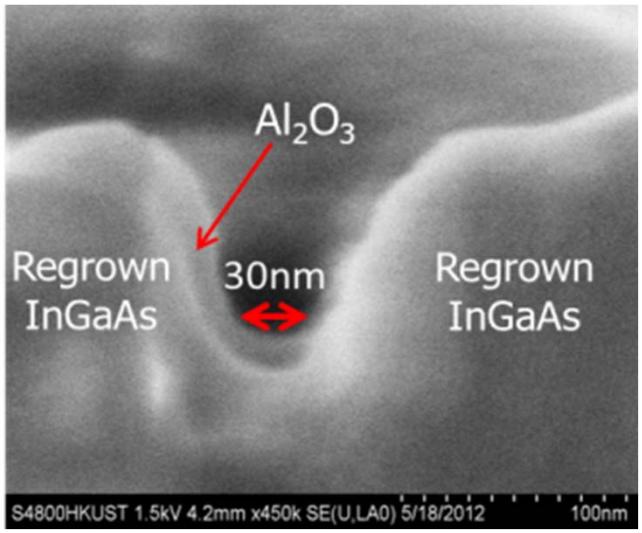


Lin, IEDM 2012

- S = 69 mV/dec at V_{DS} = 50 mV
- Close to lowest S reported in any III-V MOSFET: 66 mV/dec [Radosavljevic, IEDM 2011]

Regrown source/drain InGaAs QW-MOSFET on Si (HKUST)



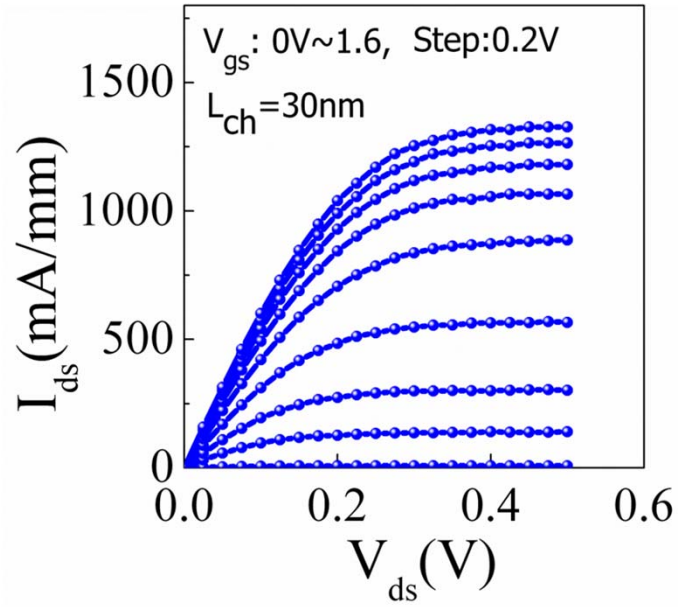


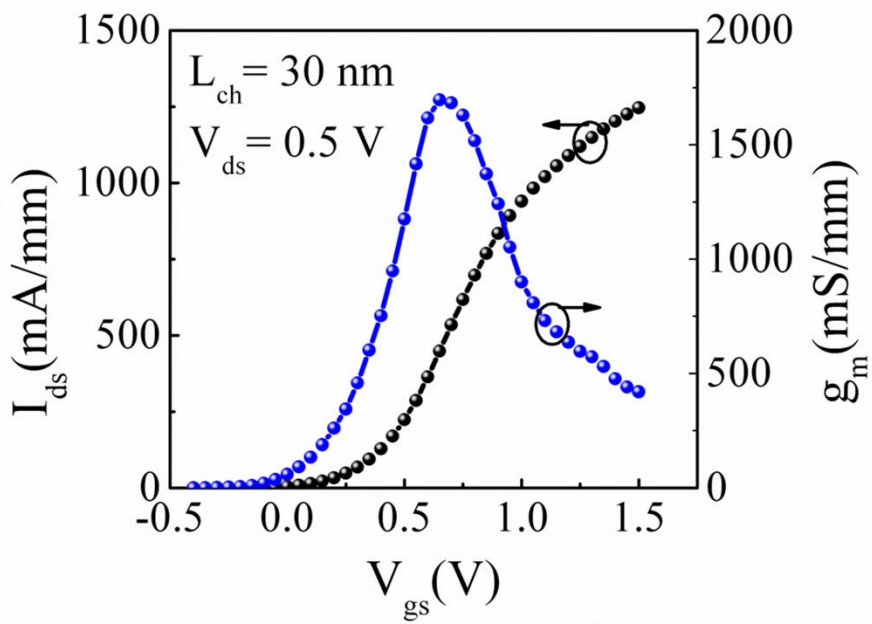
- MOCVD epi growth on Si wafer
- n^+-InGaAs raised source/drain
- Self-aligned to gate
- Composite barrier:

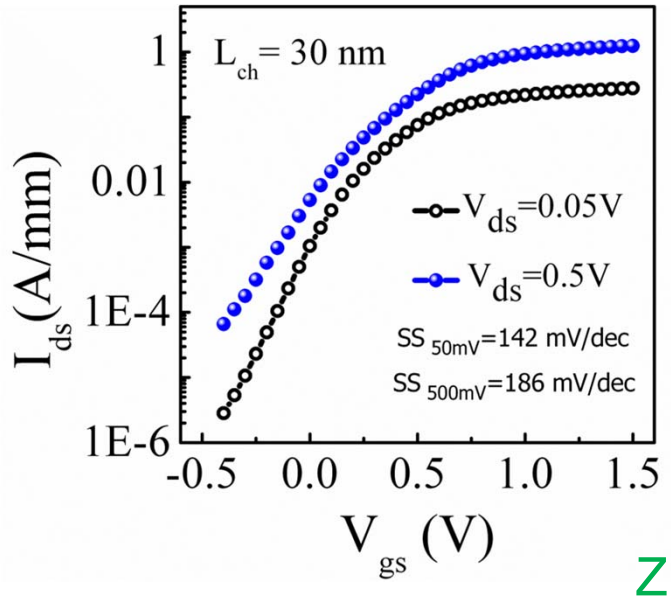
  InAlAs (10 nm) + Al_2O_3 (4.6 nm)

Zhou, IEDM 2012

Characteristics of L_g=30 nm MOSFET







At V_{DS}=0.5 V:

- g_m = 1.7 mS/μm
- S = 186 mV/dec
- R_{ON} = 157 Ω.μm

Zhou, IEDM 2012

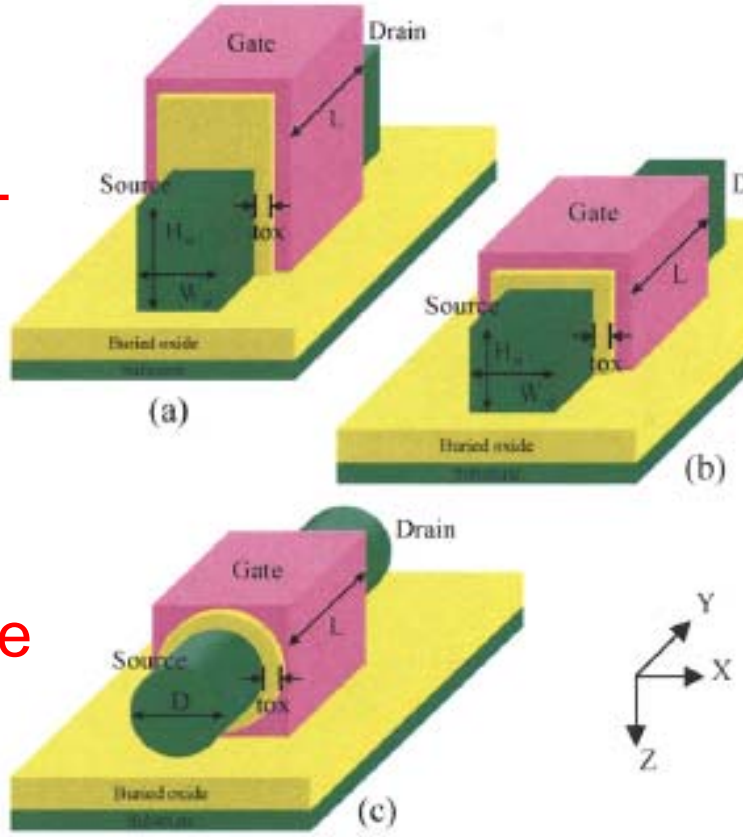
Multiple-gate MOSFETs

gates ↑ → improved electrostatics → enhanced scalability

FinFET

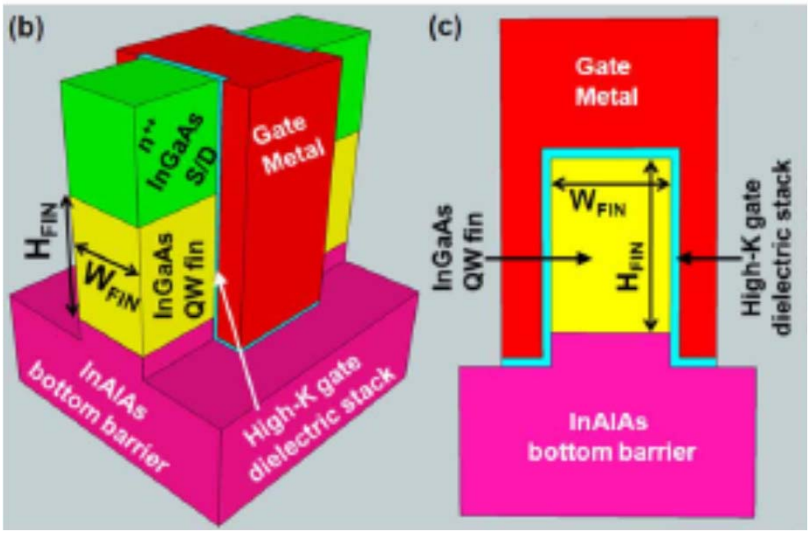
Trigate

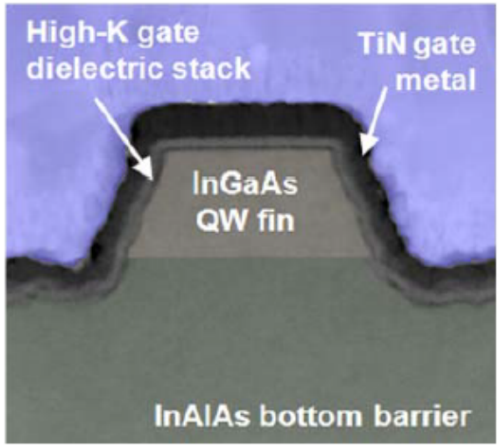
Nanowire



Chen, ICSICT 2008

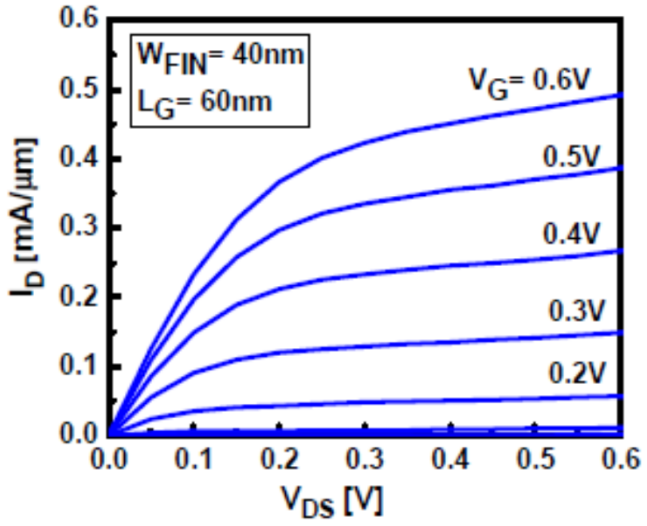
InGaAs Trigate MOSFET (Intel)

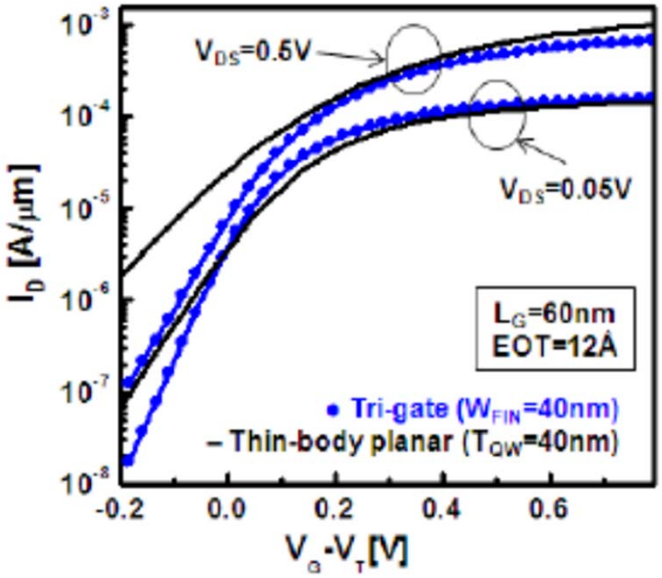




H_{FIN}=40 nm

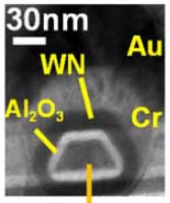
Radosavljevic, IEDM 2011



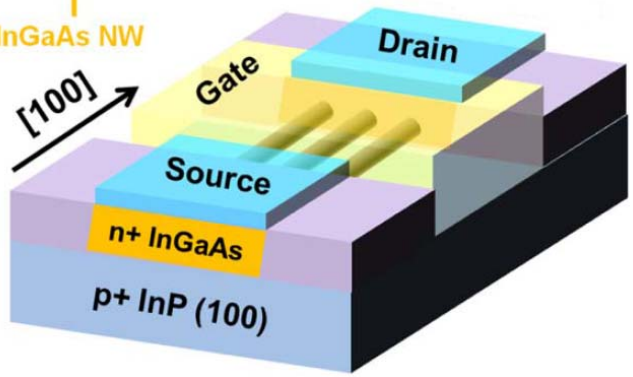


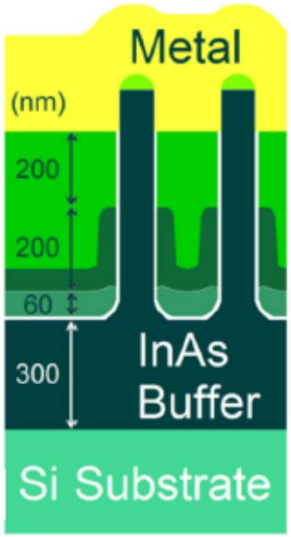
Improved S over planar MOSFET on same heterostructure

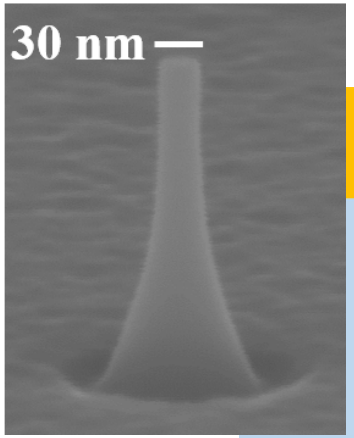
InGaAs Nanowire MOSFETs



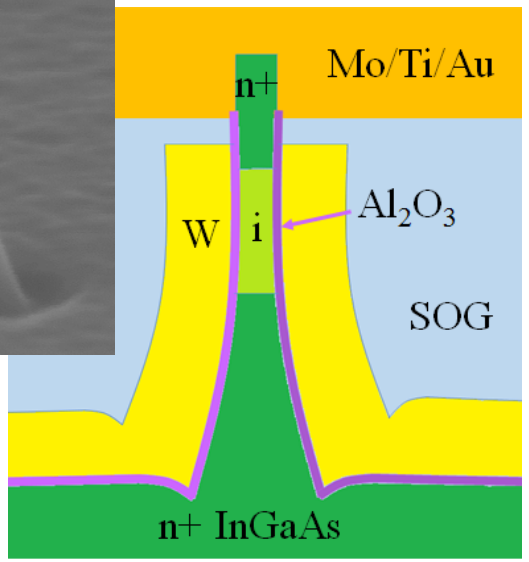
D = 20 nm

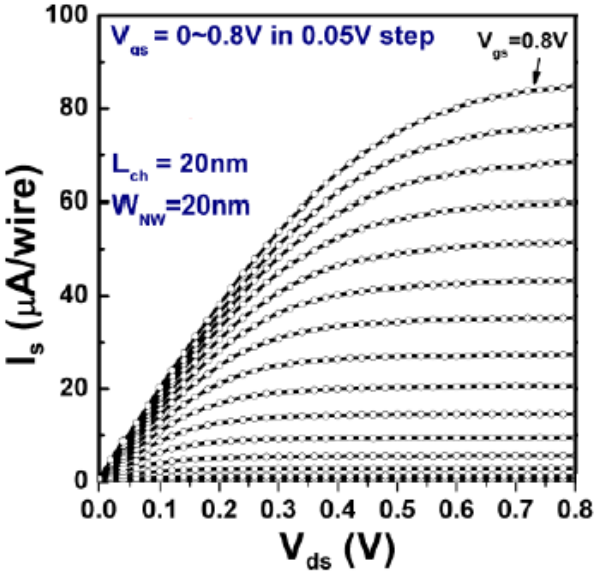




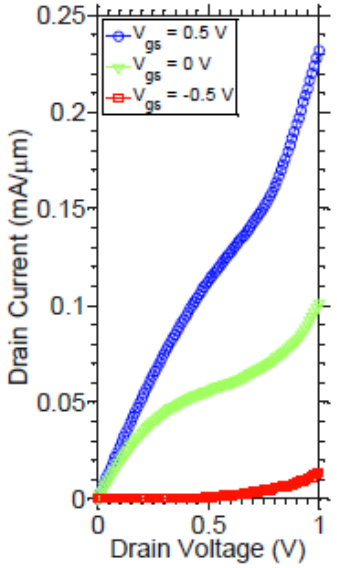


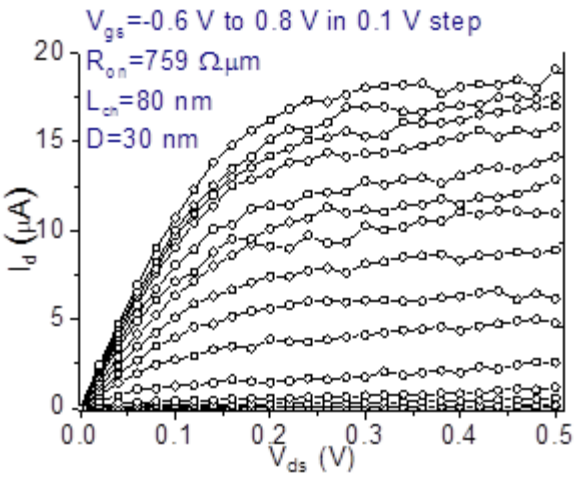
D = 30 nm





D = 28 nm





Gu, IEDM 2012

Persson, DRC 2012

Zhao, IEDM 2013

Conclusions: exciting future for InGaAs

- Most promising material for ultra-high frequency and ultra-high speed applications

  → first THz transistor?

- Most promising material for n-MOSFET in a post-Si CMOS logic technology

  → first sub-10 nm CMOS logic?

- InGaAs + Si integration:

  → THz + CMOS + optics integrated systems?