Nanometer-scale InGaAs Field-Effect Transistors for THz and CMOS technologies

J. A. del Alamo
Microsystems Technology Laboratories, Massachusetts Institute of Technology,
Rm. 39-567, Cambridge, MA 02139, USA

Abstract— Integrated circuits based on InGaAs Field Effect Transistors are currently in wide use in the RF front-ends of smart phones and other mobile platforms, wireless LANs, high data rate fiber-optic links and many defense and space communication systems. InGaAs ICs are also under intense research for new millimeter-wave applications such as collision avoidance radar and gigabit WLANs. InGaAs FET scaling has nearly reached the end of the road and further progress to propel this technology to the THz regime will require significant device innovations. Separately, as Si CMOS faces mounting difficulties to maintain its historical density scaling path, InGaAs-channel MOSFETs have recently emerged as a credible alternative for mainstream logic technology capable of scaling to the 10 nm node and below. To get to this point, fundamental technical problems had to be solved though there are still many challenges to be addressed before the first non-Si CMOS technology becomes a reality. The intense research that this exciting prospect is generating is also reinvigorating the prospects of InGaAs FETs to become the first true THz electronics technology. This paper reviews progress and challenges of InGaAs-based FET technology for THz and CMOS.

I. INTRODUCTION

InGaAs is a relatively well known material [1]. $In_xGa_{1-x}As$ is a ternary alloyed semiconductor that mixes GaAs and InAs. As the InAs composition changes from 0 to 100%, the optical and electronic properties of InGaAs change widely. This makes it a rather versatile material with a wide range of applications. Our interest in this paper is the unique electronic properties of InGaAs, in particular, its extraordinary electron transport characteristics. The room temperature electron mobility of InGaAs ranges, depending on composition and strain, from about 6,000 to 30,000 $cm^2/V.s$ at room temperature. This makes InGaAs singular for transistor applications. Over the years, InGaAs MESFETs, JFETS, HEMTs and HBTs have all been demonstrated.

In this paper, we initially focus our attention on InGaAs High-Electron Mobility Transistors (HEMTs) that take advantage of bandgap engineering and advanced heteroepitaxial growth techniques. InGaAs HEMTs are relatively well established devices with superb high frequency and low noise characteristics. While the markets are not very large, significant commercial applications exist. At the frontiers of high frequency operation, InGaAs HEMTs enable signal amplification at frequencies in excess of 500 GHz. In the quest for active circuits that operate in the THz regime, InGaAs HEMTs are positioned like no other device.

This paper charts the progress of InGaAs HEMTs in its march towards THz operation. It argues that without a drastic device redesign, the potential for significant further enhancements in frequency response is rather limited. It also argues that recent demonstration of the feasibility of high-quality metal-oxide-semiconductor structures involving high dielectric constant ("high-K") dielectrics represents a breakthrough that opens new avenues for InGaAs to reach the THz frontier. Possible future THz InGaAs-based FET device designs are discussed.

What makes InGaAs attractive for THz applications has also caught the attention of the IC industry as it searches for a path forward for Moore's Law. The increasing difficulty of Si transistors to support the historical rate of progress of CMOS scaling has prompted the identification of alternative channel materials. In the last few generations of CMOS technology, Si transistors have shed their traditional polysilicon gate and even the use of SiO_2 as gate dielectric. Instead, they have turned to metal gates and high-K dielectrics as a way to address the limitations of the conventional logic MOSFET design. Continued progress is seen ahead if the Si channel itself is substituted by a high mobility material so that greater performance, i.e. current density, can be obtained out of a given footprint and a tolerable parasitic load in the form of off-current, parasitic resistance and capacitance. It is in this role of alternative channel material of a future logic n-type MOSFET that InGaAs looks very attractive [2].

An impediment to earlier efforts to develop MOSFETs based on III-V compound semiconductors was Fermi level pinning at the dielectric/semiconductor interface. This is the results of the high density of interfacial defects that prevents the modulation of the surface potential by a metal gate. For years, this problem seemed fundamental. However, in the last few years, there have been many demonstrations of Fermi-level unpinned oxide/III-V interfaces that strongly suggest that this is an eminently engineerable problem. Of even greater significance is the fact that some of these techniques are manufacturable, such as Atomic Layer Deposition (ALD) [3]. This has spurred a veritable race to demonstrate nano-scale InGaAs MOSFETs suitable for sub-10 nm CMOS.

This paper reviews recent advances of InGaAs MOSFETs for CMOS and outlines some of the challenges that lie ahead. Interestingly, what has made the notion of an InGaAs

MOSFET possible, a high-quality oxide/InGaAs interface, also represents a fresh opportunity for THz device design. The intense effort to develop InGaAs MOSFETs for logic is also generating new process technology, modeling tools, and basic physics and materials understanding that should propel this technology through the THz frontier.

II. Towards THz InGaAs FETs

InGaAs-based High Electron Mobility Transistors (HEMT) have been around for some time. The very first HEMT was demonstrated in the AlGaAs/GaAs system now more than 30 years ago [4]. The first InGaAs-channel HEMT followed soon after that in the InAlAs/InGaAs system lattice-matched to InP (InAs composition in the $In_xGa_{1-x}As$ channel is 53%) [5]. The first AlGaAs/InGaAs pseudomorphic HEMT (PHEMT) on the GaAs system (x=15% in the channel) saw the light just a few years later [6]. If we fast forward to today, InGaAs HEMT electronics is a relatively mature technology with >$1B/yr business [7]. InGaAs PHEMTs are used in the power amplifiers of many smart phones, in very high speed fiber optic systems and in millimeter-wave systems, such as collision avoidance radar [7]. Commercial processes that integrate Enhancement-Mode and Depletion-Mode InGaAs PHEMTs as well as InGaAs Bipolar Transistors are available today in foundry basis [8]. These processes enable highly integrated mixed-signal sub-systems such as single-chip WLAN MMICs [9].

At the high-frequency end, InGaAs HEMTs display today unparalleled performance. The record f_{max} (a power-gain cut-off frequency) is held by InGaAs HEMTs [10], the record f_T (current-gain cut-off frequency) now exceeds 700 GHz [11] and although InGaAs Heterojunction Bipolar Transistors have a slight edge on absolute f_T [12], this comes at the price of a fairly low f_{max}. InGaAs HEMTs have been demonstrated in which both f_T and f_{max} are above 688 GHz [13]. A device technology that features both high f_T and f_{max} is versatile and can be used for many different kinds of circuits that operate at very high frequencies. When it comes to ultra-high frequency operation, InGaAs HEMTs reigned unrivaled.

Fig. 1 shows the evolution of record current-gain cut-off frequency f_T of InGaAs HEMTs. If we consider GaAs as $In_xGa_{1-x}As$ with x=0, the first few years in this graph correspond to GaAs devices on GaAs substrate. Since the first demonstration of InAlAs/InGaAs HEMTs on InP substrate, this family of devices have held the record ever since. This extraordinary frequency capability has resulted in impressive circuit demonstrations such as a 10-stage 670 GHz Low-Noise Amplifier [14]. The technology has also attained unprecedented reliability with InGaAs HEMTs on InP having been used in major space missions such as the Wilkinson Microwave Anisotropy Probe that obtained a full-sky map of the Cosmic Microwave Background radiation with unprecedented resolution [15].

It is of interest to look at modern InGaAs HEMTs and to speculate about what it takes to achieve a device with f_T= 1 THz. An analysis of a device family that attained 688 GHz at

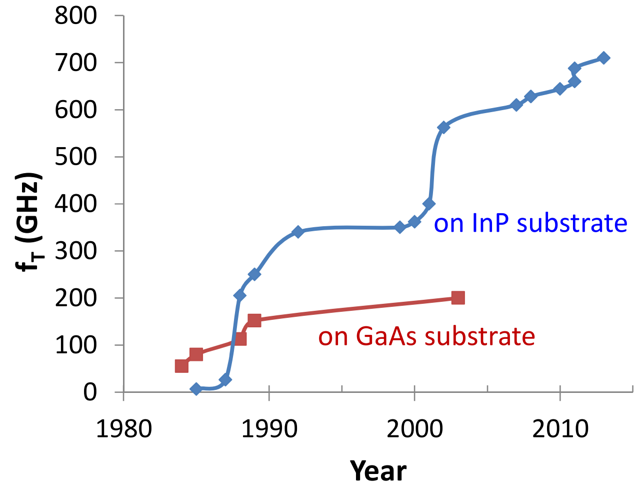

Figure 1. InGaAs HEMT record f_T vs. year.

L_g=40 nm suggests that f_T=1 THz is possible if the gate length is scaled to 25 nm and parasitic resistance and capacitance is reduced by 30%. Is this feasible?

A way to ascertain this is to look at the progression of device design in the last 30 years [16]. When we examine the evolution of gate length, channel InAs composition, channel thickness and gate barrier thickness for the record devices, it becomes clear that device design has essentially stagnated in the last 10 years or so. This suggests that little further progress seems possible in the future.

The reason for this lies in the difficulty of scaling the barrier thickness due to gate leakage current. As is well known, device scaling must take place in a harmonious way with a good balance between the horizontal and lateral dimensions. In the last few years, barrier thickness scaling has stalled with a minimum value of 4 nm having been stable for some time [16]. What prevents further barrier thickness scaling is a rapidly increasing gate leakage current, as illustrated in Fig. 2 for a family of identical InGaAs HEMTs in which the InAlAs barrier has been recessed to a different final thickness [17]. As the InAlAs barrier thickness is reduced, the gate current increases exponentially. From this graph we can conclude that modern InGaAs HEMTs have essentially reached the limit of scaling and further progress for this device design will be at best incremental.

Gate leakage current is a problem in HEMTs because the barrier material has a relatively small bandgap. A possible solution to this problem lies in the use of a much wider bandgap barrier, such as an oxide. This can suppress gate leakage current and enable reductions in oxide thickness which in turn, allows further scaling of the lateral device dimensions. Indeed, Fig. 2 shows that by inserting 3 nm of Al_2O_3, the gate leakage current can be suppressed by five orders of magnitude [17].

InGaAs Quantum-Well MOSFETs (QW-MOSFETs) have been demonstrated recently with excellent frequency response.

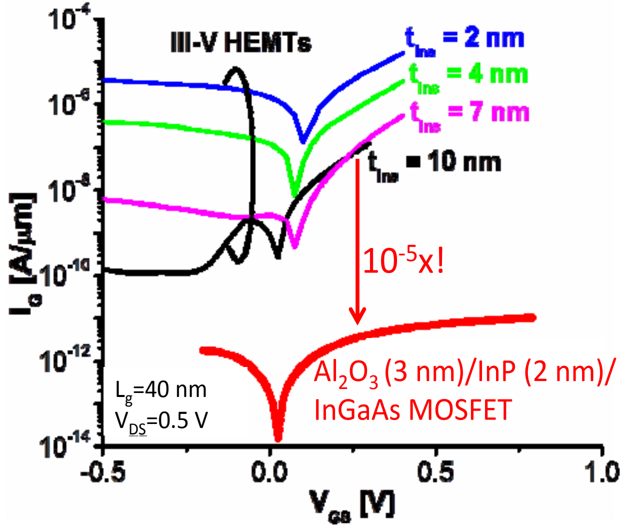

Figure 2. Gate leakage current of L_g=40 nm InGaAs HEMTs and MOSFETs. As the thickness of InAlAs barrier in HEMTs scales down, the gate leakage current increases exponentially. The introduction of a thin dielectric layer suppresses gate leakage current by several orders of magnitude [17].

An f_T of 370 GHz has recently been attained on devices with L_g=60 nm [18]. Undoubtly, rapid improvements lie ahead. The elimination of the wide bandgap barrier brings an additional bonus and that is the reduction in parasitic resistance. In a HEMT, the barrier that separates the channel from the gate also separates the contacts from the gate. Inevitably, this barrier contributes to contact resistance. The use of a dielectric barrier allows a different epitaxial design in which the ohmic contacts are in much better communication with the channel. In fact, in the devices in [18], the ON resistance is 220 Ω.μm while in most HEMTs it can be substantially higher than that.

There is something remarkable about this achievement. A III-V MOSFET has been pursued for over 30 years. If Si MOSFETs worked so well, III-V MOSFETs should work even better, or so was the thinking. Claims of working III-V MOSFETs date back from as early as 1965 [19]. Yet, in spite of strong interest, III-V MOSFETs never became a mature commercial technology. The reason lies in Fermi level pinning at the oxide-semiconductor interface caused by high interface state density. This effectively prevents the modulation of the surface potential inside the device and results in poor performance. In addition, the charging and discharging of the interface states results in severe device instability.

What has changed? In 1997 it was shown that the in-situ growth of Ga_2O_3/Gd_2O_3 on GaAs resulted in a Fermi level unpinned interface [20]. This was a real breakthrough since by then, this was thought not to be possible. More significantly, in 2003, Al_2O_3 deposited by ALD an ex-situ technique, also yielded an excellent interface on GaAs [3]. This was soon observed with other oxides and III-V semiconductors. This remarkable finding is attributed to the so-called "self-cleaning" that takes place in the early stages of ALD in which the native oxides responsible for Fermi level pinning are reduced and new interfacial bonding is created that yields a very low interface state density. The results have been particularly impressive for InGaAs in which interface state densities in the mid-10^{11} to mid-10^{12} $cm^{-2}eV^{-1}$ have been demonstrated close to the conduction band edge. This all of a sudden makes n-channel MOSFETs possible.

In the last few years, the distinct prospect of InGaAs MOSFETs has reignited the interest on their use in logic circuits. This has coincided with mounting difficulties for Si CMOS to continue its historical scaling path ("Moore's Law"). How InGaAs has come to be seen as a credible candidate that might enable a few more generations of CMOS is discussed in the next section.

III. Towards InGaAs MOSFETs for CMOS

The first indication that InGaAs-based heterostructure field-effect transistors were endowed with unique potential for logic applications was presented in 2005 [21]. It was shown that InGaAs HEMTs that had been designed for high-frequency applications exhibited outstanding subthreshold characteristics and current drive that projected to gate delays that should be significantly better than those of Si MOSFETs. Prior to this, there had been some work concerning the use of III-V compound semiconductors in the channel of future CMOS but the interest had centered around InSb [22]. InSb is a material with outstanding electron transport characteristics but very narrow bandgap and large lattice constant, two significant difficulties.

Subsequent work focused on InGaAs HEMT optimization with emphasis on logic figures of merit, that is, gate length scaling, current drive and short-channel effects. It was found that through a combination of channel composition design, and channel and barrier thickness scaling, outstanding overall logic performance could be obtained [23-26]. At the root of these promising characteristics was the large velocity of electrons in the channel, particularly for InAs-rich channels [27]. In addition, the electron effective mass in the channel was found to be larger than the bulk value due to strong quantization, non-parabolicity and biaxial compressive stress [28]. This dispelled fears that for low voltage operation, InGaAs-based FETs would not deliver the required drive current.

Separately and following the first demonstration of GaAs MOSFETs using an ALD oxide [3], InGaAs MOSFETs were also demonstrated with increasing InAs composition in the channel [29, 30, 31]. As with HEMTs, the performance of these devices was seen to improve as more InAs was introduced in the channel [32]. Detailed interface characterization revealed a very low interface state density in Al_2O_3/InGaAs MOS structures in the vicinity of the conduction band edge where it matters for n-channel devices [33]. Excellent results have also been demonstrated with higher-permittivity dielectrics deposited by ALD on InAs-rich InGaAs [34].

A problematic aspect of high-K/InGaAs MOSFETs was found to be a significantly lower electron mobility than in

InGaAs HEMTs [35]. This has been attributed to interface roughness scattering and Coulomb scattering associated with interface states [36]. A solution to this has been found in a "buried-channel" design in which a thin wide-bandgap semiconductor (InP appears as the most promising choice) is placed between the channel and the oxide. This brings the oxide/semiconductor interface at some distance away from the channel and results in significantly reduced scattering and improved mobility [37]. To date, the buried quantum-well channel InGaAs MOSFET design has yielded the best results [38-40]. This design combines the best features of the HEMT (undoped quantum-well channel with specular interfaces, undoped access regions, and raised source and drain regions), with an ultra-thin high-K oxide for superior electrostatic control and scalability.

A critical aspect of a III-V MOSFET design for logic applications is self-aligned contacts. These are not commonly used in HEMTs though demonstrations exist [41]. Self-aligned contacts are essential to achieving the ultralow parasitic resistance that is required in future low-voltage MOSFETs as well as to be able to meet transistor footprint goals. A self-aligned device architecture based on dry-etched Mo contacts in a gate-last approach (Fig. 3) has been recently demonstrated by us [39]. A contact to gate spacing of 30 nm on 30 nm gate length devices has been achieved. Alternative self-aligned designs are being investigated based on silicide-like processes using Ni, Co or Pd [42,43].

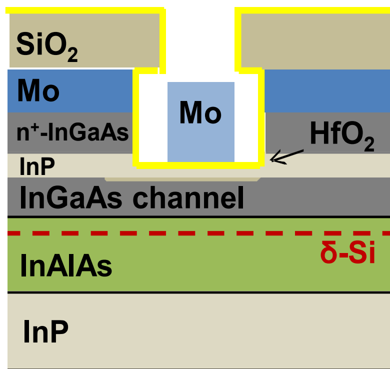

Figure 3. Sketch of self-aligned buried-channel MOSFET under investigation at MIT [39].

A self-aligned gate-last approach allows the MOS gate stack to be formed late in the process and hence helps preserve a high quality oxide-semiconductor interface. Coupled with aggressive barrier scaling, this yields outstanding short-channel effects and current drive [39]. The best measure of the balance between these two essential attributes is the ON current that is obtained at a certain voltage for a certain fixed I_{off} [26]. Fig. 4 shows this figure of merit as a function of gate length for recent InGaAs HEMTs and MOSFETs for an I_{off} of 100 nA/μm and V_{DD}=0.5 V. It is quite challenging for a device to enter this graph in the first place. First, the gate length must be below 150 nm. Then, the device has to turn off well so that a subthreshold current as low as 100 nA/μm can be reached. Only the devices that are depicted in this graph are known to this author to meet these criteria. Among all of them, the InGaAs HEMTs set the high-water mark for performance. MITs InGaAs MOSFETs are also among the very best planar MOSFETs ever demonstrated. They closely match the performance of InGaAs Trigate MOSFETs (more on these devices below).

A key element in obtaining high performance in the figure of merit selected in Fig. 4 is a small subthreshold swing, S. The subthreshold swing describes the sharpness of the turn off of the device current below threshold. Fig. 5 shows S as a function of gate length for recent InGaAs-channel MOSFETs and HEMTs. The HEMTs exhibit a nearly ideal behavior with a subthreshold swing approaching 60 mV/dec [25]. Among the MOSFETs, the self-aligned devices fabricated at MIT exhibit the lowest subthreshold swing and closely approach that of InGaAs TriGate MOSFETs [44].

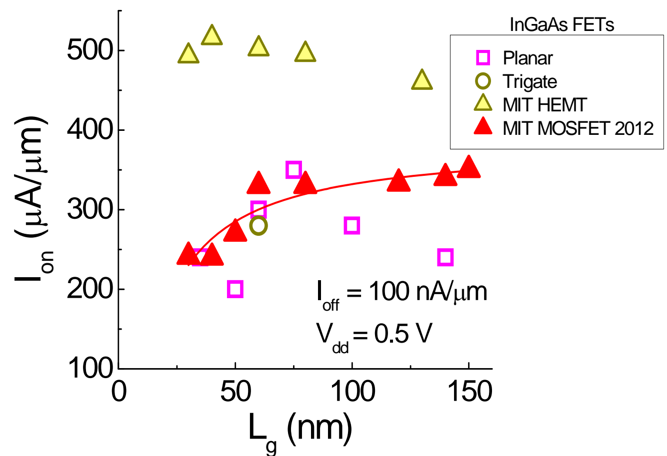

Figure 4. ON current vs. gate length for recent InGaAs MOSFETs and HEMTs. I_{off} is fixed at 100 nA/μm and V_{DD}=0.5 V.

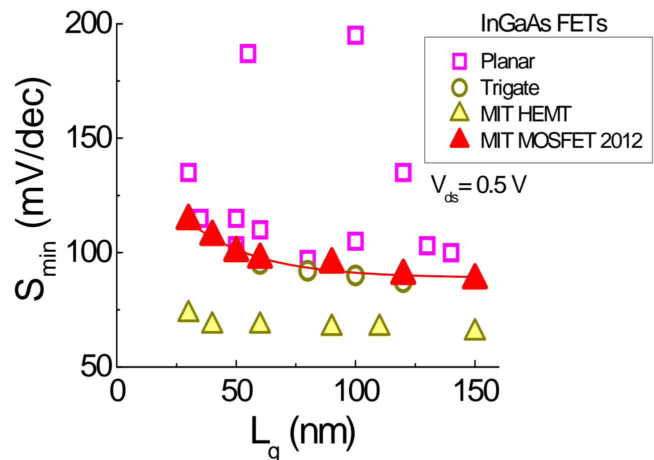

Figure 5. Subthreshold swing vs. gate length for recent InGaAs MOSFETs and HEMTs.

Underlying the excellent performance of our devices is an ultrathin gate oxide (2 nm of HfO_2 for the red triangle devices

in Figs. 4 and 5) and a high quality interface. We have proven this by demonstrating long-channel InGaAs buried-channel MOSFETs with a nearly ideal low-V_{DD} subthreshold swing of 69 mV/dec [39].

An alternative architecture for planar quantum-well MOSFETs is a selectively regrown source and drain design [45]. This is sketched in Fig. 6. In this approach, the channel is recessed to some depth using a real or a dummy gate as a mask and then heavily doped source and drain regions are grown around it. This device design has yielded to date the lowest access resistance of any FET design. An R_{ON} of 157 Ω.μm has been demonstrated on 30 nm InGaAs channel devices that all around have excellent characteristics [46]. An attractive aspect of this approach is the possibility of introducing tensile strain in the channel which could further boost performance [45].

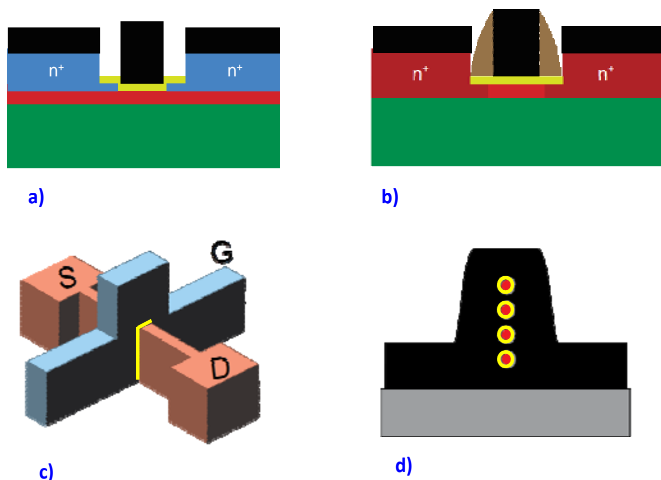

Figure 6. semi Possible future MOSFET architectures using a III–V compound conductor channel: A) recessed source-and-drain quantum-well MOSFET; b) regrown source-and-drain quantum-well MOSFET; c) Trigate MOSFET in which the channel charge is electrostatically controlled by a gate that wraps around three sides of a very thin channel; d) 'Gate-all-around' nanowire MOSFET, which has an array of very short and thin nanowires with the gate wrapped around them.

Scaling to very small dimensions will very likely require 3D device architectures such as Trigate FET or Gate-all-around Nanowire FETs. These alternative designs are depicted in Fig. 6. For the same channel length, increasing the number of gates that modulate the electron concentration in the channel provides improved charge control and short-channel effects. Trigate FETs with fins as narrow as 30 nm and excellent characteristics have been demonstrated [44,47]. Lateral and vertical Gate-All-Around Nanowire FETs have also been demonstrated with impressive characteristics [48-49].

The integration approach for InGaAs MOSFETs, in particular the 3D device designs, is uncertain. A significant complication is the need to use Si as substrate material. This is dictated for economic reasons. A second problem is the fact that a high performance p-channel device, as required in CMOS, is unlikely to be possible using InGaAs in the channel. This is due to its relatively small hole mobility [2]. The most likely channel material candidates for a p-channel MOSFET in a future post-Si CMOS technology are Ge and InGaSb. They both have different relaxed lattice constants than InAs-rich InGaAs which makes their integration on Si indeed a very difficult technological problem. Several integration schemes have been demonstrated such as direct wafer bonding [50], epitaxial layer transfer to an SOI substrate [51]. Aspect Ratio Trapping [52] also exhibits considerable promise but n- and p-channel device integration is still to be demonstrated.

IV. Conclusions

The recent interest on InGaAs MOSFET technologies for future CMOS applications represents a several order of magnitude increase in the effort dedicated to InGaAs FETs of any kind for any application. This burst of activity has opened new lines of research and development such as MOS gate stacks, self-aligned designs, low resistance compact contacts, dry recess and the use of Si-compatible metals and integration with p-channel devices on Si. The hope is that all this will culminate in a new CMOS technology that will extend Moore's law for a few more generations. At the least, the new effort should pay handsomely in enabling future highly-integrated and power efficient THz systems integrated on Si substrates.

Acknowledgements

The authors is grateful to present and former students, postdocs and collaborators in this research: Dimitri Antoniadis, Donghyun Jin, Dae-Hyun Kim, Taewoo Kim, Jianqiang Lin, Niamh Waldron, and Ling Xia. Over the years, this research has been funded by FCRP MSD Center, Intel Corporation, US Army Research Lab. and SRC. The MIT devices are fabricated at the Microsystems Technology Laboratories, Scanning Electron Beam Laboratory and NanoStructures Laboratory at MIT.

References

[1] S. Adachi, "Physical Properties of III-V Semiconductor Compounds." Wiley 1992.

[2] J. A. del Alamo, Nature 479, 317 (2011)

[3] P. D. Ye et al., IEEE Electron Dev. Lett. 24, 209 (2003).

[4] T. Mimura et al., Japn. J. Appl. Phys. 20, L598 (1981).

[5] C. Y. Chen et al., IEEE Electron Dev. Lett.3, 152 (1982).

[6] A. Ketterson et al., IEEE Electron Dev. Lett. 6, 628 (1985).

[7] J. A. del Alamo, CS MANTECH 2011, paper 2.1.

[8] T. Henderson et al., CS MANTECH 2007, p. 247.

[9] H. Morkner et al., IEEE RFIC Symp. 2007, p. 365.

[10] D.-H. Kim et al., IEDM 2010, p. 692.

[11] E.-Y. Chang et al., Appl. Phys. Express 6, 034001 (2013).

[12] W. Snodgrass et al., Int. Electron Dev. Meet. 2006.

[13] D.-H. Kim et al., Int. Electron Dev. Meet. 2011, p. 319.

[14] K. Leong et al., InP and Rel. Mat. Conference 2012.

[15] M. W. Pospieszalski et al., IEEE MTT-S Digest 2000, p. 25.

[16] J. A. del Alamo, Int. Conf. on Solid St. Dev. and Mat. 2012.

[17] D.-H. Kim et al. IEEE Electron Def. Lett. 34, 196 (2013).
[18] D.-H. Kim et al., Appl. Phys. Lett. 101, 223507 (2012).
[19] H. Becke, et al., Solid State Electron. 8, 813 (1965).
[20] F. Ren, et al., Solid State Electron. 41, 1751 (1997).
[21] D.-H. Kim et al., Int. Electron Dev. Meet. 2005.
[22] S. Datta et al., Int. Electron Dev. Meet. 2005.
[23] D.-H. Kim et al., Int. Electron Dev. Meet. 2006.
[24] D.-H. Kim et al., Int. Electron Dev. Meet. 2007.
[25] D.-H. Kim et al., Int. Electron Dev. Meet. 2008, p. 719.
[26] J. A. del Alamo et al., InP and Rel. Mat. Conf. 2011.
[27] D.-H. Kim et al., Int. Electron Dev. Meet. 2009, p. 861.
[28] D. Jin et al., Int. Electron Dev. Meet. 2009, p. 495.
[29] P. D. Ye et al., Appl. Phys. Lett. 84, 434 (2004).
[30] Y. Xuan et al., Int. Electron Dev. Meet. 2007, p. 637.
[31] N. Li et al., Appl. Phys. Lett. 92, 143507 (2008).
[32] P. D. Ye et al., ECS Trans. 19, 605 (2009).
[33] G. Brammertz et al., Appl. Phys. Lett. 95, 202109 (2009).
[34] J. Huang et al., Int. Electron Dev. Meet. 2009, p. 335.
[35] J. Lin et al., Int. Electron Dev. Meet. 2008.
[36] A. Sonnet et al., Microelectron. Eng. 88, 1083 (2011).
[37] S. Oktyabrsky et al., ECS Trans. 35, 385 (2011).
[38] M. Radosavljevic et al., Int. Electron Dev. Meet 2009, p. 319.
[39] J. Lin et al., Int. Electron Dev. Meet. 2012, p. 757.
[40] D.-H. Kim et al., Int. Electron Dev. Meet. 2012, p. 761.
[41] N. Waldron et al., IEEE Trans. Electron Dev. 57, 297 (2010).
[42] S.-H. Kim et al., Appl. Phys. Express 4, 024201 (2011).
[43] Ivana et al., Solid St. Electron. 78, 62 (2012).
[44] M. Radosavljevic et al., Int. Electron Dev. Meet. 2011, p. 765.
[45] H.-C. Chin et al., IEEE Electron Device Lett. 30, 805 (2009).
[46] X. Zhou et al., Int. Electron Dev. Meet. 2012, p. 773.
[47] M. Radosavljevic et al., Int. Electron Dev. Meet. 2010, p. 126.
[48] J. J. Gu et al., Int. Electron Dev. Meet. 2012, p. 633.
[49] K.-M. Persson et al., IEEE Electron Dev. Lett. 31, 428 (2010).
[50] M. Yokoyama et al., VLSI Tech. Symp. 2011, p. 60.
[51] J. Nah et al., NanoLett. 12, 3592 (2012).
[52] J. Fiorenza et al., ECS Trans. 33, 963 (2010).