

InGaAs Nanoelectronics: from THz to CMOS

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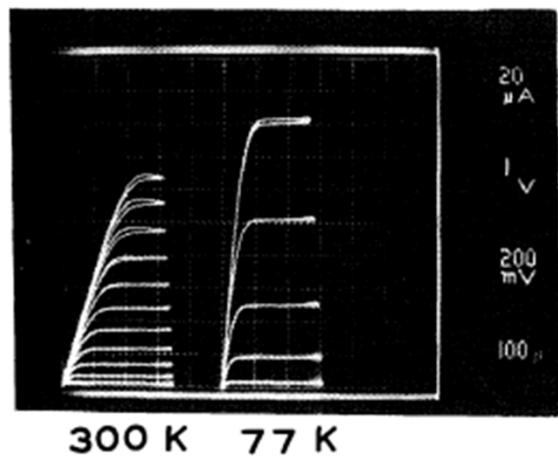


Outline

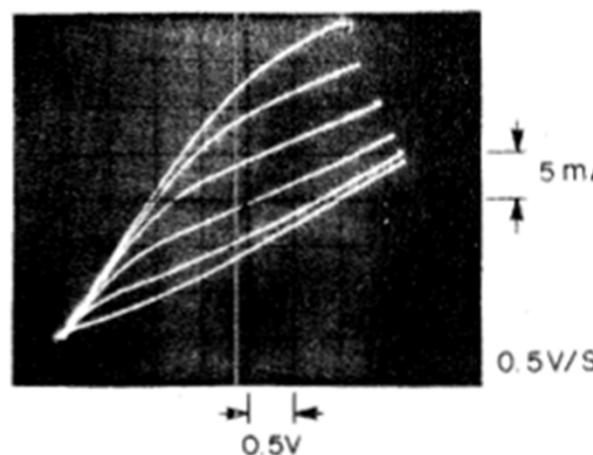
1. InGaAs HEMT today
2. InGaAs HEMTs towards THz operation
3. InGaAs MOSFETs: towards sub-10 nm CMOS

A bit of perspective...

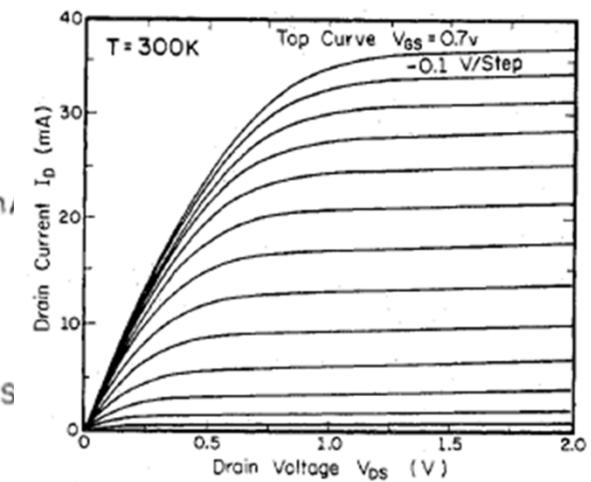
- Invention of **AlGaAs/GaAs HEMT**: Fujitsu Labs. 1980
- First **InAlAs/InGaAs HEMT on InP**: Bell Labs. 1982
- First **AlGaAs/InGaAs Pseudomorphic HEMT**: U. Illinois 1985
- Main attraction of InGaAs: RT $\mu_e = 6,000\sim30,000 \text{ cm}^2/\text{V.s}$



Mimura JJAPL 1980



Chen EDL 1982



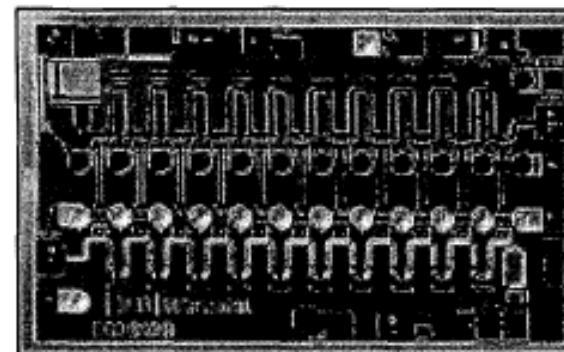
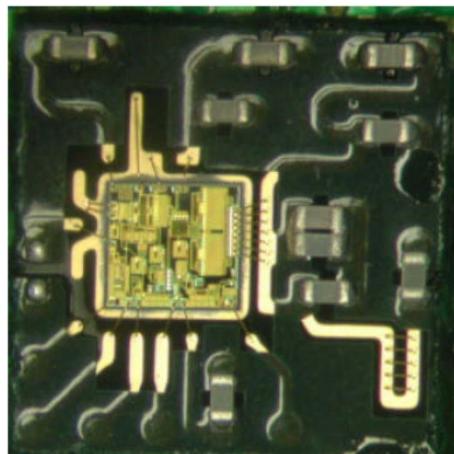
Ketterson EDL 1985

InGaAs Electronics Today

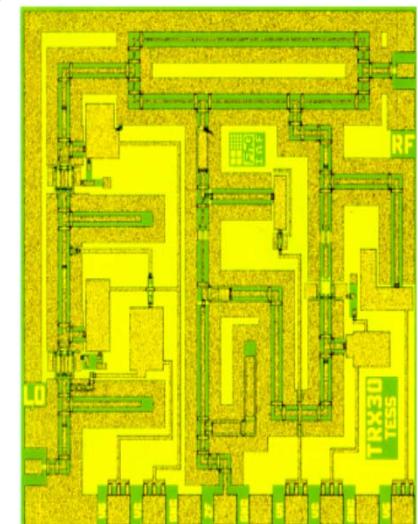


TriQuint and Skyworks Power iPhone 5

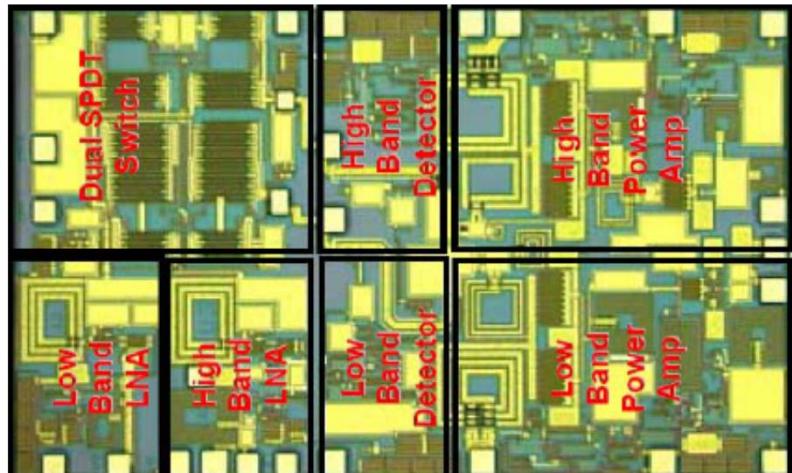
UMTS-LTE PA module
Chow, MTT-S 2008



40 Gb/s modulator driver
Carroll, MTT-S 2002

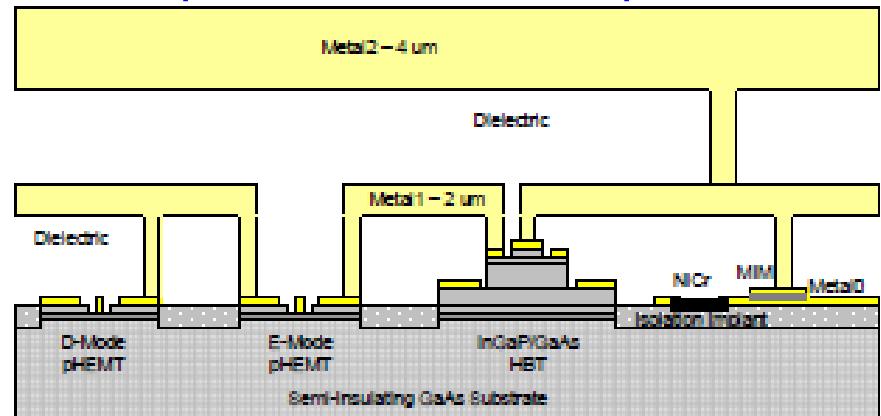


77 GHz transceiver
Tessmann, GaAs IC
1999



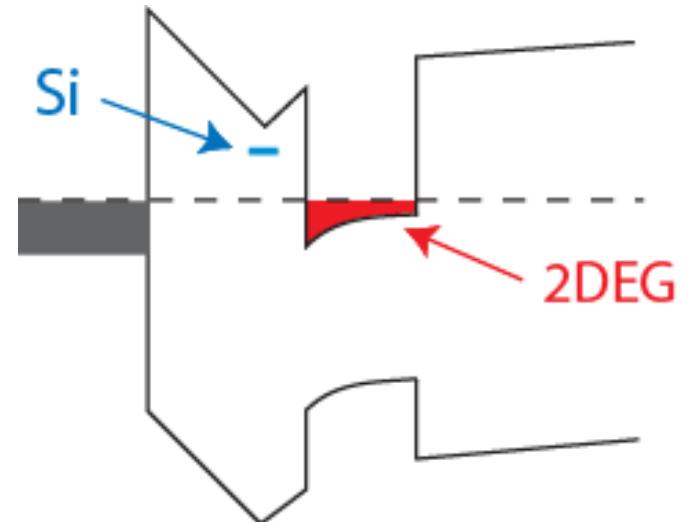
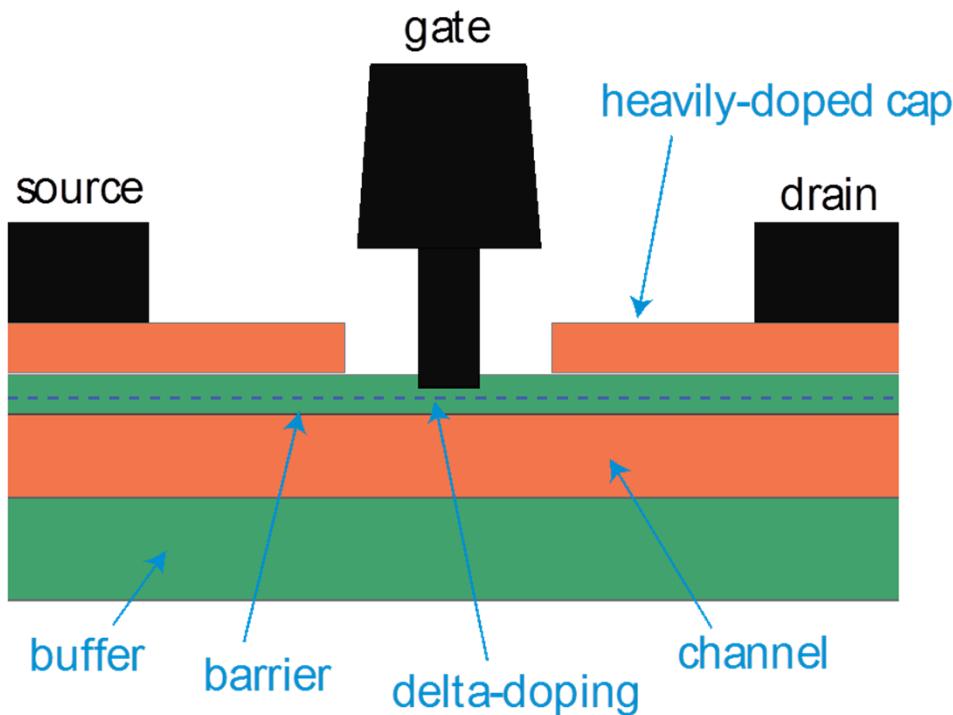
Single-chip WLAN MMIC, Morkner, RFIC 2007

Bipolar/E-D PHEMT process



Henderson, Mantech 2007

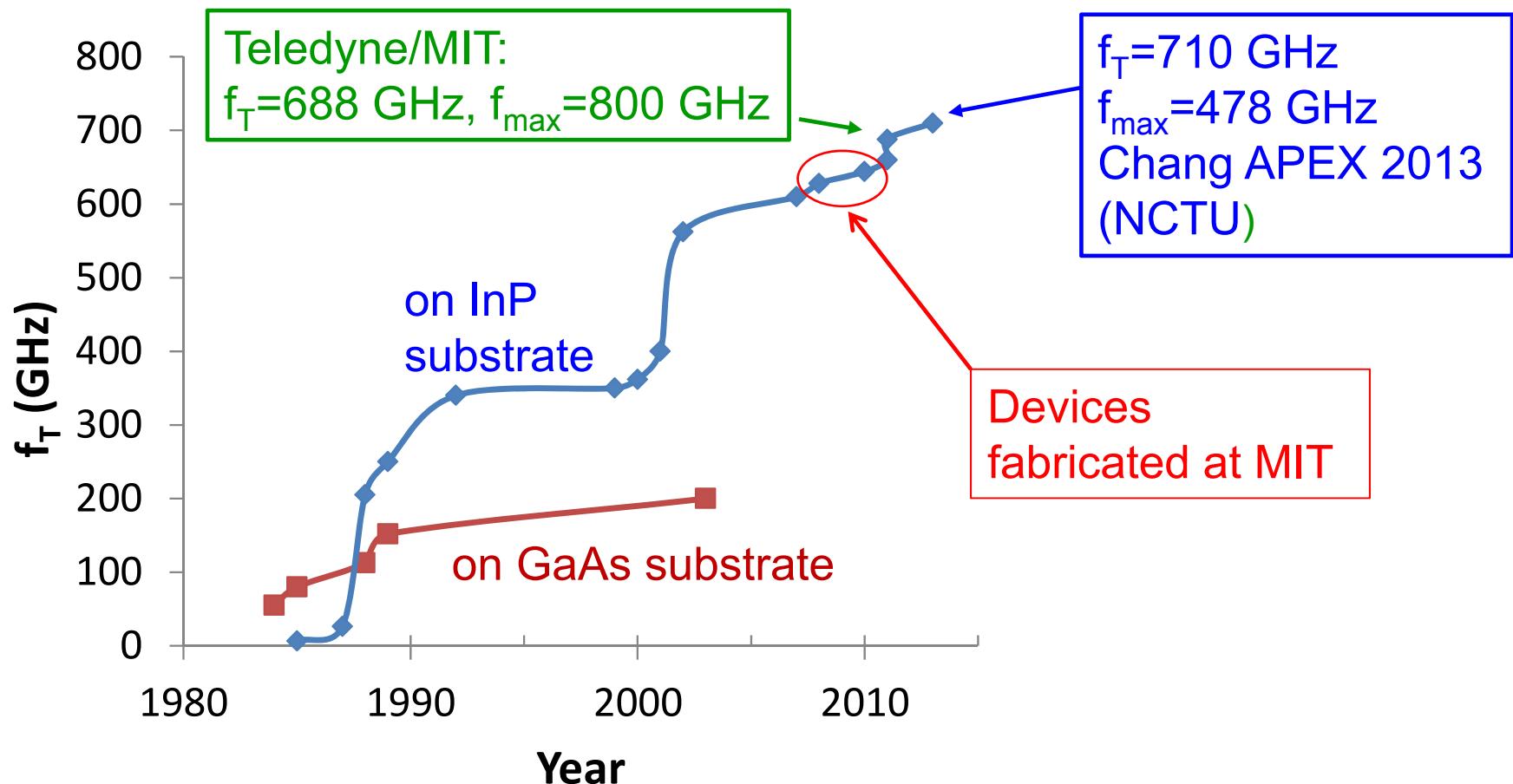
InGaAs High Electron Mobility Transistor (HEMT)



Modulation doping:

→ 2-Dimensional Electron Gas at InAlAs/InGaAs interface

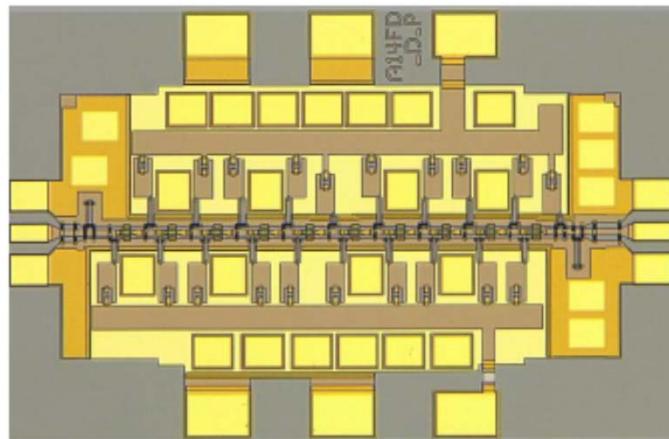
InGaAs HEMT: high-frequency record vs. time



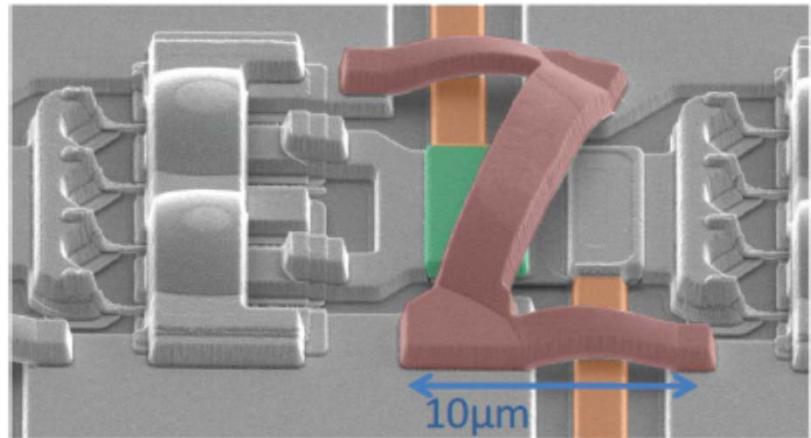
- Highest f_T of any FET on any material system
- Best balanced f_T and f_{max} of any transistor on any material

InGaAs HEMTs: circuit demonstrations

10-stage 670 GHz LNA

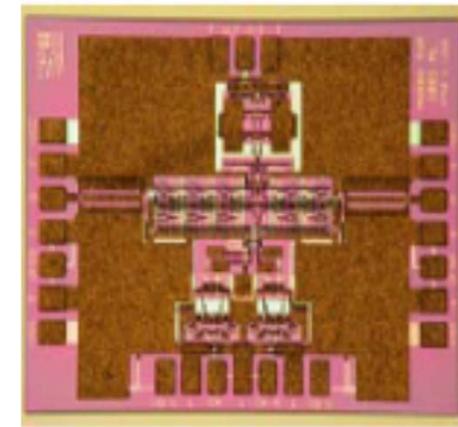


Leong, IPRM 2012



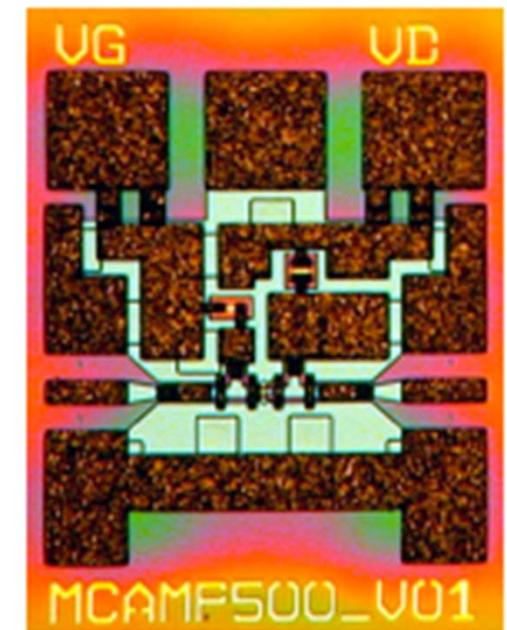
Sarkozy, IPRM 2013

80 Gb/s multiplexer IC



Wurfl, GAAS 2004

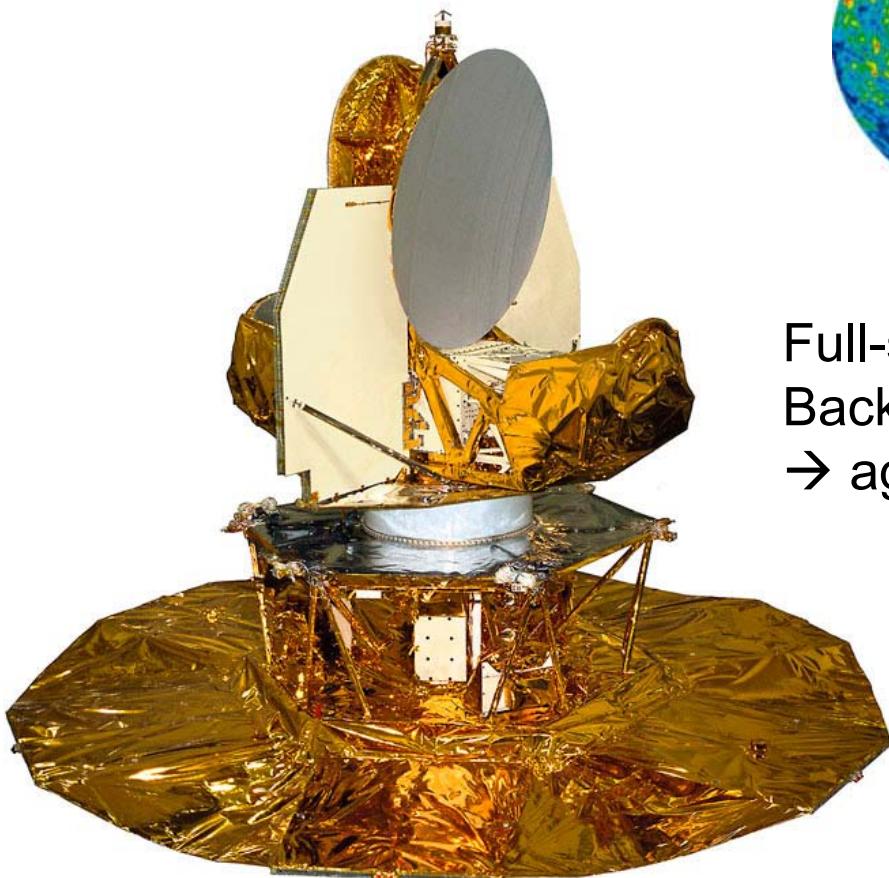
Single-stage
500 GHz LNA



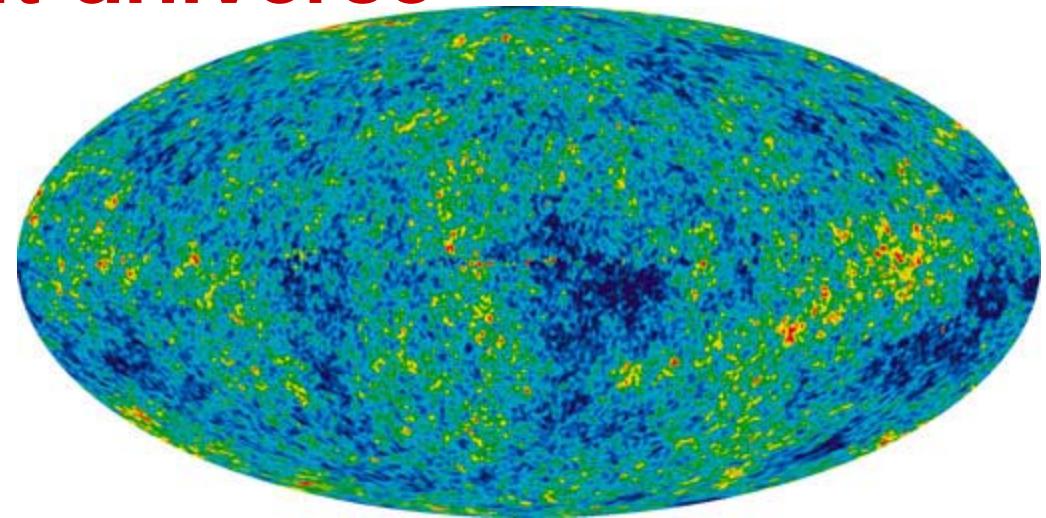
Tessmann, CSIC 2010

InGaAs HEMTs on InP used to map infant universe

WMAP = *Wilkinson Microwave
Anisotropy Probe*
Launched 2001

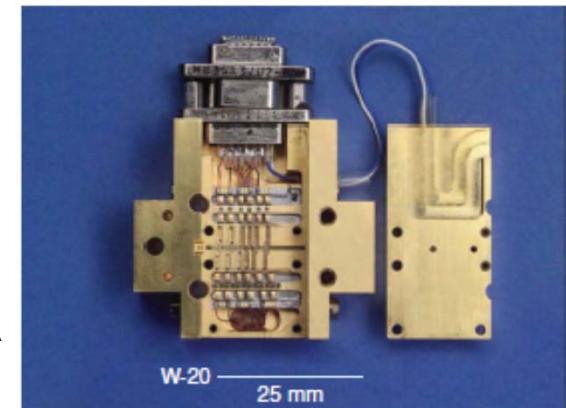


<http://map.gsfc.nasa.gov/>

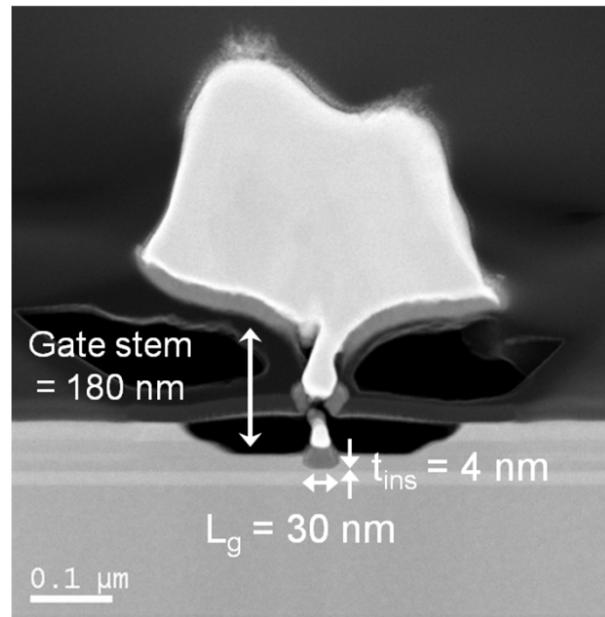
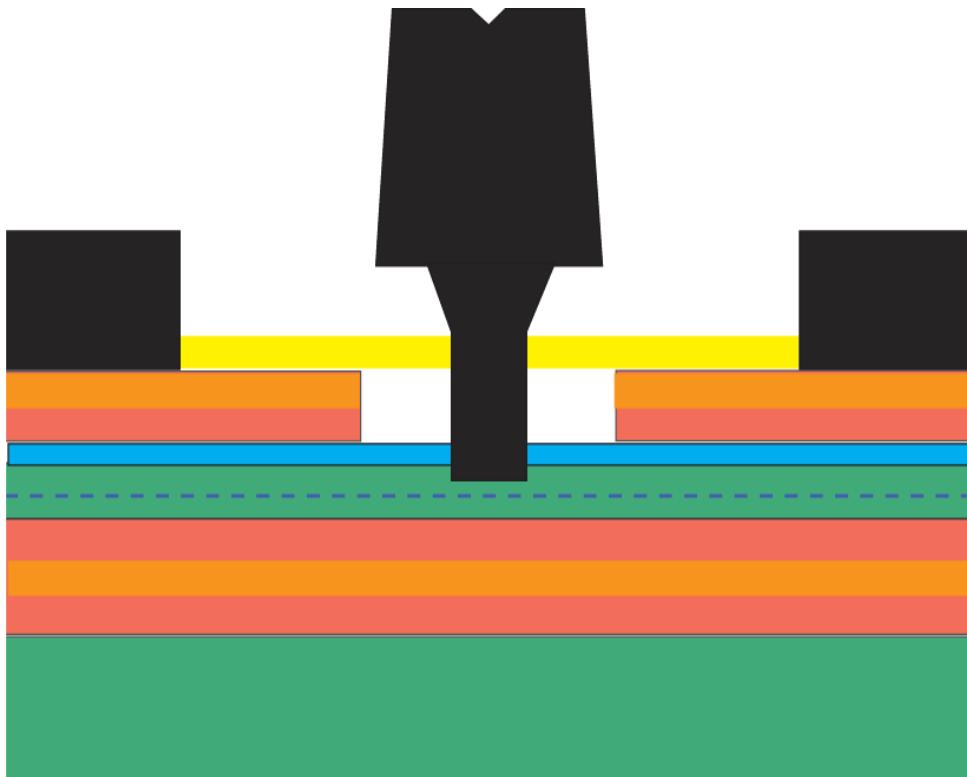


Full-sky map of Cosmic Microwave
Background radiation (oldest light in Universe)
→ age of Universe: 13.73B years ($\pm 1\%$)

0.1 μ m InGaAs HEMT LNA
Pospieszalski MTT-S 2000

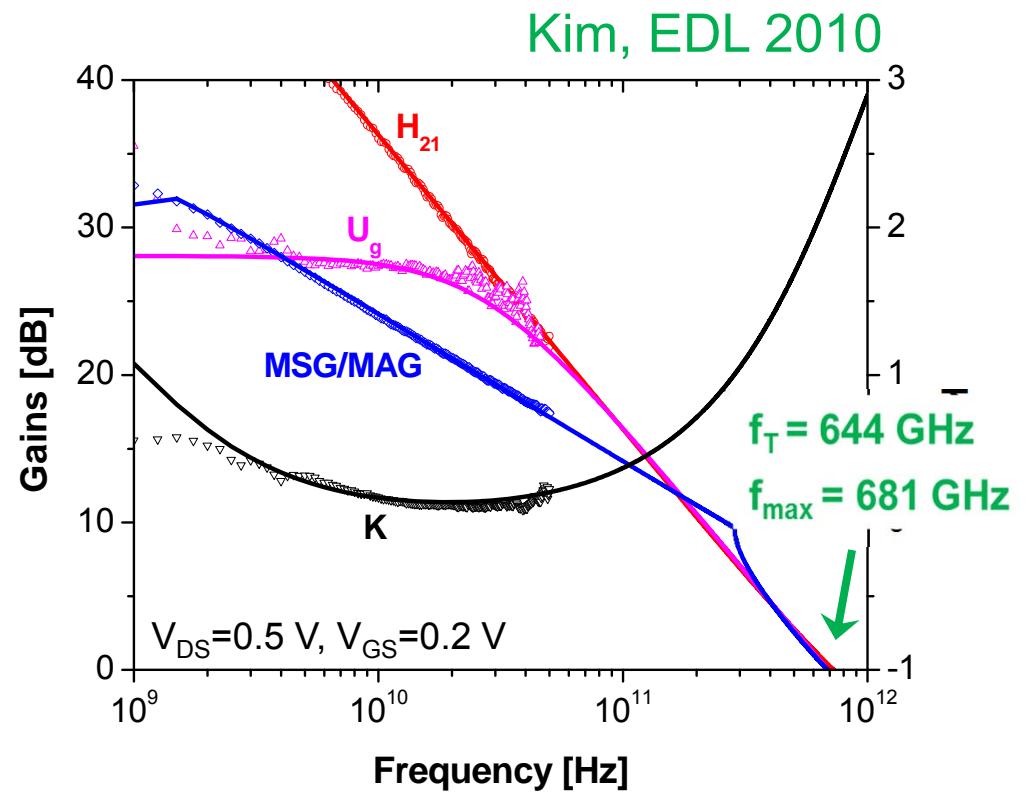
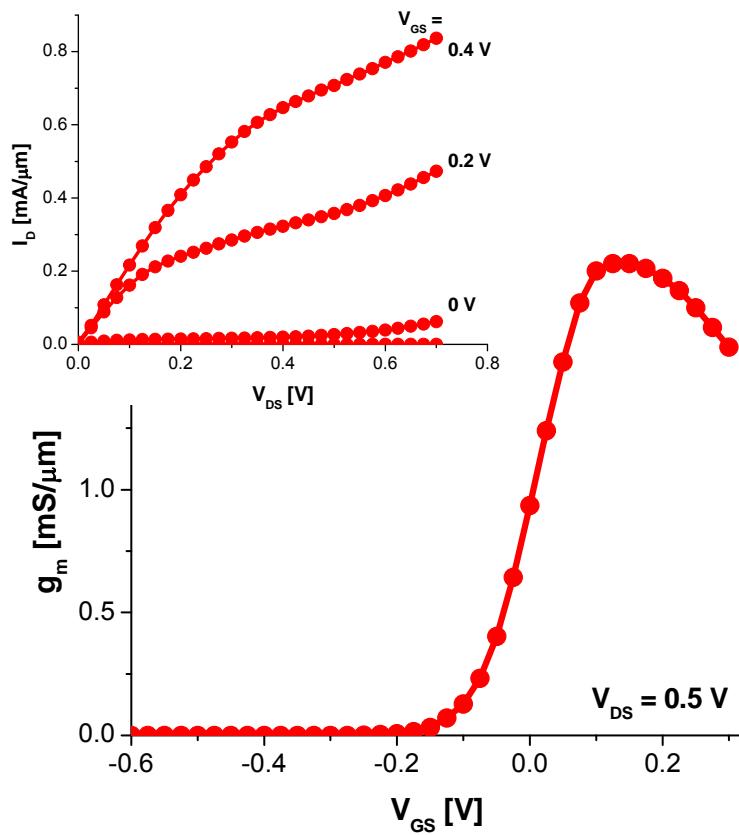


A closer look: InGaAs HEMTs at MIT



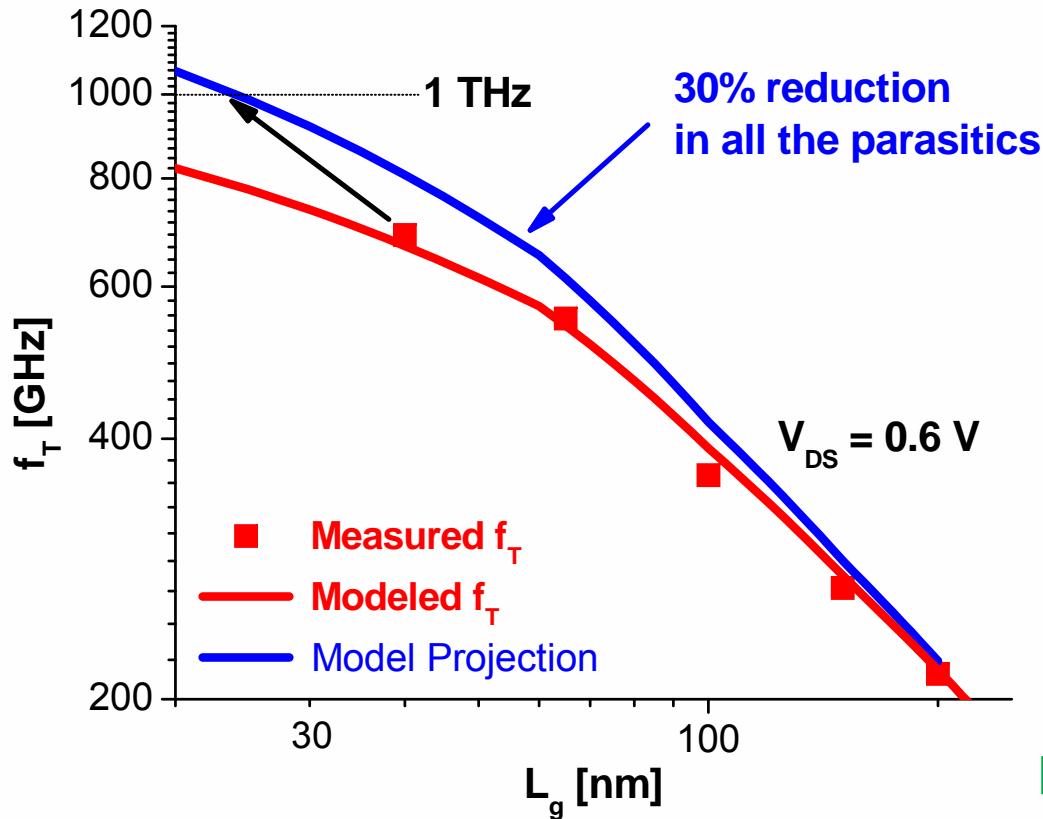
- QW channel ($t_{ch} = 10 \text{ nm}$):
 - InAs core
 - InGaAs cladding
- $\mu_e = 13,200 \text{ cm}^2/\text{V}\cdot\text{sec}$
- InAlAs barrier ($t_{ins} = 4 \text{ nm}$)
- $L_g = 30 \text{ nm}$

$L_g = 30 \text{ nm InGaAs HEMT}$



- High transconductance: $g_m = 1.9 \text{ mS}/\mu\text{m}$ at $V_{DD} = 0.5 \text{ V}$
- First transistor of any kind with both f_T and $f_{max} > 640 \text{ GHz}$

How to reach $f_T = 1$ THz?

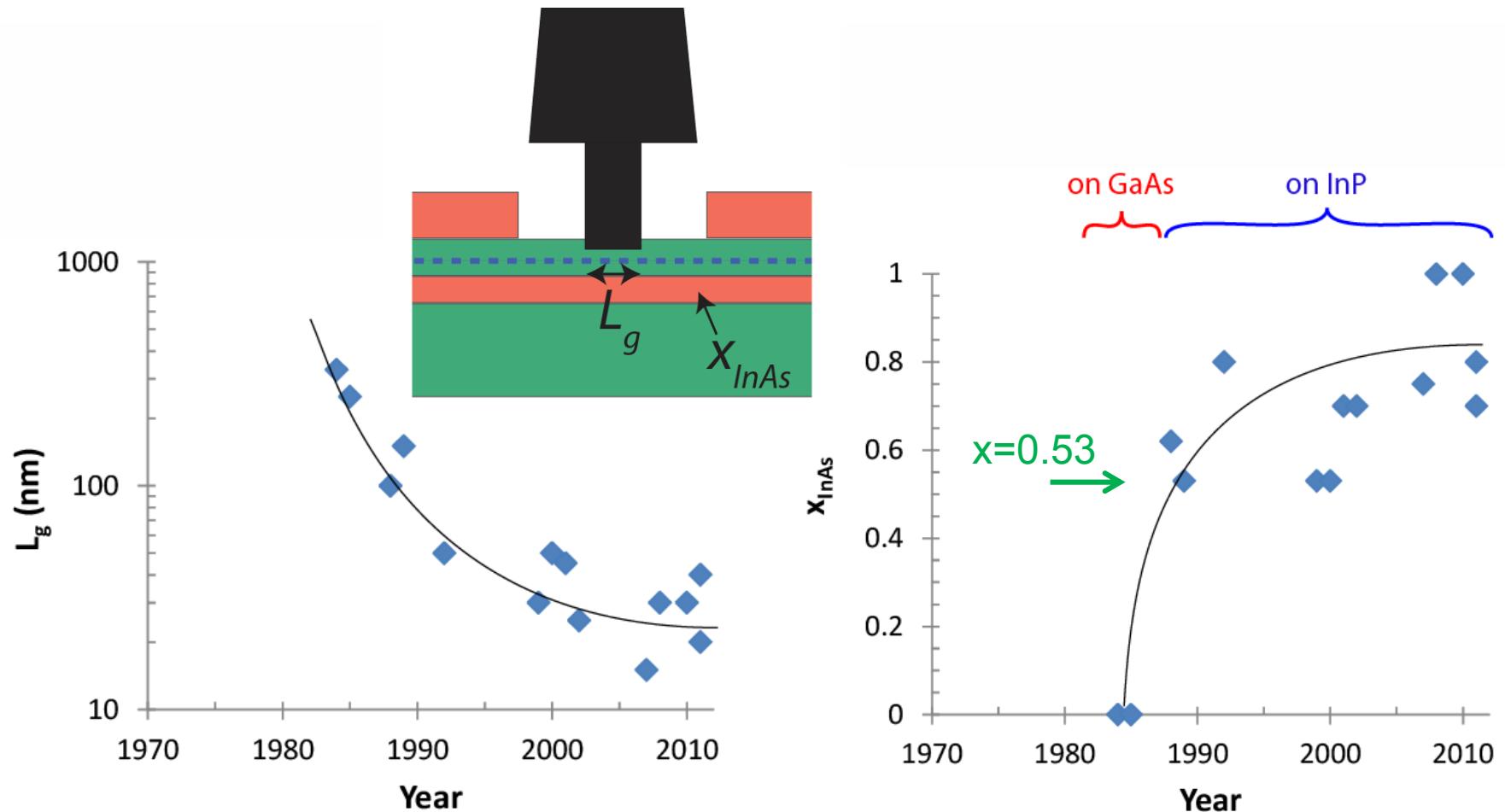


Kim, IEDM 2011

$f_T = 1$ THz feasible by:

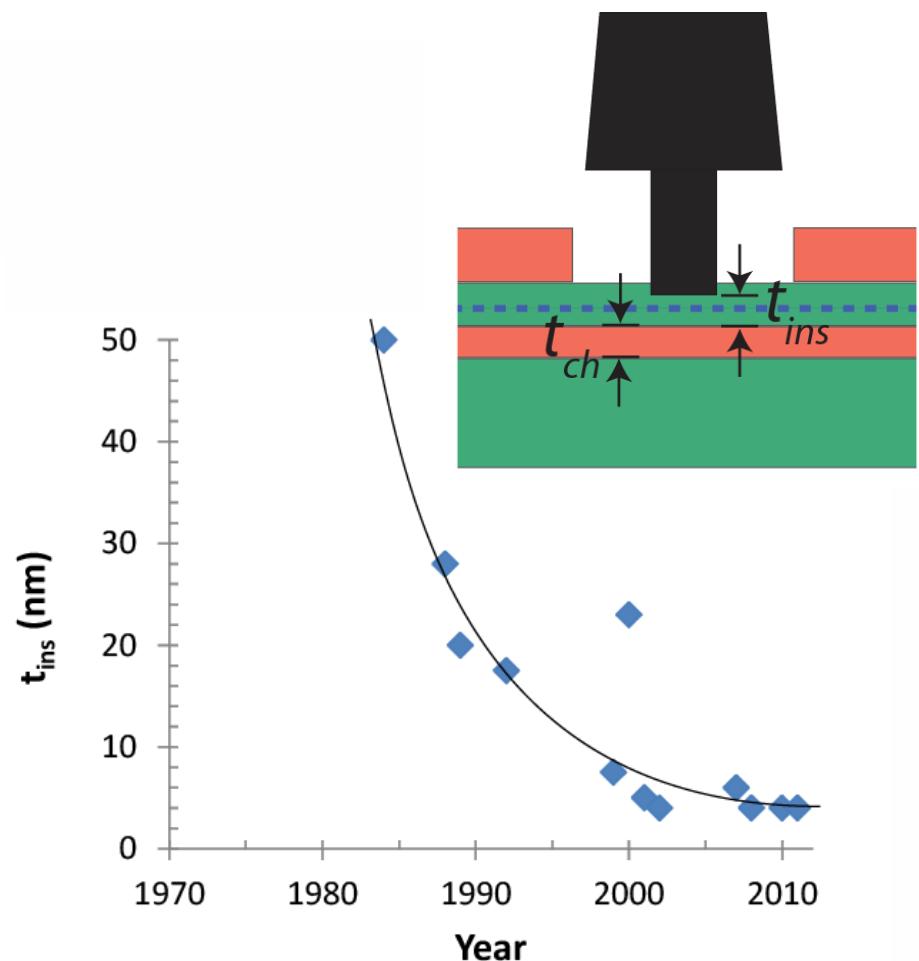
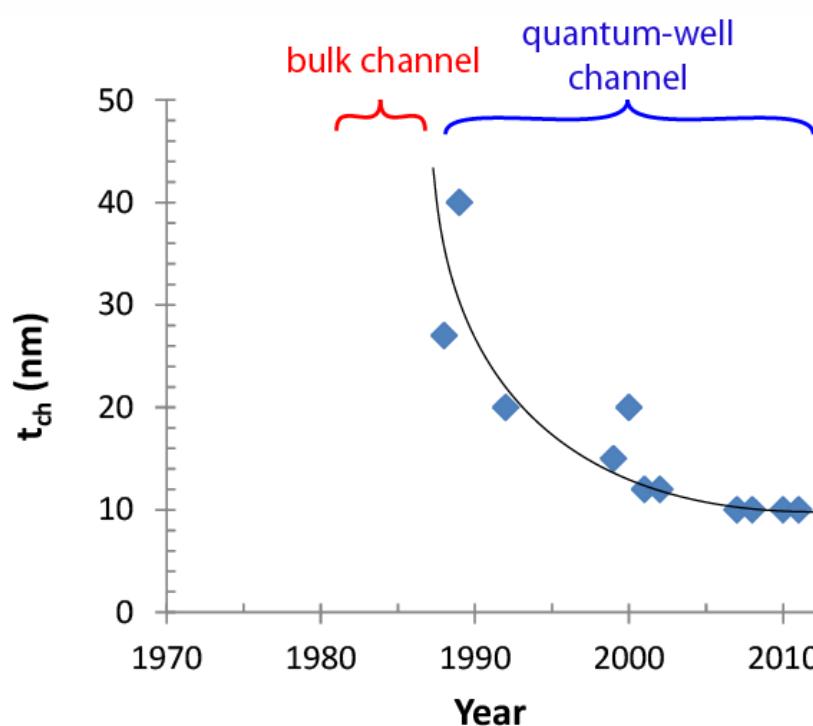
- scaling to $L_g \approx 25$ nm
- ~30% parasitic reduction

Record f_T InGaAs HEMTs: megatrends



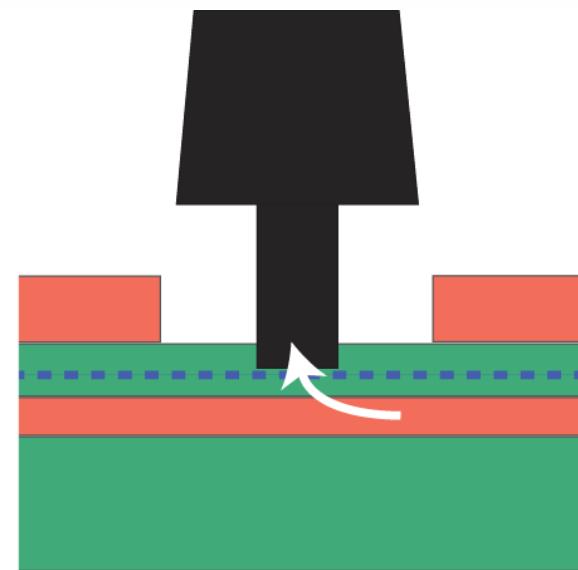
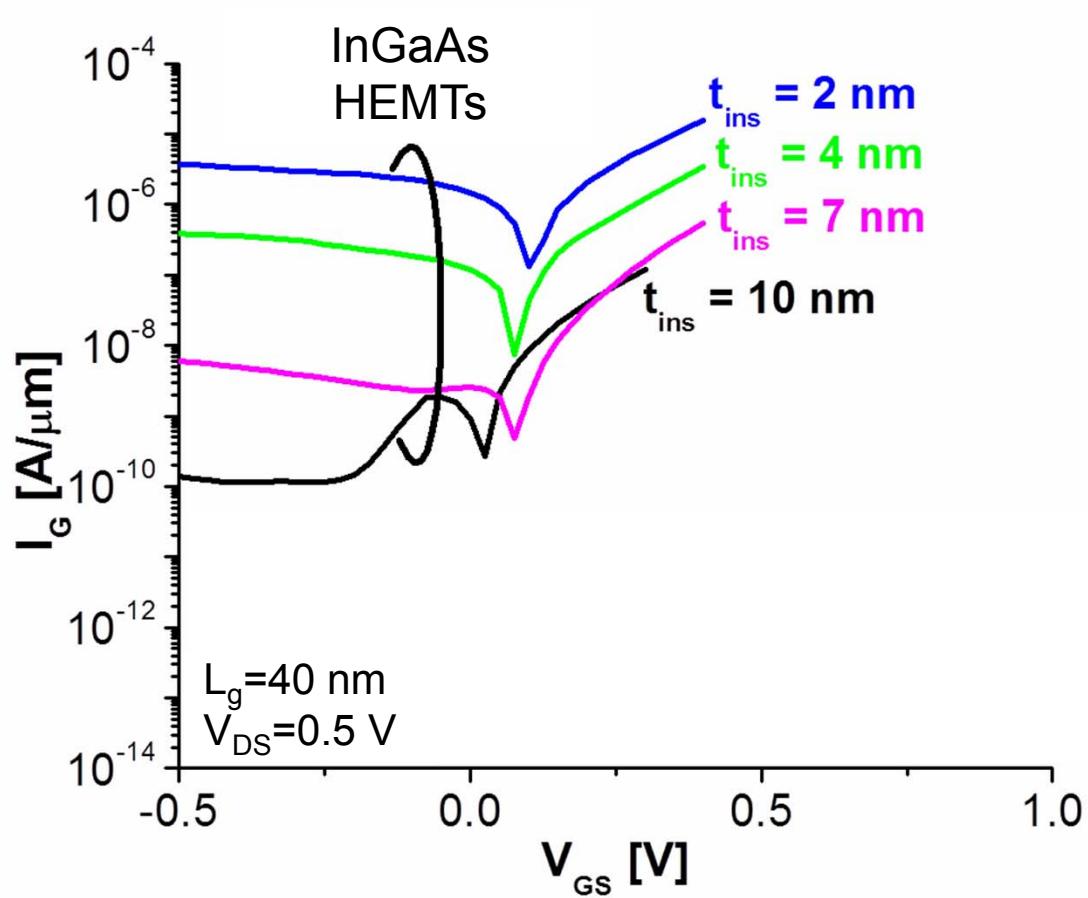
- Over time: $L_g \downarrow$, $In_xGa_{1-x}As$ channel $x_{InAs} \uparrow$
- L_g , x_{InAs} saturated \rightarrow no more progress possible?

Record f_T InGaAs HEMTs: megatrends



- Over time: $t_{ch} \downarrow$, $t_{ins} \downarrow$
- t_{ch} , t_{ins} saturated \rightarrow no more progress possible?

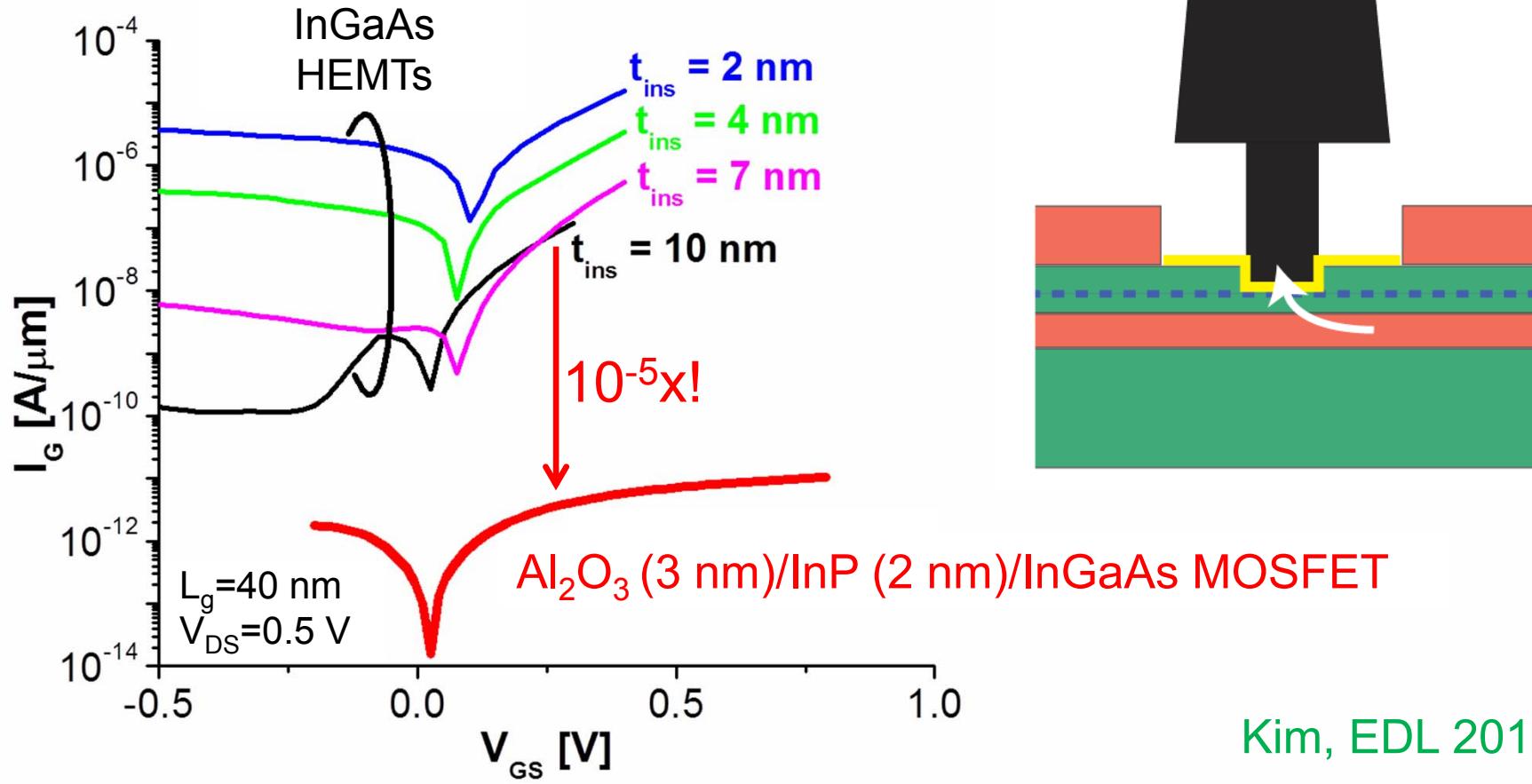
Limit to HEMT barrier scaling: gate leakage current



Kim, EDL 2013

At $L_g=30-40 \text{ nm}$, modern HEMTs are at the limit of scaling!

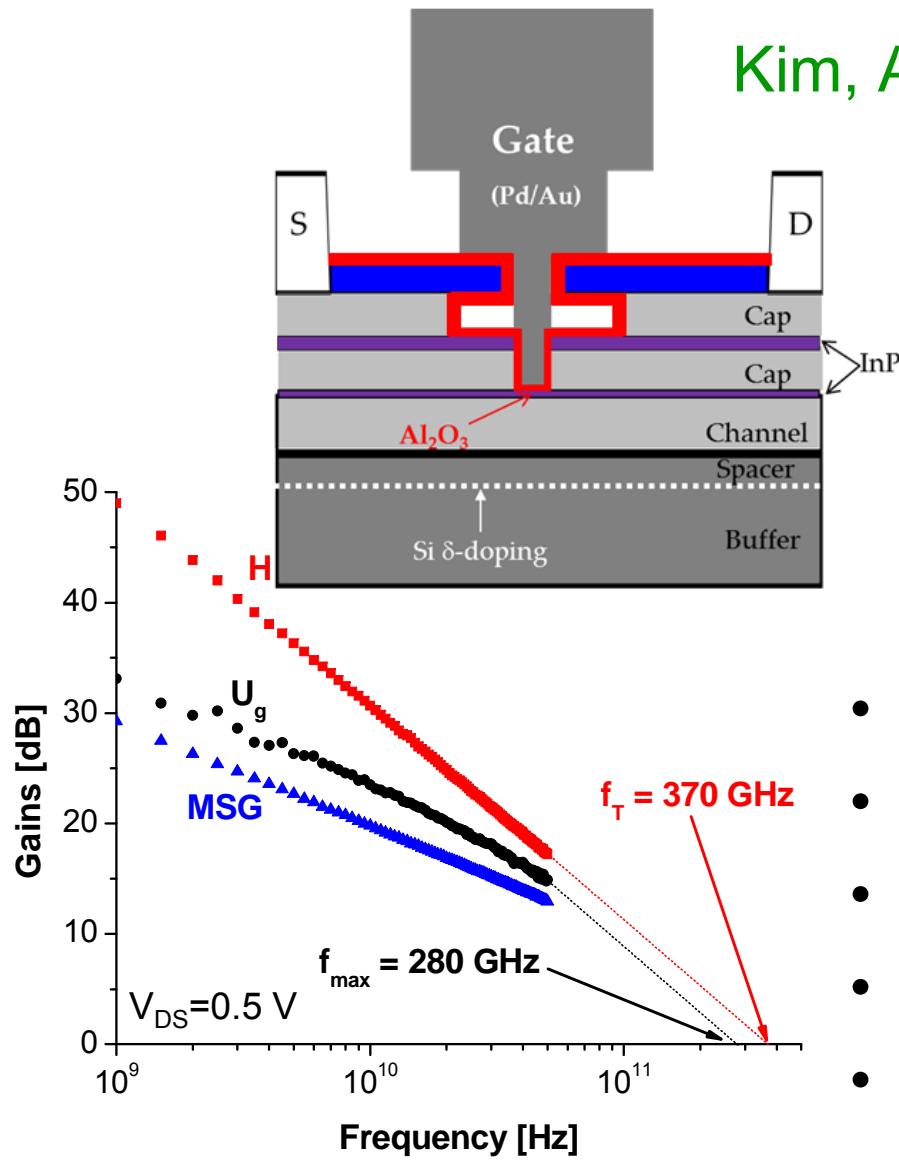
Solution: MOS gate!



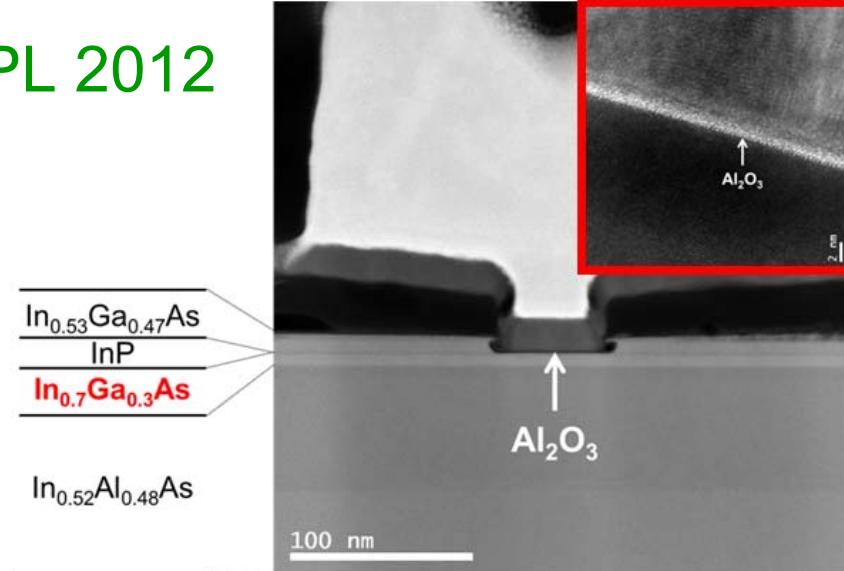
Kim, EDL 2013

Need high-K gate dielectric: HEMT \rightarrow MOSFET!

InGaAs MOSFETs with $f_T = 370$ GHz (Teledyne/MIT/IntelliEpi/Sematech)



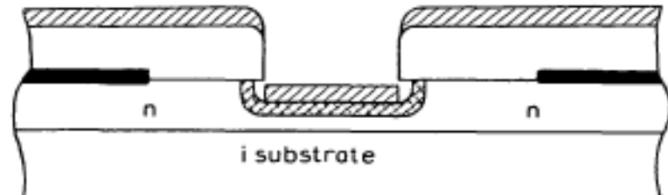
Kim, APL 2012



- Channel: 10 nm In_{0.7}Ga_{0.3}As
- Barrier: 1 nm InP + 2 nm Al₂O₃
- $L_g = 60$ nm
- $g_m = 2$ mS/ μ m
- $R_{ON} = 220 \Omega \cdot \mu$ m

III-V MOSFET: a >30 year pursuit!

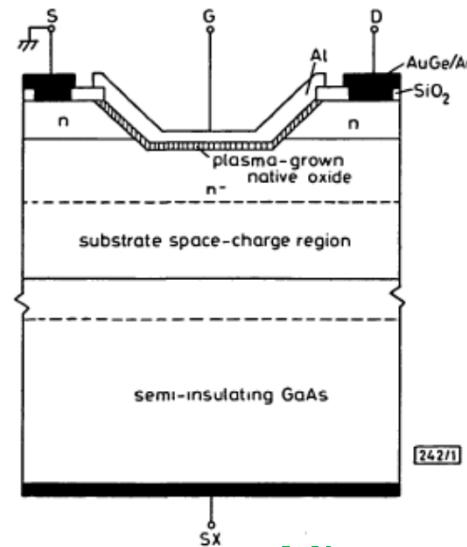
GaAs



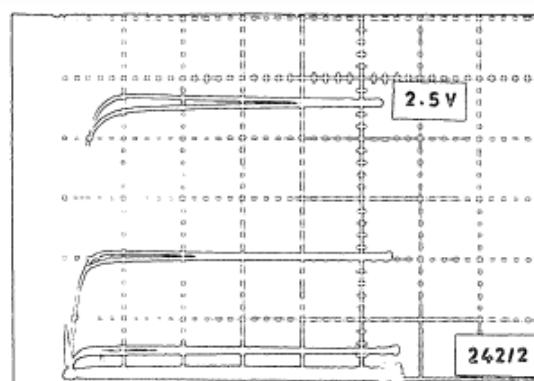
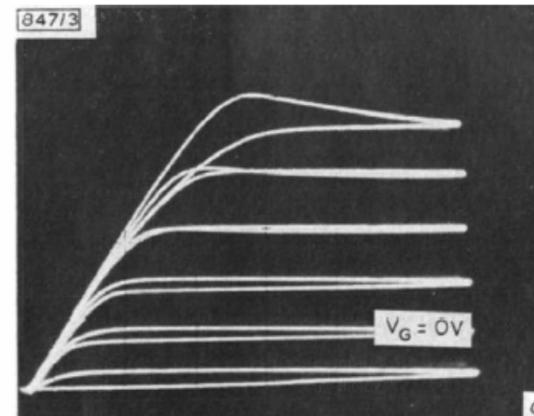
- gate metal
- photoresist
- anodic oxide
- ohmic contact

Kohn, EL 1977

GaAs



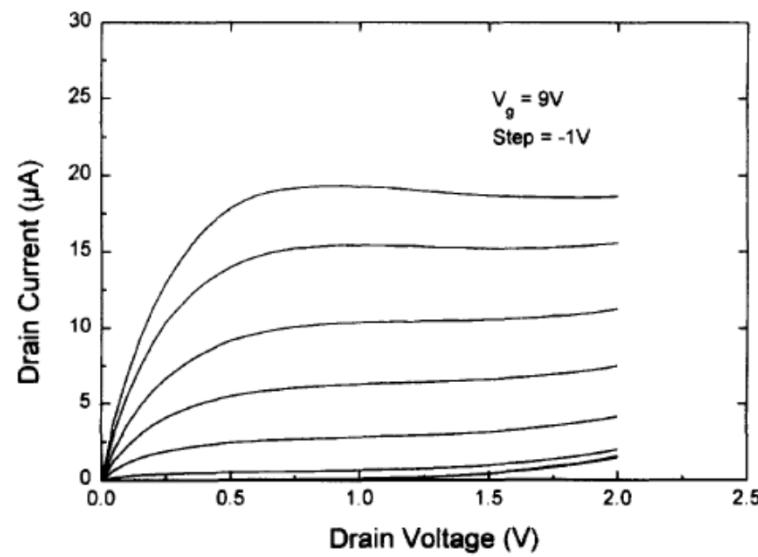
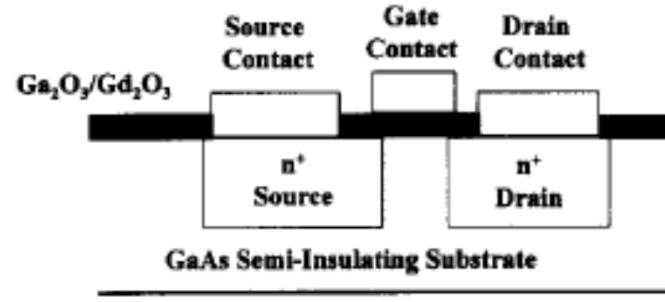
Mimura, EL 1978



Poor electrical characteristics due to oxide/semiconductor interface defects → *Fermi level pinning*

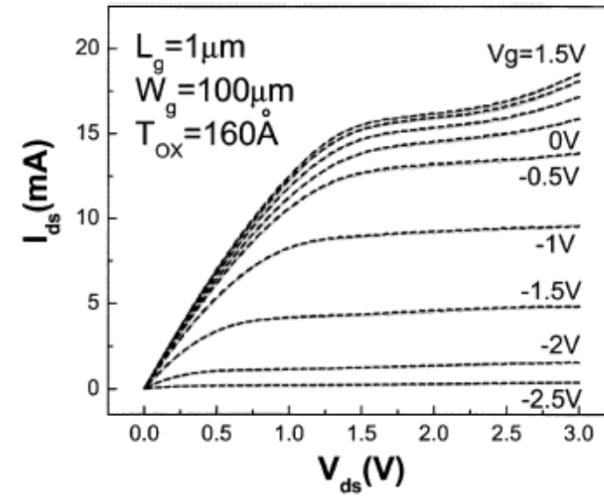
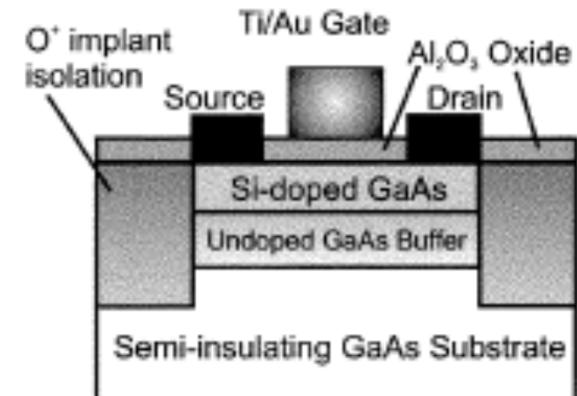
Recent breakthrough: oxide/III-V interfaces with unpinned Fermi level

In-situ UHV Ga_2O_3 - Gd_2O_3 on GaAs



Ren, SSE 1997

Ex-situ ALD Al_2O_3 on GaAs

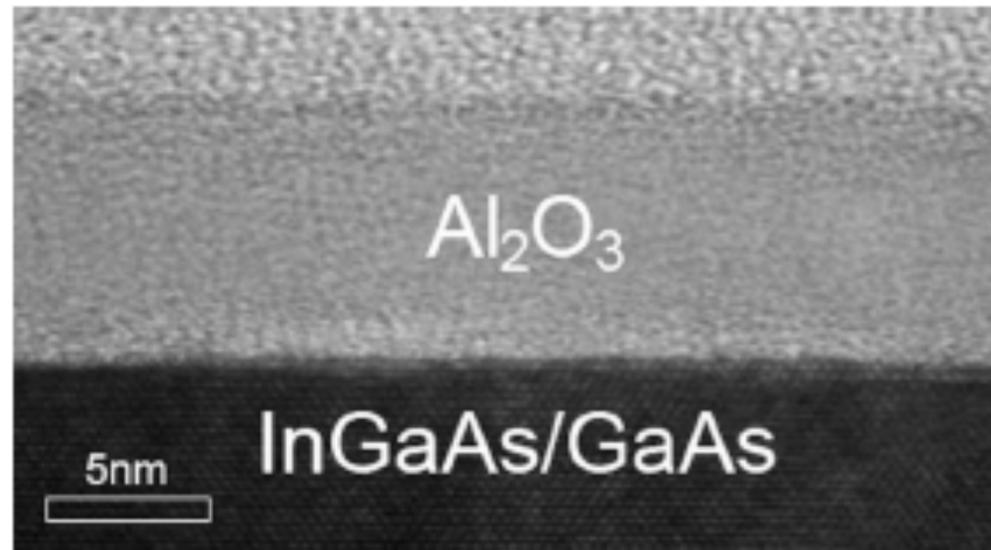


Ye, EDL 2003

“Self-cleaning” during ALD

ALD eliminates surface oxides that pin Fermi level:

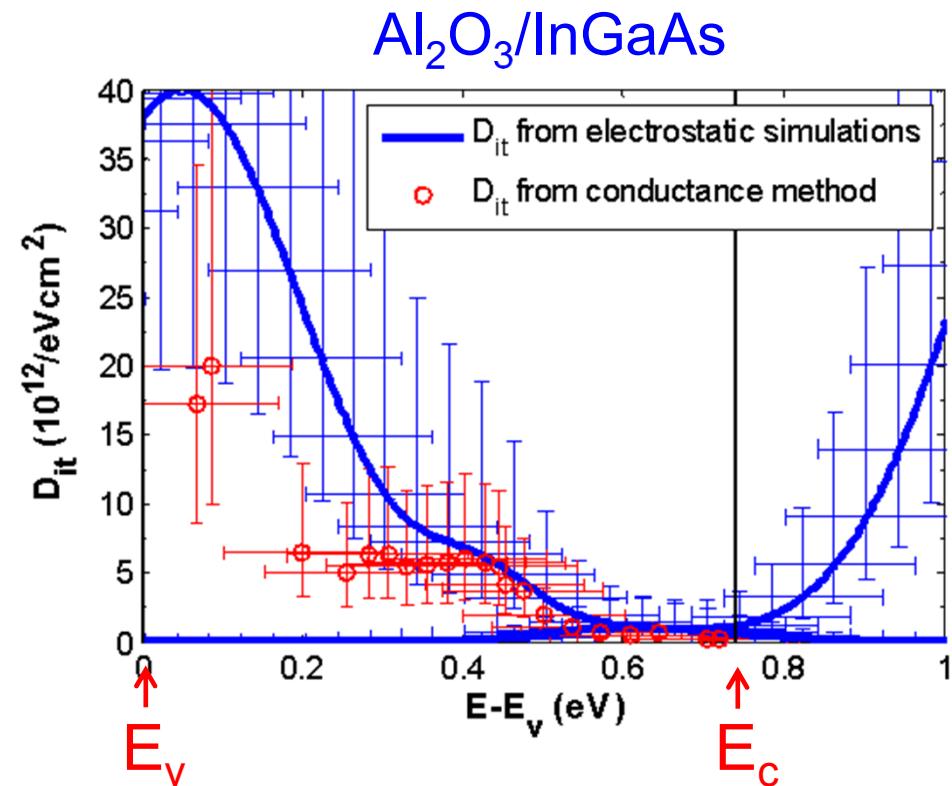
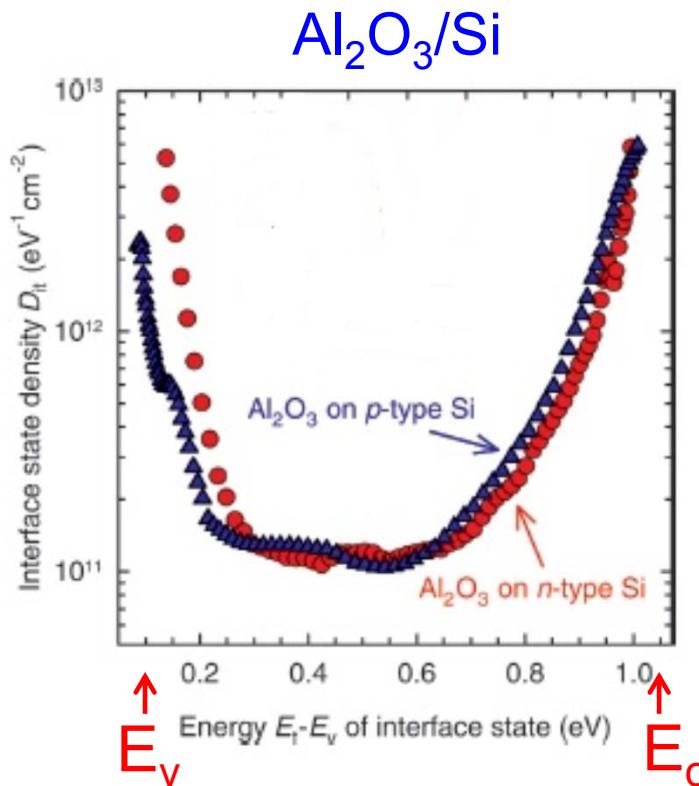
- First observed with Al_2O_3 , then with other high-K dielectrics
- First seen in GaAs, then in other III-Vs



← Clean, smooth
interface
without surface
oxides

Huang, APL 2005

Interface quality: $\text{Al}_2\text{O}_3/\text{InGaAs}$ vs. $\text{Al}_2\text{O}_3/\text{Si}$



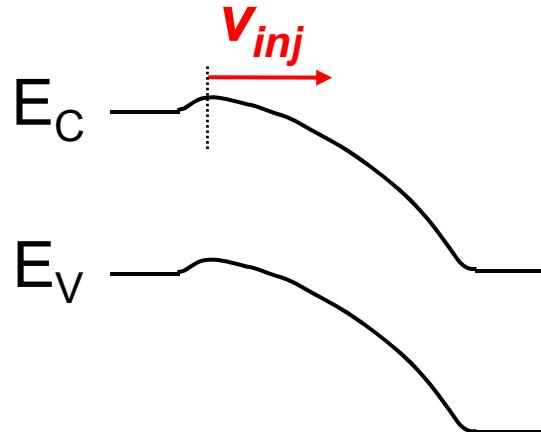
Werner, JAP 2011

Brammertz, APL 2009

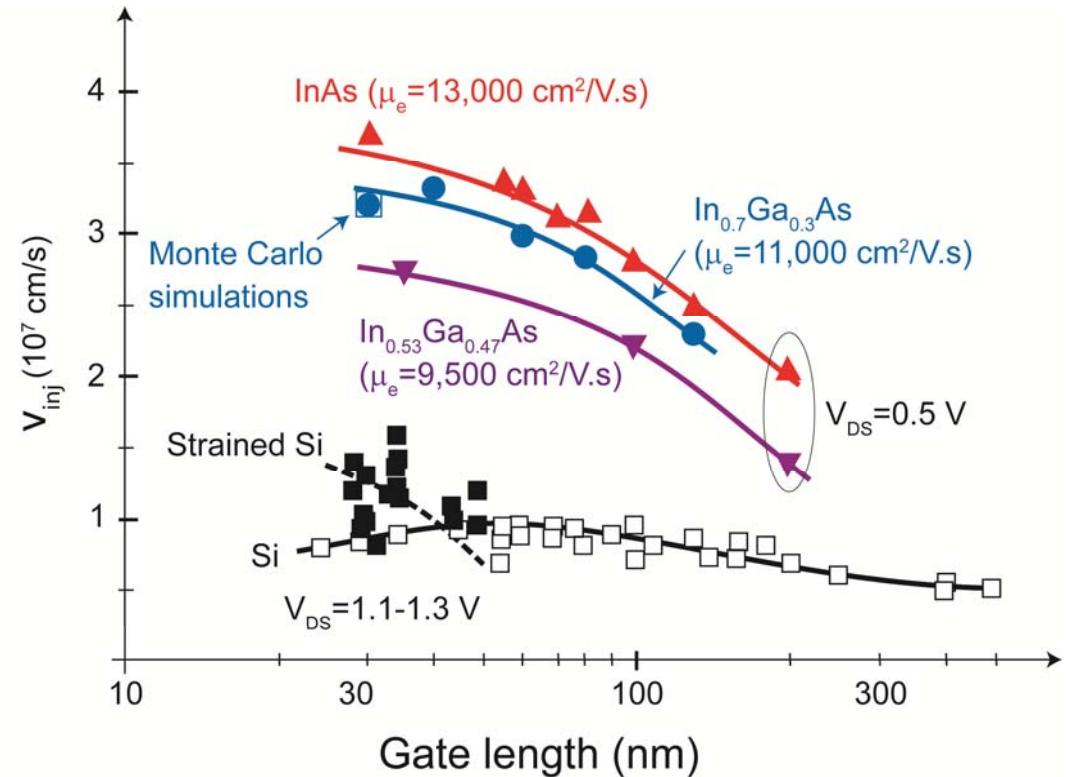
Close to conduction band edge, $\text{Al}_2\text{O}_3/\text{InGaAs}$ shows comparable interface state density to $\text{Al}_2\text{O}_3/\text{Si}$ interface

Electron injection velocity: InGaAs vs. Si

Measurements of electron injection velocity in HEMTs:



Kim, IEDM 2009
Liu, Springer 2010
Khakifirooz, TED 2008
del Alamo, Nature 2011

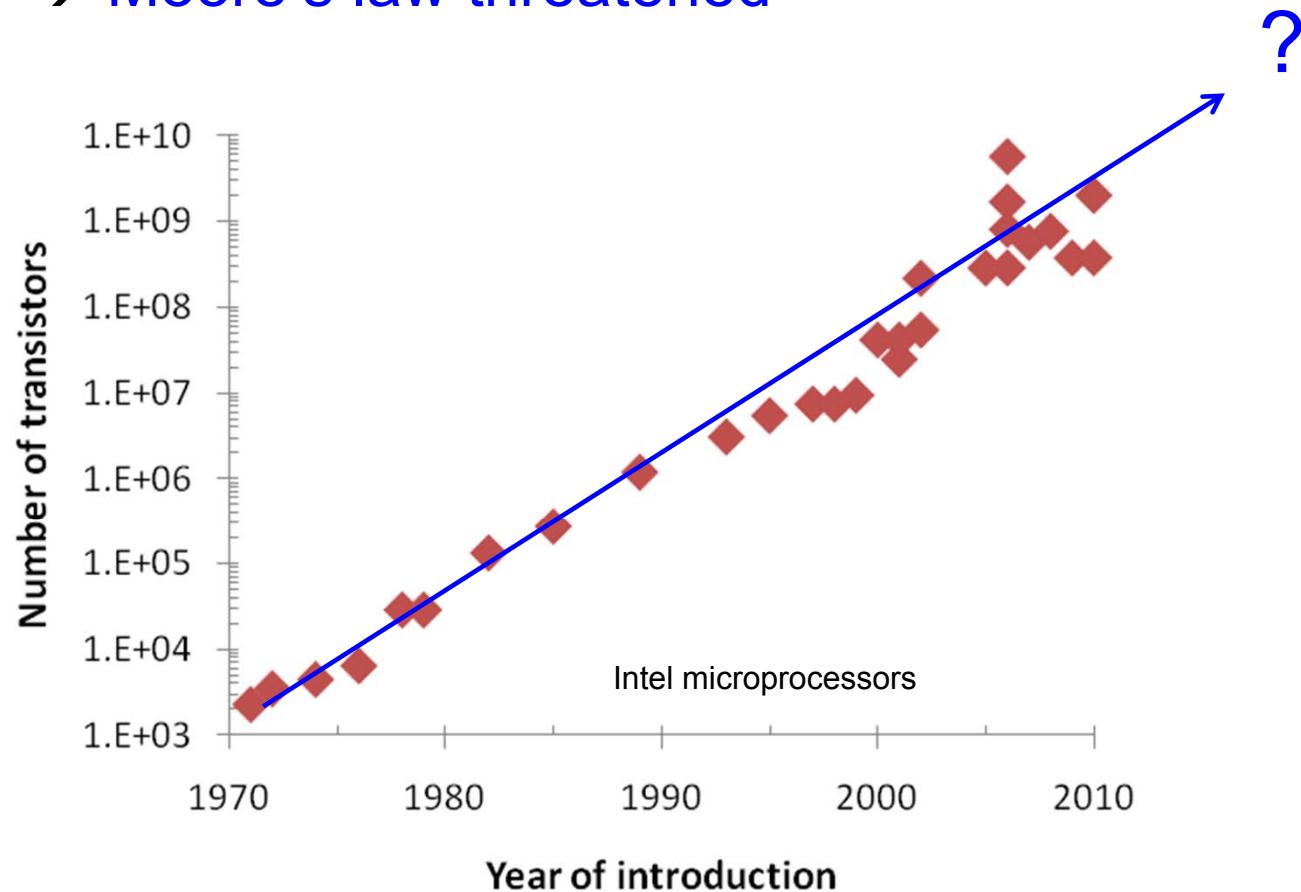


- $v_{inj}(\text{InGaAs})$ increases with InAs fraction in channel
- $v_{inj}(\text{InGaAs}) > 2v_{inj}(\text{Si})$ at less than half V_{DD}
- ~100% ballistic transport at $L_g \sim 30 \text{ nm}$

InGaAs n-MOSFET: best candidate for post-Si CMOS

Si CMOS scaling seriously stressed

→ Moore's law threatened





The III-V view



The III-V view

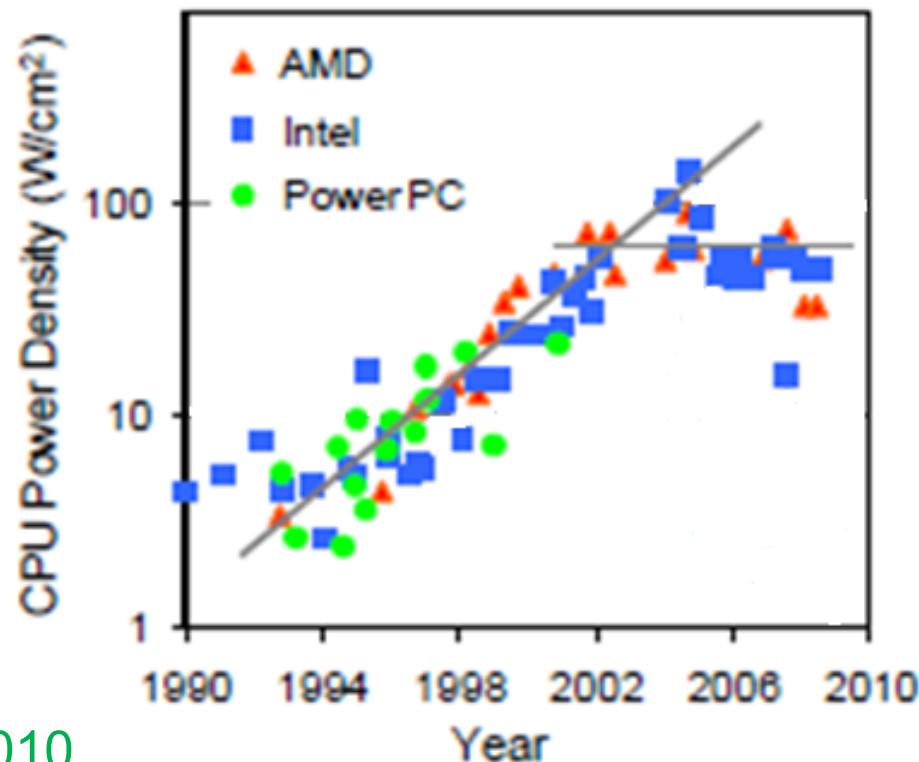


The Si view

CMOS scaling in the 21st century

Si CMOS has entered era of “*power-constrained scaling*”:

→ Microprocessor power density saturated at ~100 W/cm²

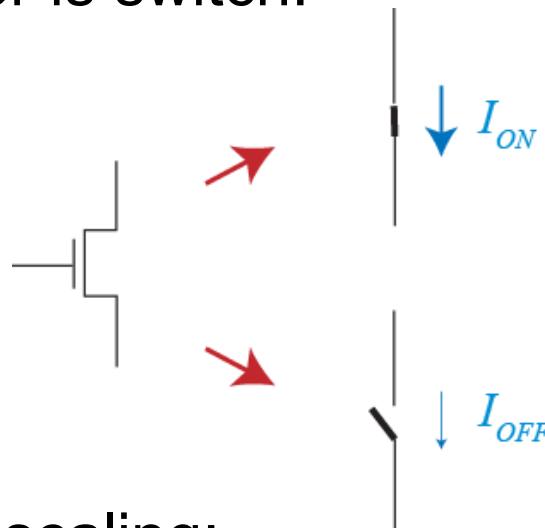


Pop, Nano Res 2010

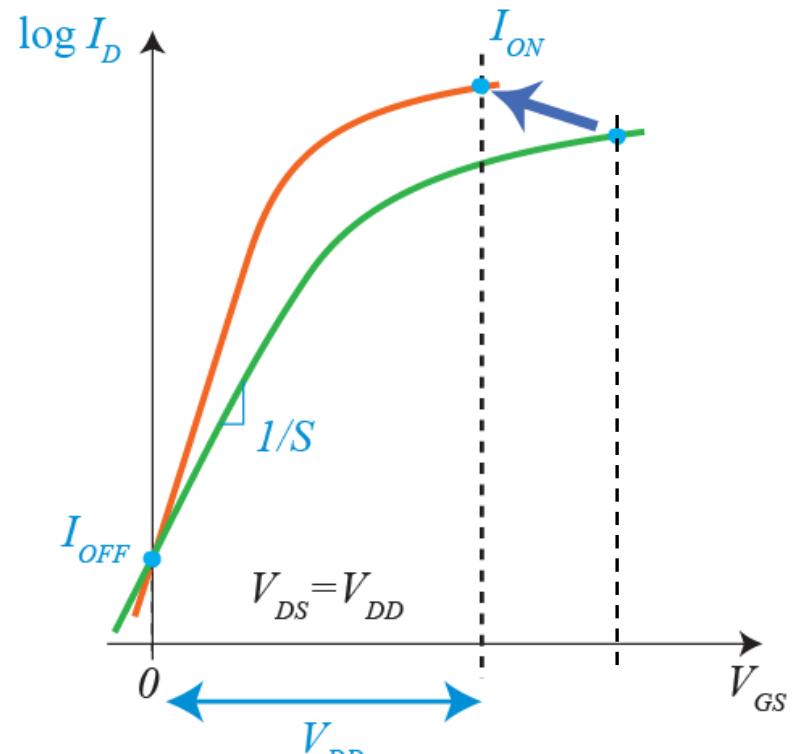
Future scaling demands $V_{DD} \downarrow$

How to enable further V_{DD} reduction?

- Transistor is switch:



- Goals of scaling:
 - reduce transistor footprint
 - reduce V_{DD}
 - extract maximum I_{ON} for given I_{OFF}

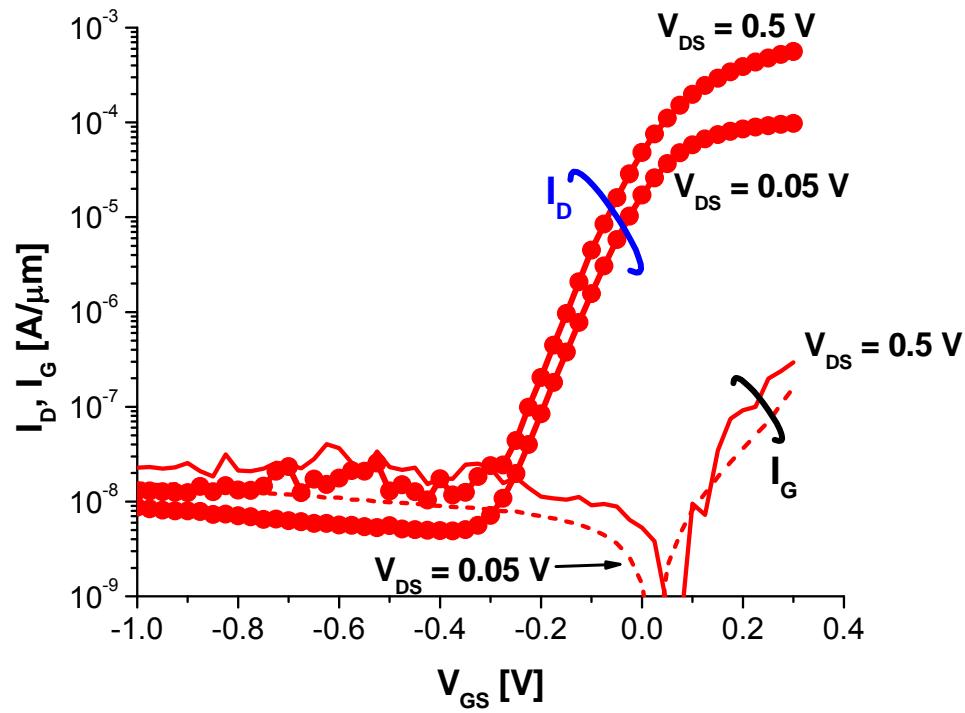


- The path forward:
 - increase electron velocity $\rightarrow I_{ON} \uparrow$
 - tighten electron confinement $\rightarrow S \downarrow$

} \rightarrow use InGaAs!

$L_g = 30 \text{ nm InGaAs HEMT} -$ Subthreshold characteristics

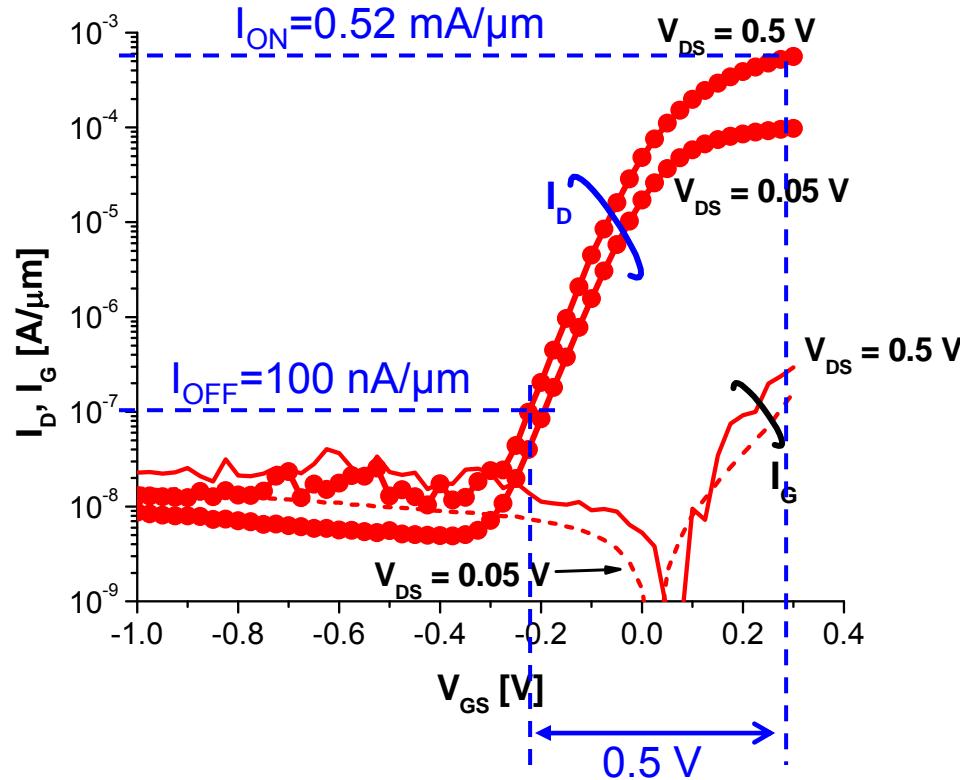
Kim, EDL 2010



- $S = 74 \text{ mV/dec}$
- Sharp subthreshold behavior due to tight electron confinement in quantum well

$L_g = 30 \text{ nm InGaAs HEMT} -$ Subthreshold characteristics

Kim, EDL 2010

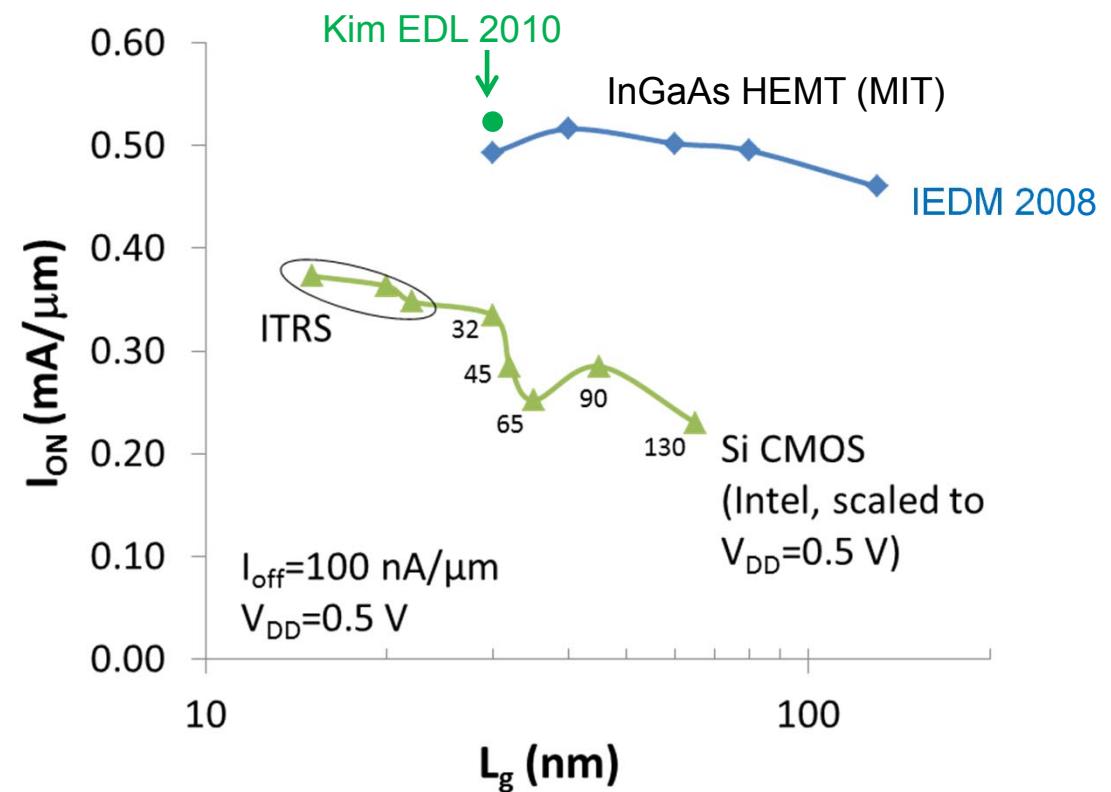
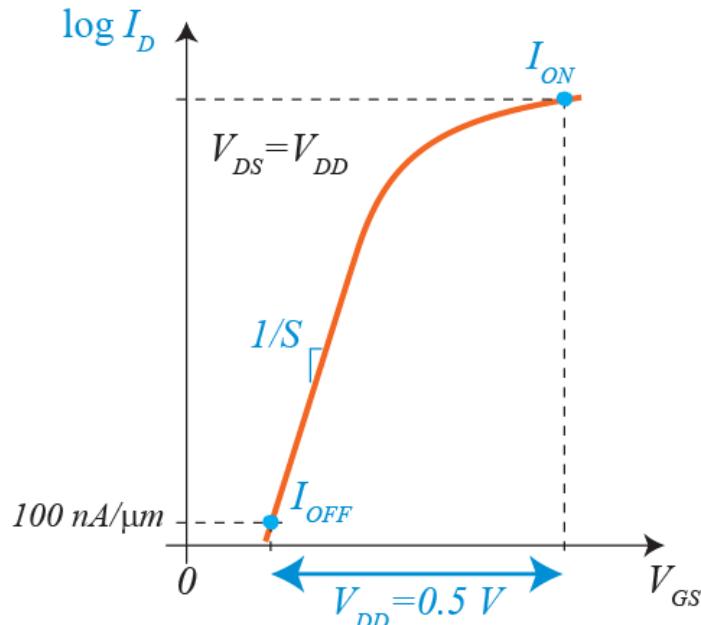


- $S = 74 \text{ mV/dec}$
- At $I_{OFF} = 100 \text{ nA}/\mu\text{m}$ and $V_{DD} = 0.5 \text{ V}$, $I_{ON} = 0.52 \text{ mA}/\mu\text{m}$

InGaAs HEMTs: Benchmarking with Si

FOM that integrates short-channel effects and transport:

I_{ON} @ $I_{OFF}=100 \text{ nA}/\mu\text{m}$, $V_{DD}=0.5 \text{ V}$



InGaAs HEMTs: higher I_{ON} for same I_{OFF} than Si

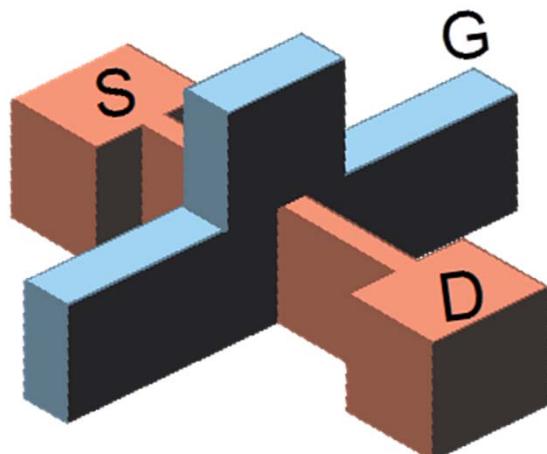
III-V MOSFET: possible designs



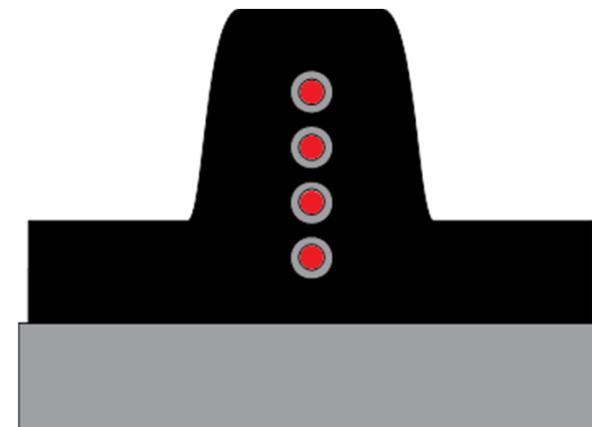
Recessed S/D QW-MOSFET



Regrown S/D QW-MOSFET



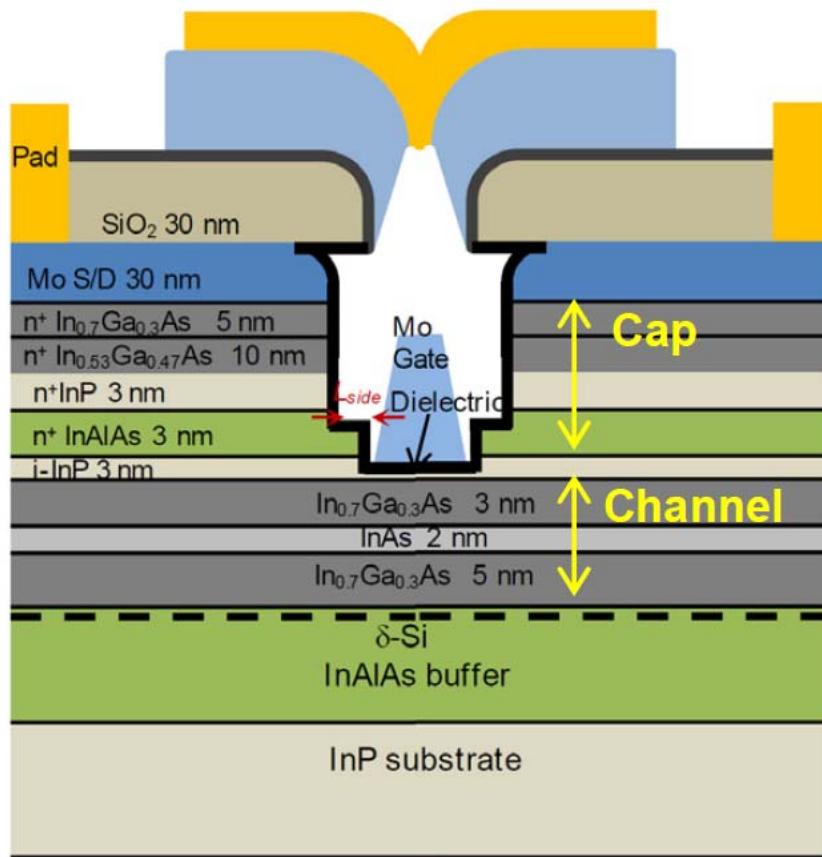
Trigate MOSFET



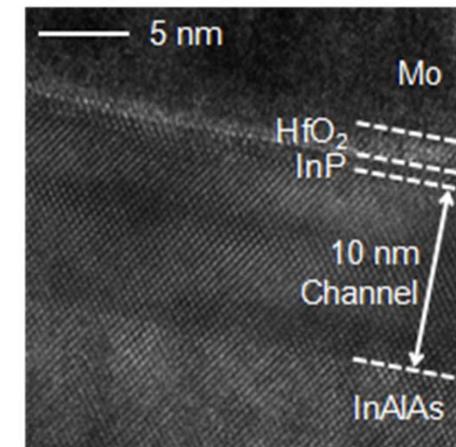
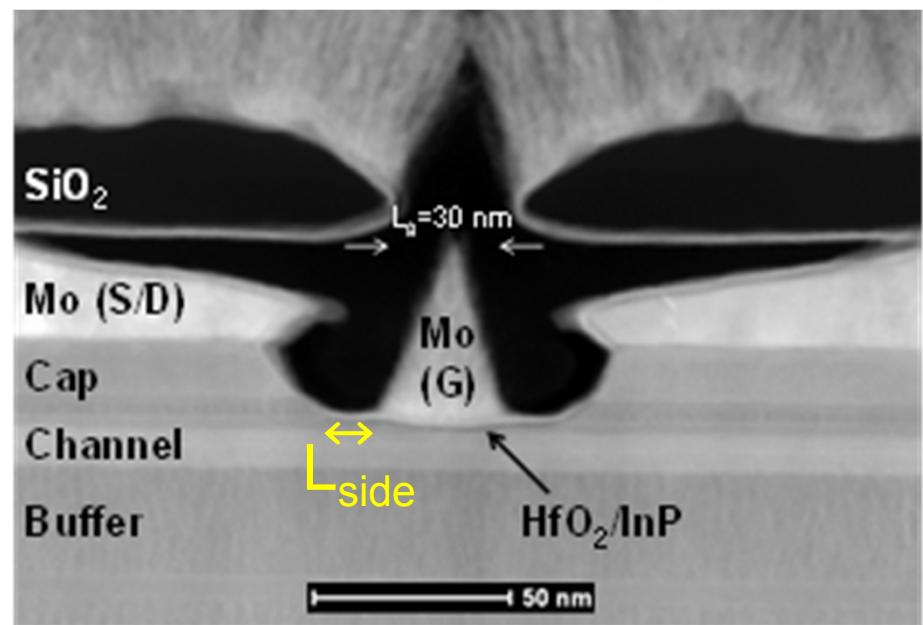
Nanowire MOSFET

Self-Aligned InGaAs QW-MOSFETs (MIT)

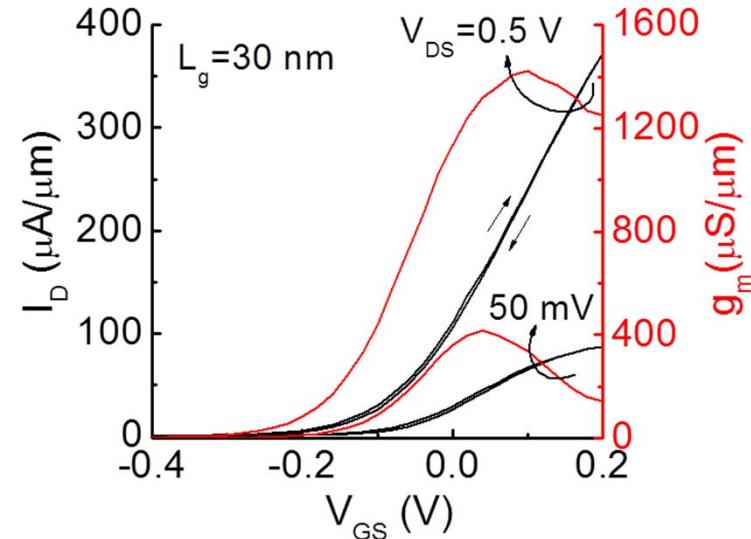
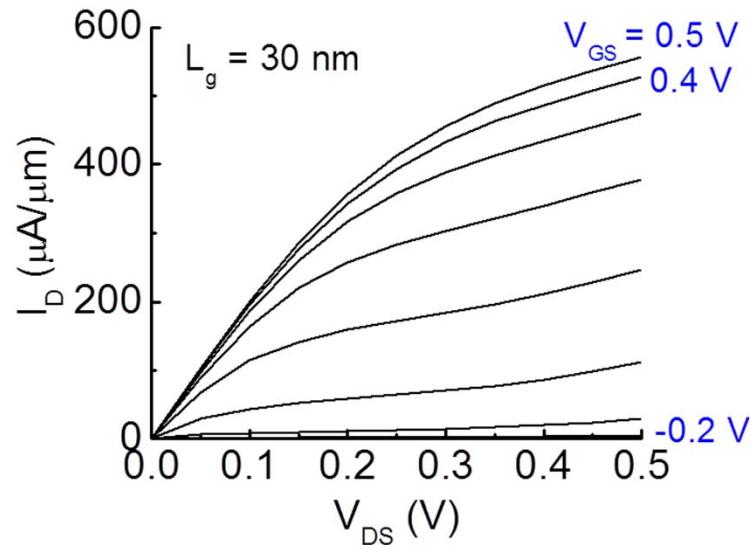
- Scaled barrier (InP: 1 nm + HfO₂: 2 nm)
- 10 nm thick channel with InAs core
- Tight S/D spacing ($L_{\text{side}} \sim 30$ nm)
- Process designed to be compatible with Si fab



Lin, IEDM 2012

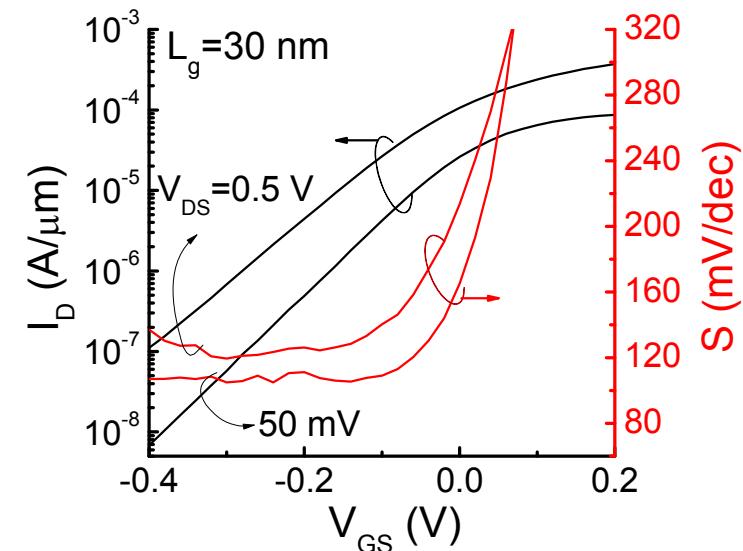


$L_g=30$ nm Self-aligned QW-MOSFET

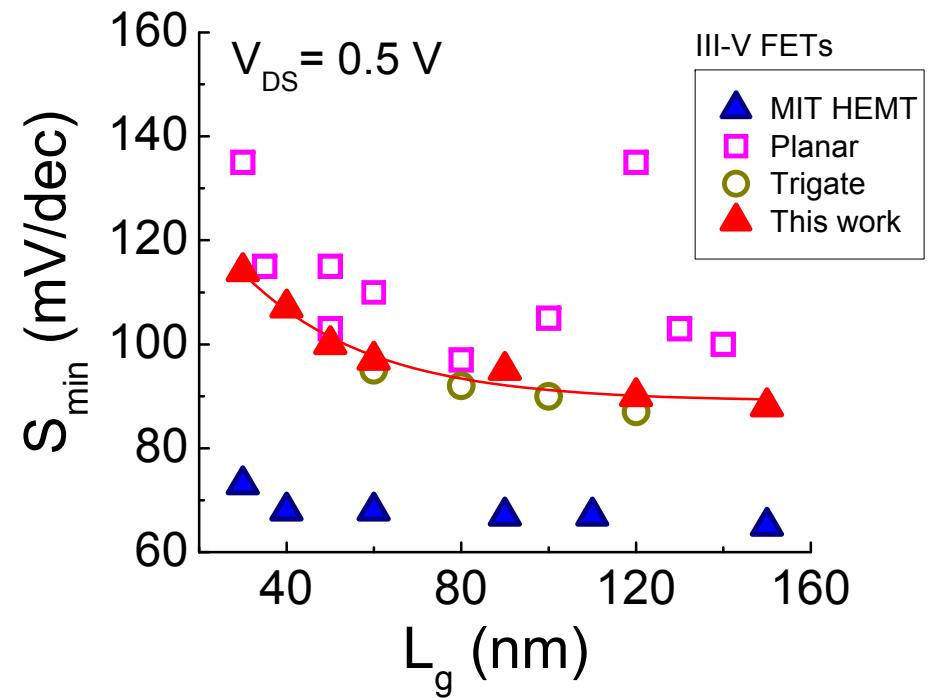
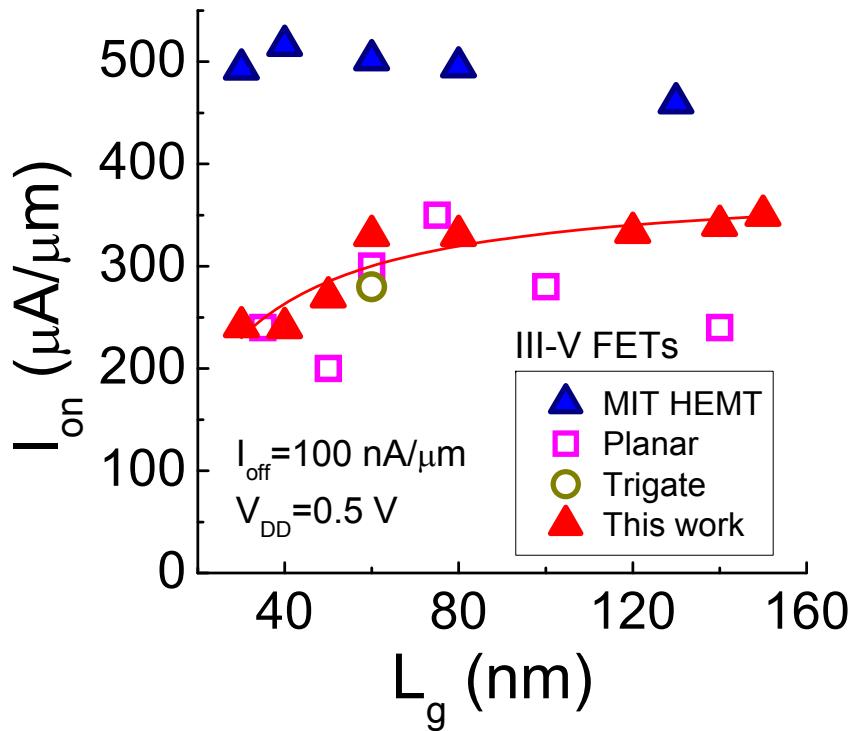


At $V_{DS} = 0.5$ V:

- $g_m = 1.4 \text{ mS}/\mu\text{m}$
- $S = 114 \text{ mV/dec}$
- $R_{ON} = 470 \Omega.\mu\text{m}$



Scaling and benchmarking

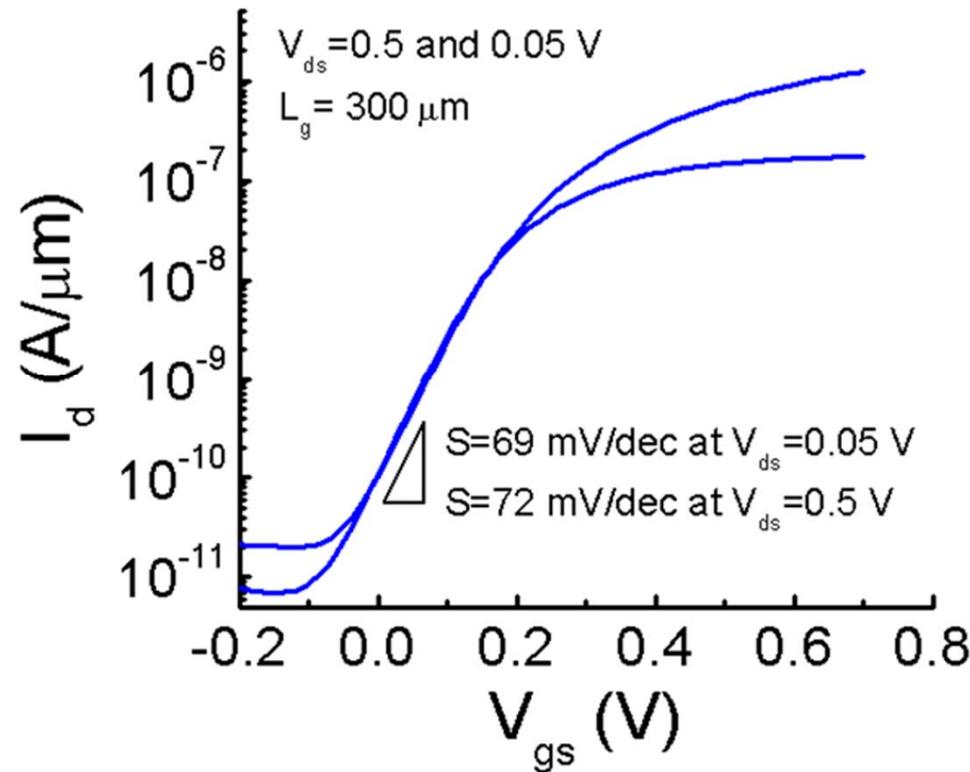


Lin, IEDM 2012

- Superior behavior to any planar III-V MOSFET to date
- Matches performance of Intel's InGaAs Trigate MOSFETs
[Radosavljevic, IEDM 2011]

Long-channel InGaAs MOSFET

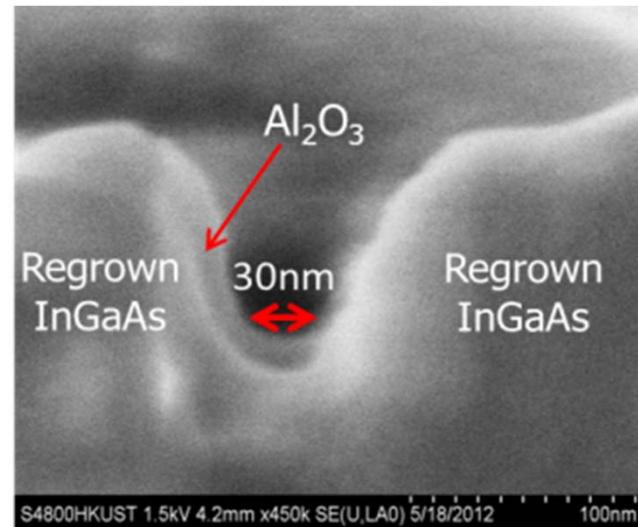
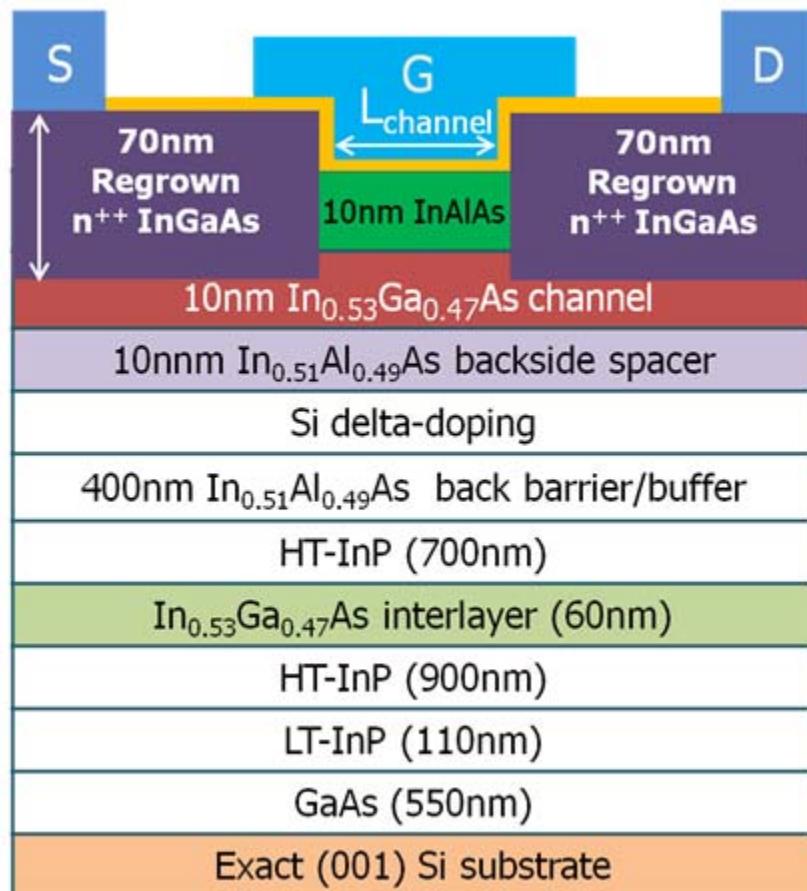
Barrier: InP (1 nm) + Al₂O₃ (0.4 nm) + HfO₂ (2 nm)



Lin, IEDM 2012

- $S = 69 \text{ mV/dec at } V_{DS} = 50 \text{ mV}$
- Close to lowest S reported in any III-V MOSFET: 66 mV/dec
[Radosavljevic, IEDM 2011]

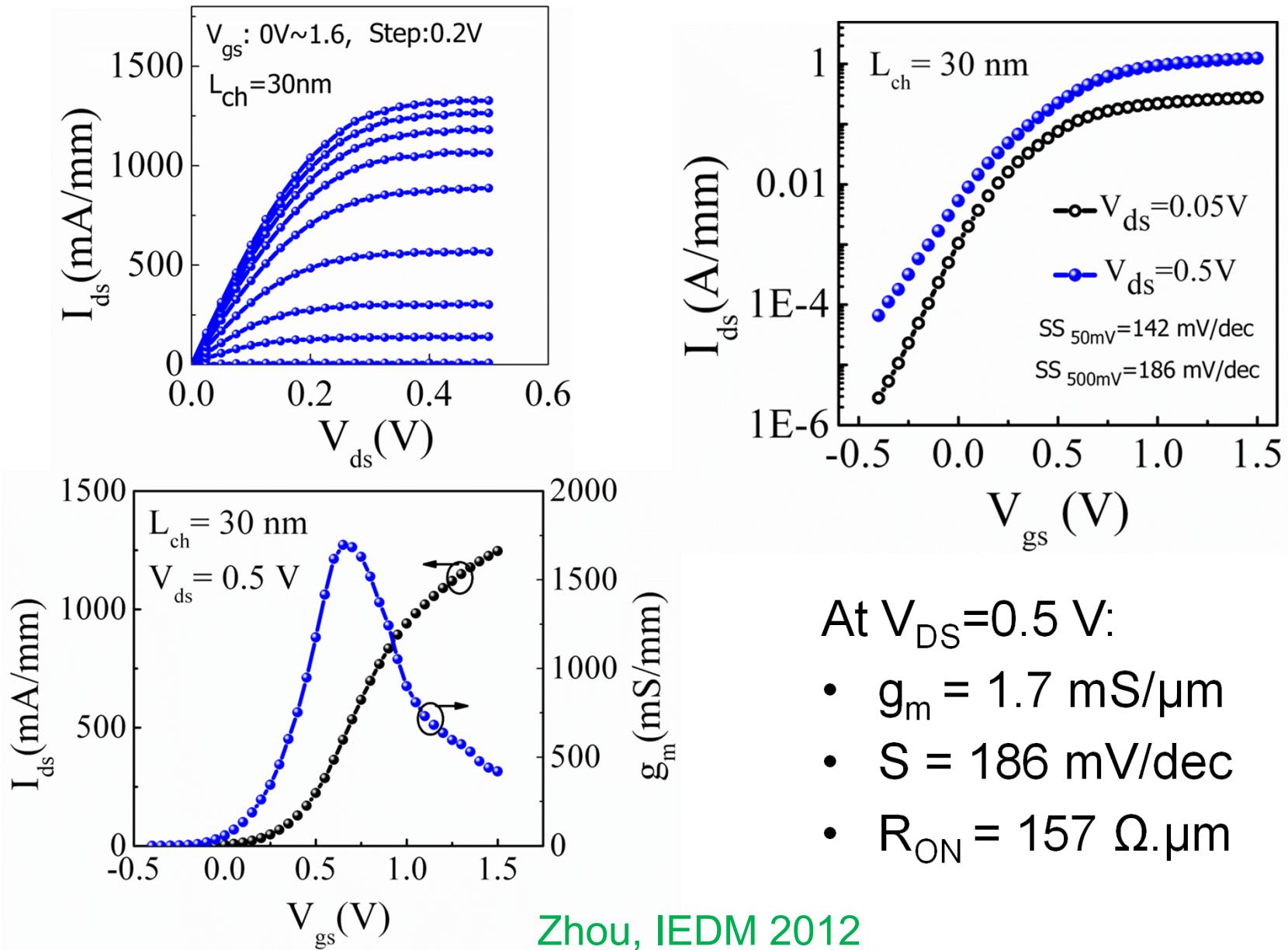
Regrown source/drain InGaAs QW-MOSFET on Si (HKUST)



- MOCVD epi growth on Si wafer
- n⁺-InGaAs raised source/drain
- Self-aligned to gate
- Composite barrier:
InAlAs (10 nm) + Al₂O₃ (4.6 nm)

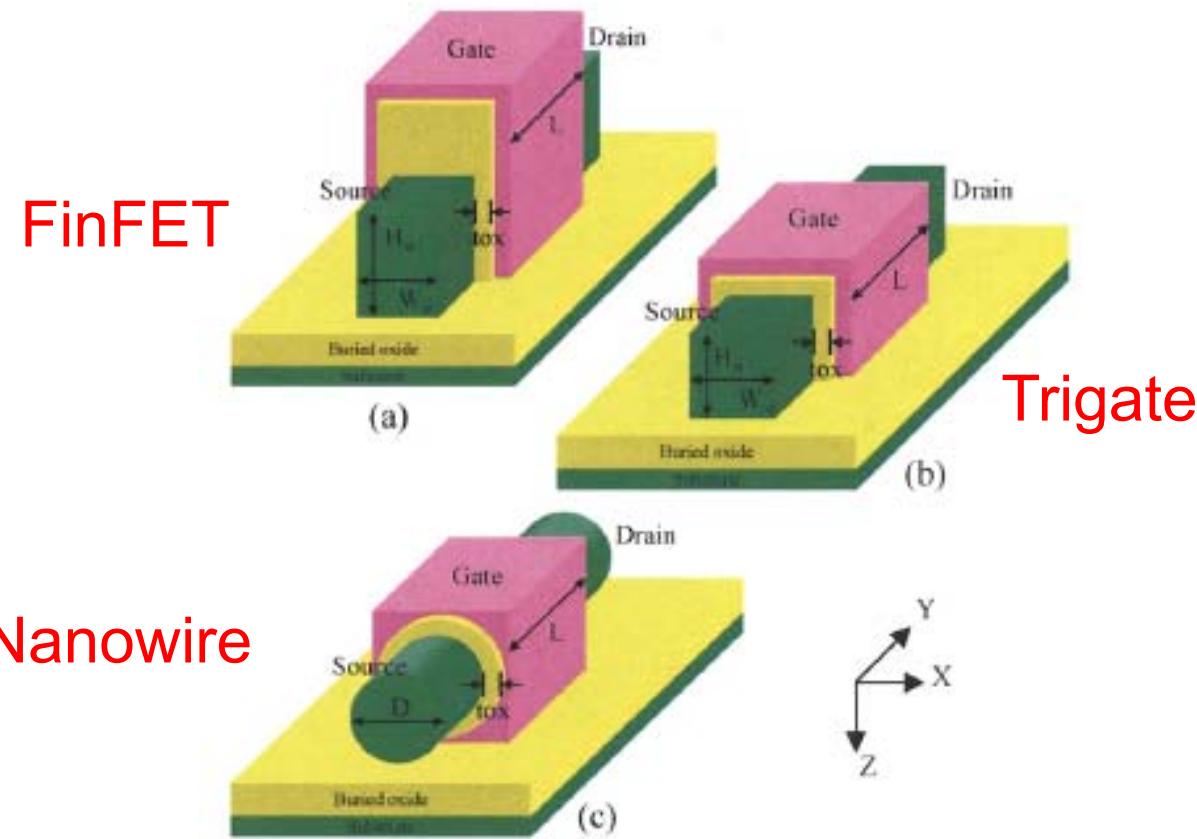
Zhou, IEDM 2012

Characteristics of $L_g=30$ nm MOSFET

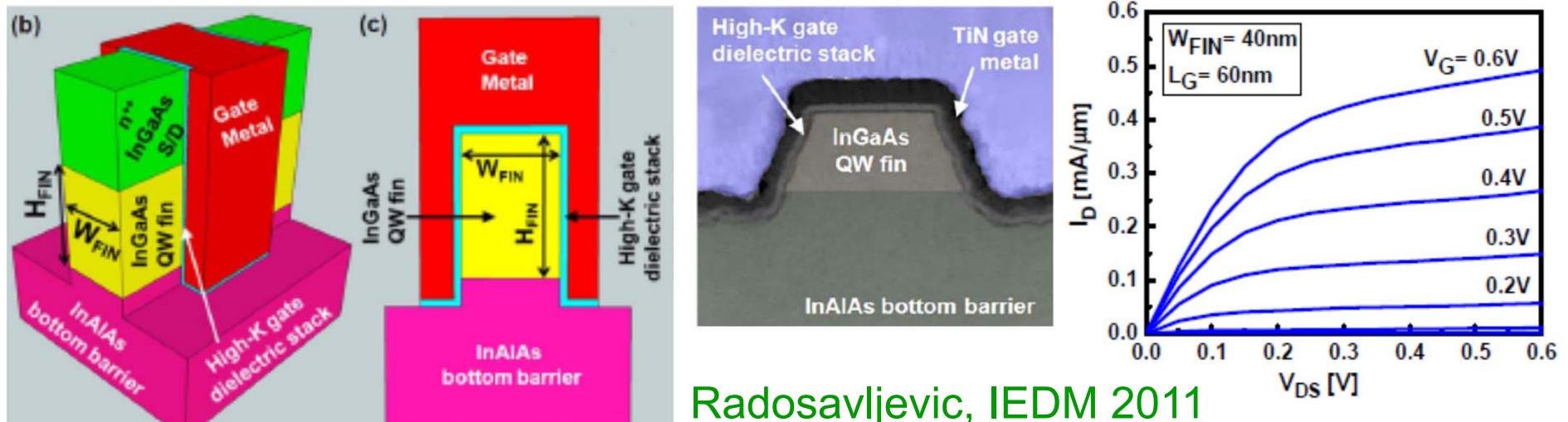


Multiple-gate MOSFETs

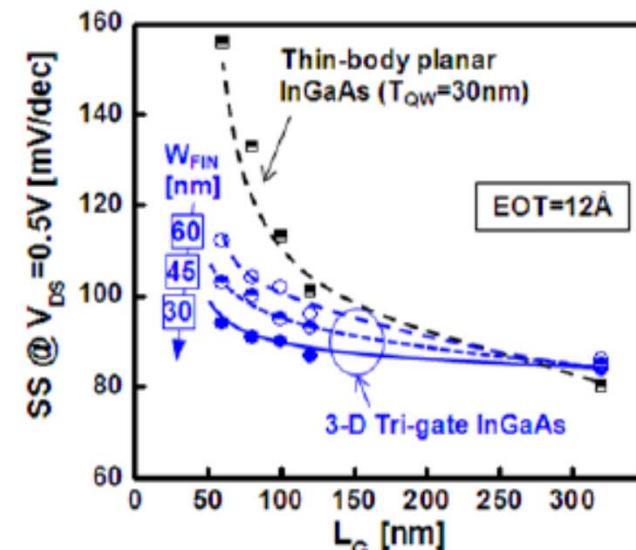
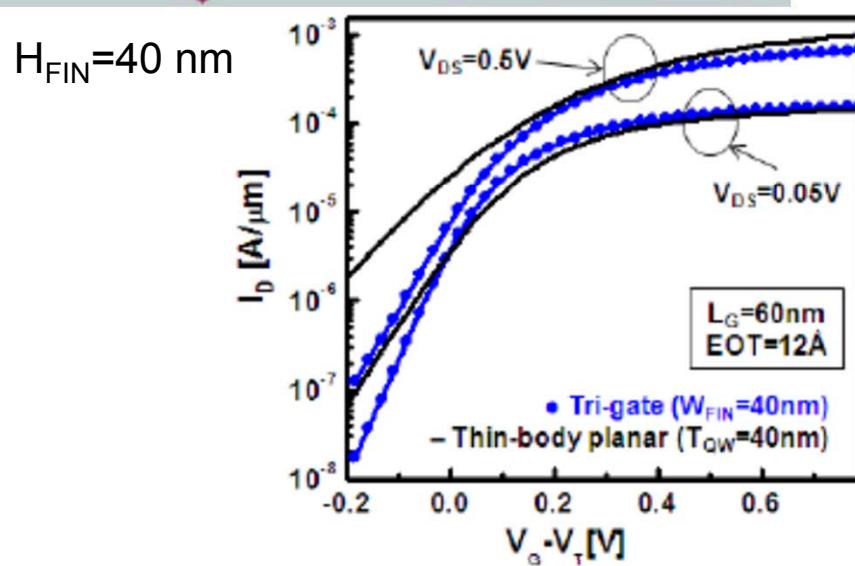
gates $\uparrow \rightarrow$ improved electrostatics \rightarrow enhanced scalability



InGaAs Trigate MOSFET (Intel)

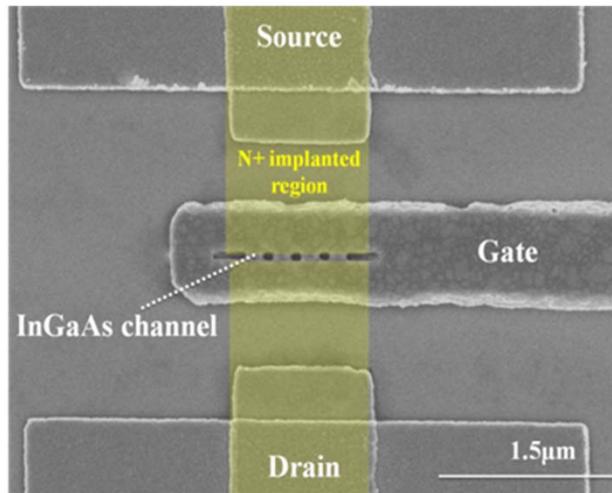
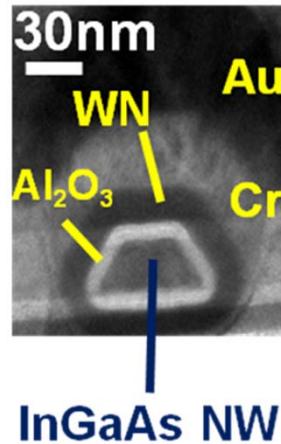
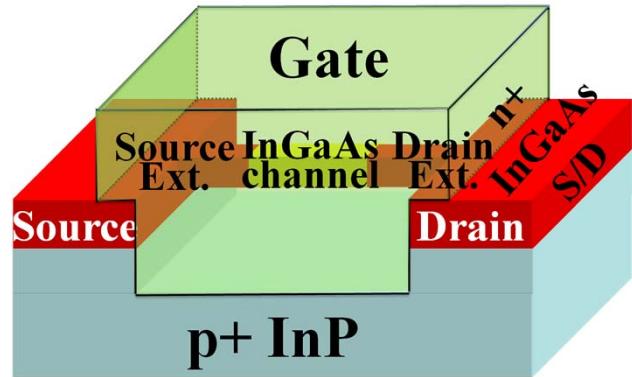


Radosavljevic, IEDM 2011

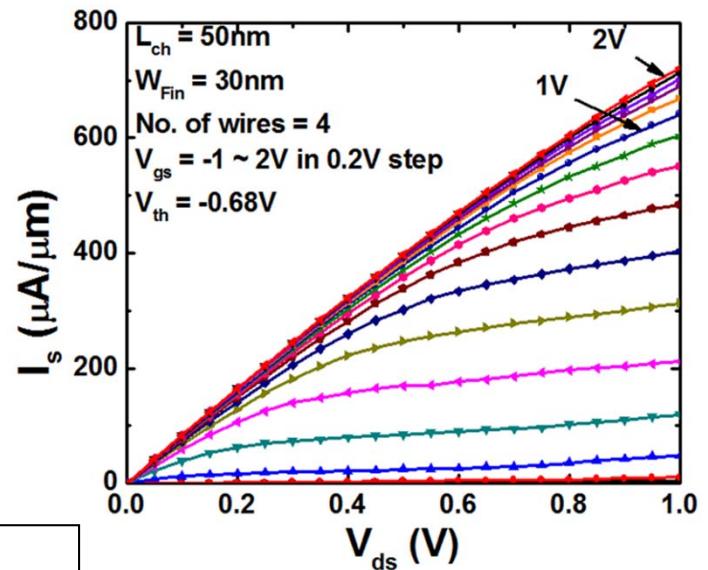


Improved subthreshold swing as fin is made thinner

InGaAs Nanowire MOSFET (Purdue)



30x30 nm fin
 $L_{ch} = 50$ nm
 Barrier: 10 nm Al_2O_3
 # wires = 4



Gu, IEDM 2011
 Gu, APL 2011
 Gu, EDL 2012

- $I_{on} = 720 \mu\text{A}/\mu\text{m}$ ($86 \mu\text{A}/\text{wire}$)
- $g_m = 0.51 \text{ mS}/\mu\text{m}$ ($61 \mu\text{S}/\text{wire}$)
- $S = 150 \text{ mV/dec}$

Conclusions: exciting future for InGaAs

- Most promising material for ultra-high frequency and ultra-high speed applications
→ first THz transistor?
- Most promising material for n-MOSFET in a post-Si CMOS logic technology
→ first sub-10 nm CMOS logic?
- InGaAs + Si integration:
→ THz + CMOS + optics integrated systems?