

THz III-V HEMT Technology

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International Wireless Symposium 2013

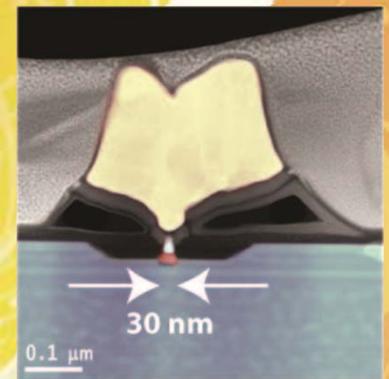
Workshop on THz Material Growth, Device Fabrication and Modeling

Beijing, April 14, 2013

Acknowledgements: Dae-Hyun Kim, Jianqiang Lin, Tae-Woo Kim, Niamh Waldron

Sponsors: FCRP-MSD, Intel, SRC, ARL

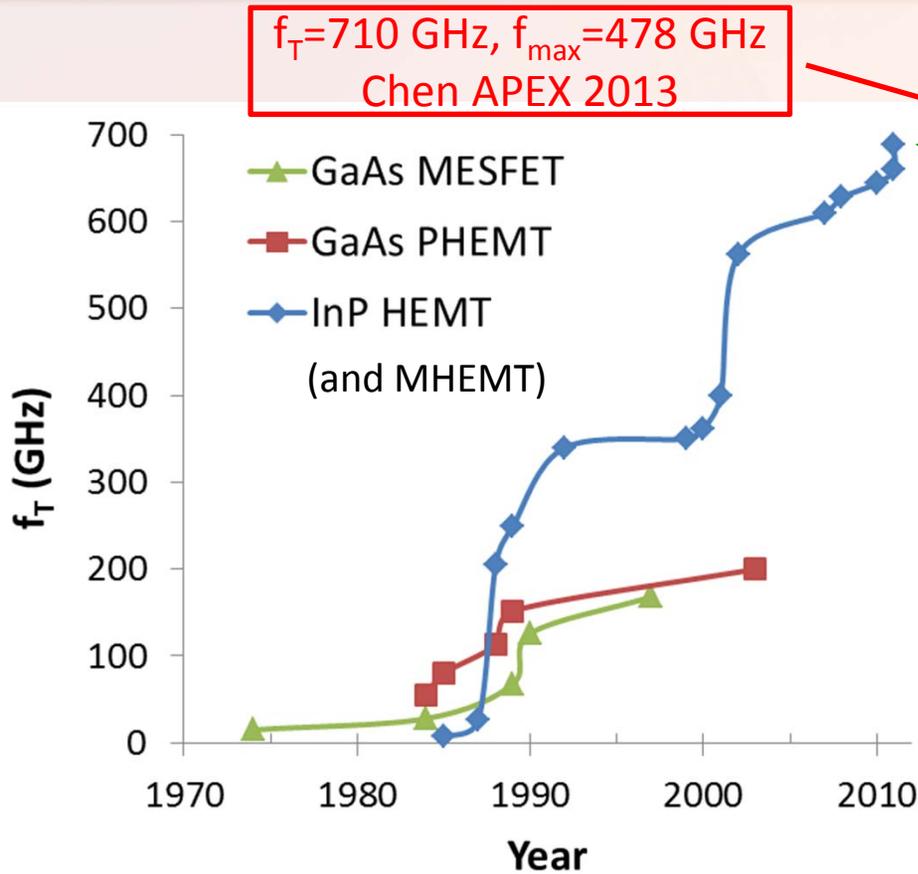
Labs at MIT: MTL, SEBL, NSL



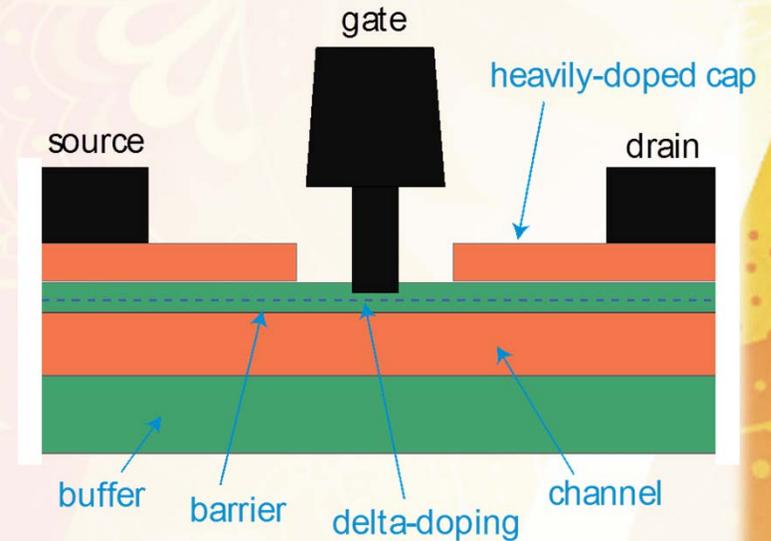
Outline

1. High-frequency III-V HEMTs: megatrends
2. State-of-the-art InGaAs HEMTs and f_T analysis
3. The path to THz operation

1. III-V HEMT: record f_T vs. time

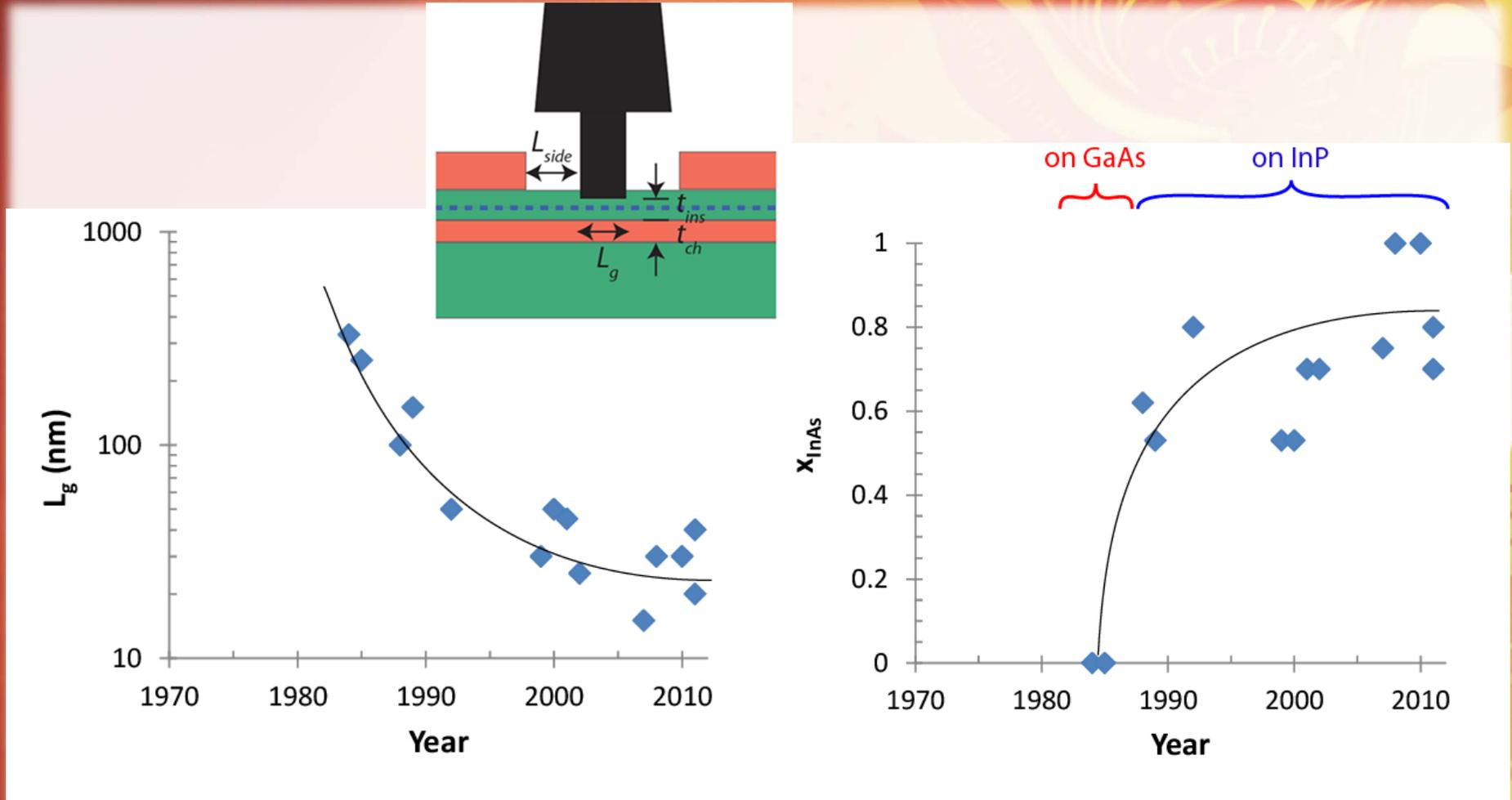


Current record:
 $f_T = 688$ GHz
 $f_{max} = 800$ GHz
 Kim IEDM 2011
 (Teledyne/MIT)



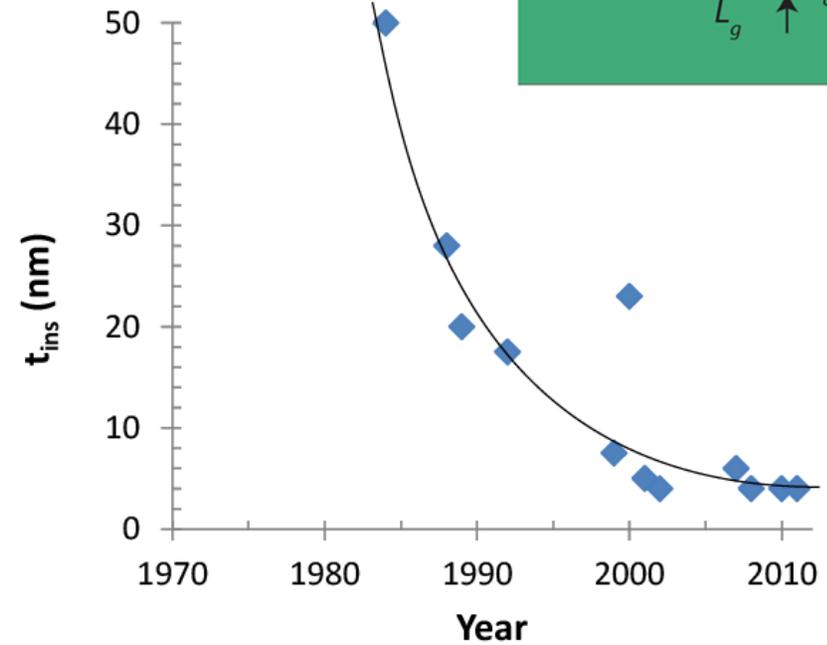
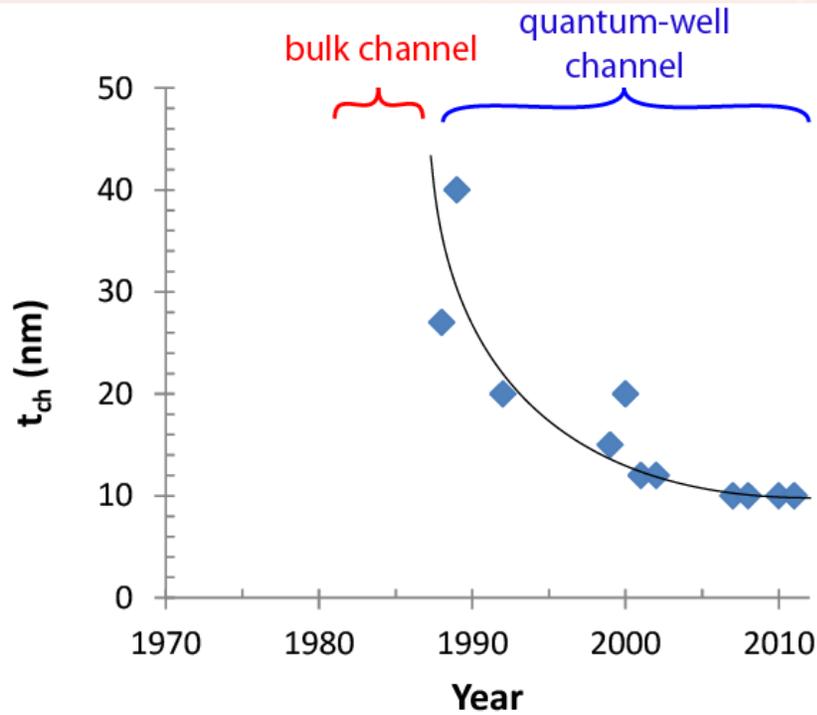
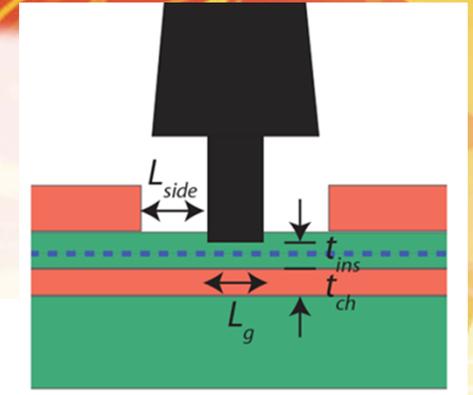
- For >20 years, record f_T obtained on InGaAs-channel HEMTs
- InGaAs-channel HEMTs offer record balanced f_T and f_{max}

Record f_T III-V HEMTs: megatrends



- Over time: $L_g \downarrow$, $In_xGa_{1-x}As$ channel $x_{InAs} \uparrow$
- L_g, x_{InAs} saturated \rightarrow no more progress possible?

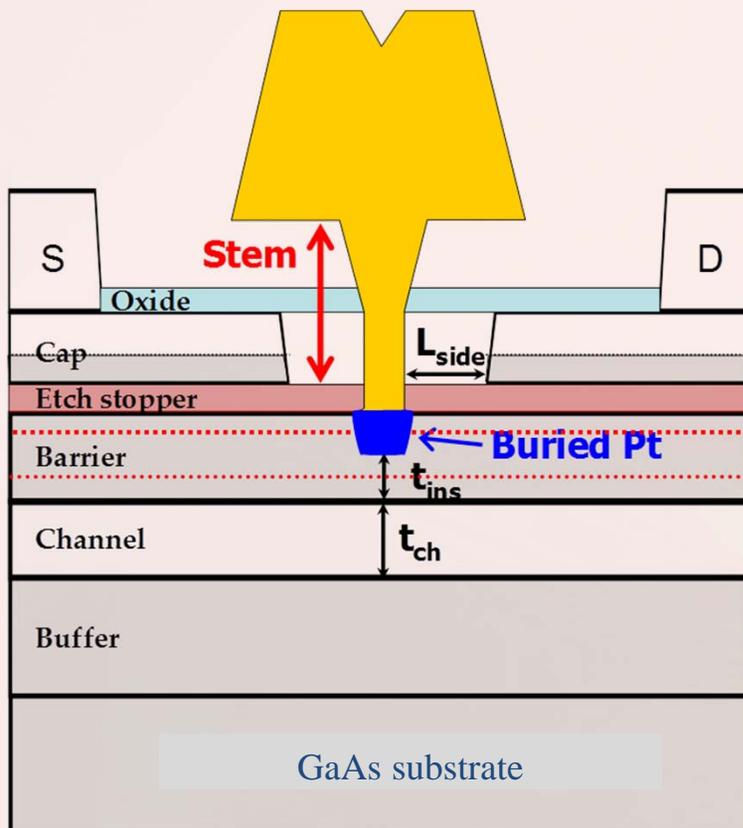
Record f_T III-V HEMTs: megatrends



- Over time: $t_{ch} \downarrow$, $t_{ins} \downarrow$
- t_{ch} , t_{ins} saturated \rightarrow no more progress possible?

2. State-of-the-art InGaAs HEMT

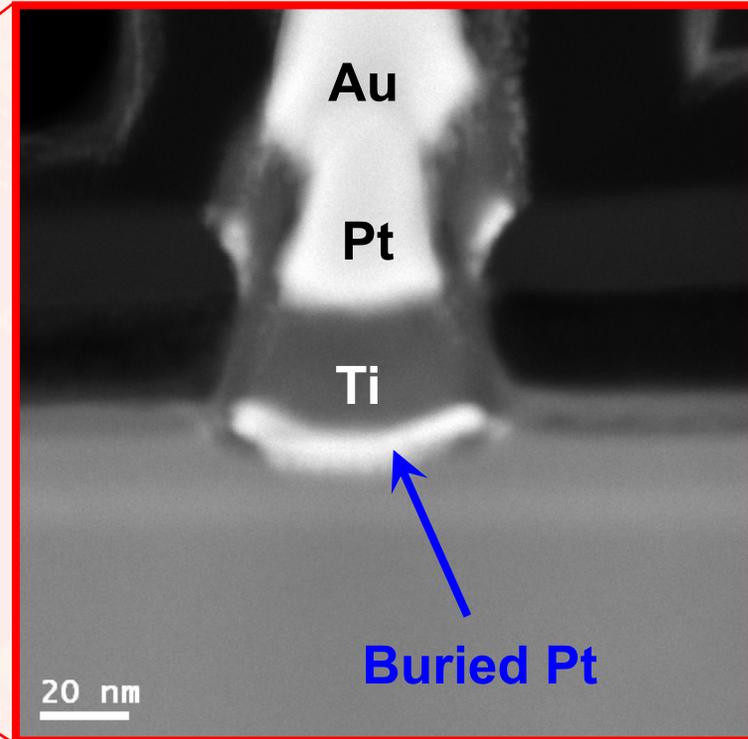
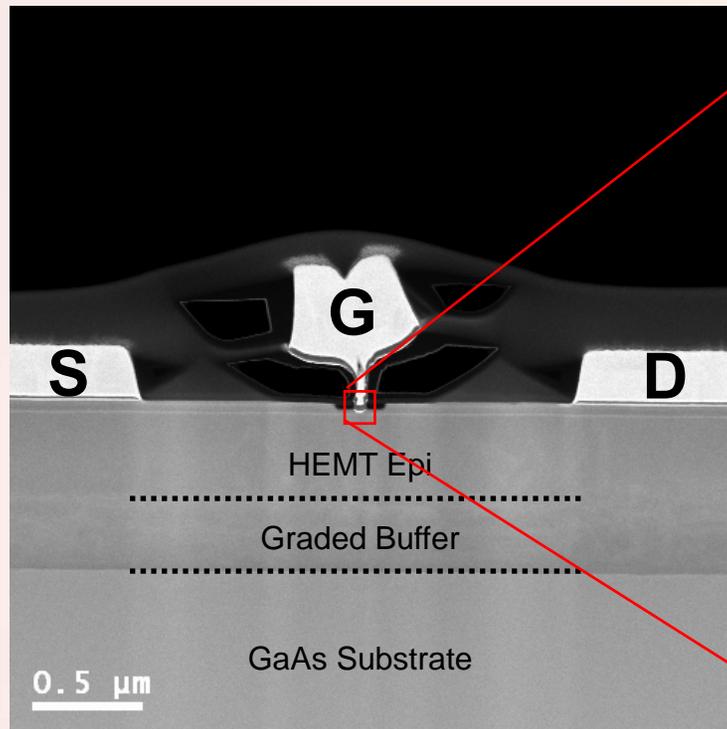
$L_g=40$ nm InGaAs Metamorphic HEMT



Kim, IEDM 2011

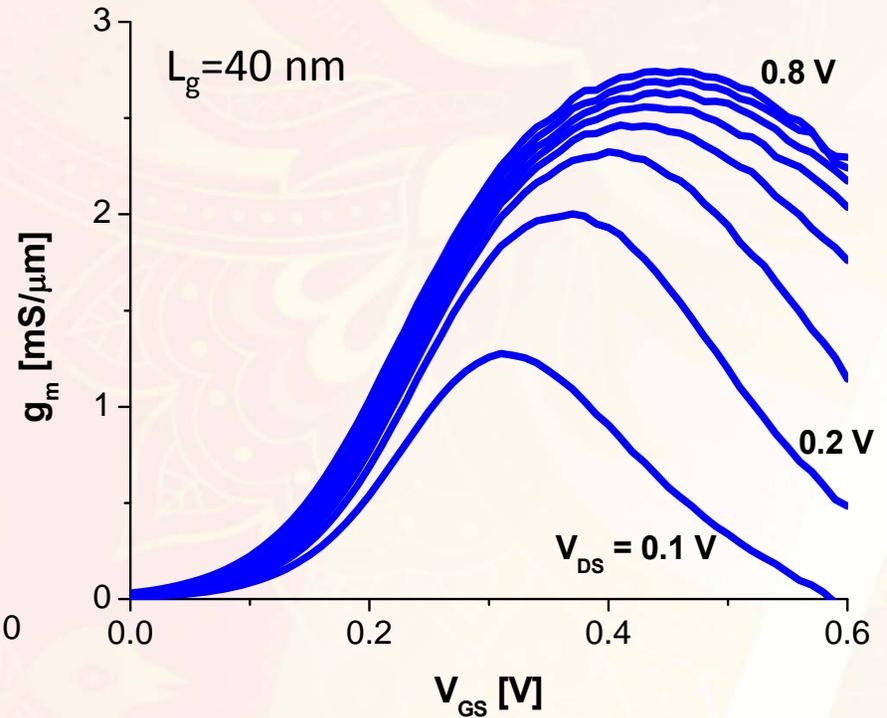
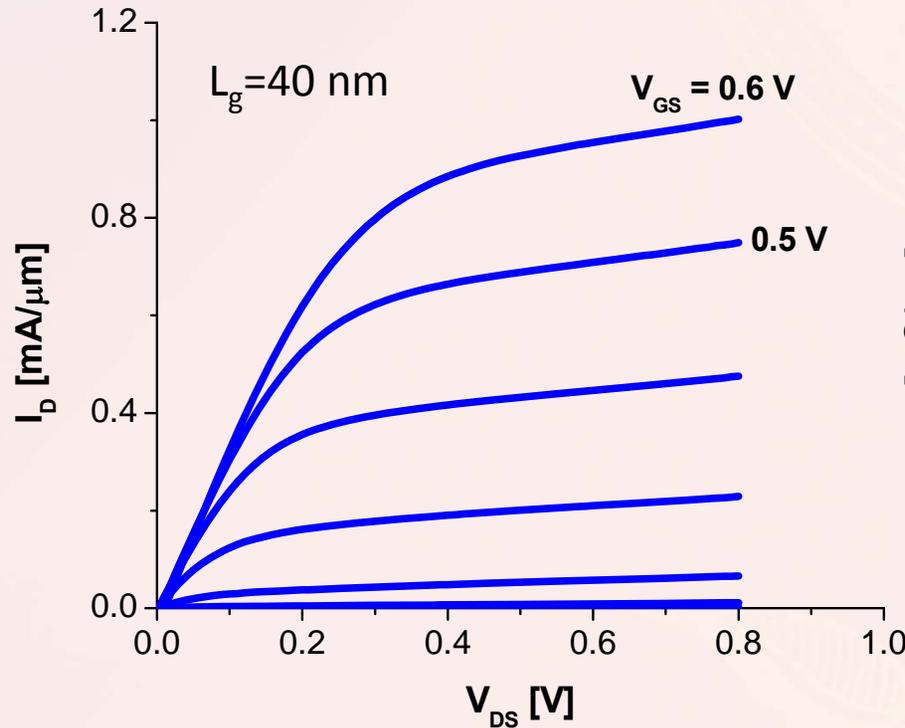
- $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ QW channel
 - $t_{\text{ch}} = 10$ nm
 - $\mu_{n,\text{Hall}} > 10,000$ cm²/V-sec
- $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier + $\text{In}_{0.7}\text{Al}_{0.3}\text{As}$ spacer (Kim, EL 2011)
- Dual Si δ -doping (Kim, IEDM 2010)
- Pt (3 nm)/Ti/Pt/Au Schottky
- $t_{\text{ins}} = 4$ nm
- InP etch stop ($t_{\text{InP}} = 6$ nm)
- $L_{\text{side}} = 100$ nm
- Gate stem > 250 nm
- Mo-based S/D with 2 μm S-D spacing

TEM cross section



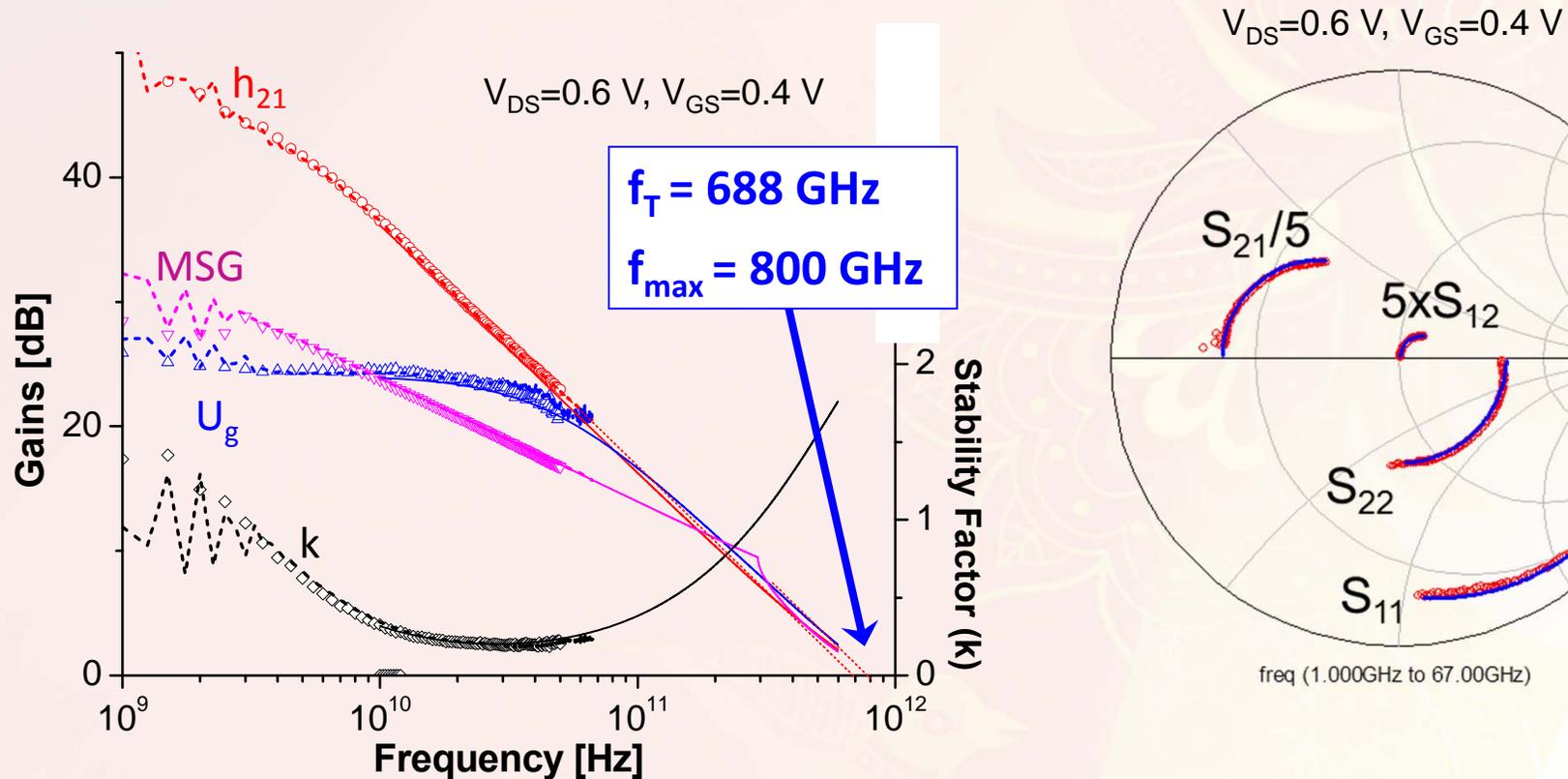
Output and transfer characteristics

Kim, IEDM 2011



- Large current drive: $I_D > 1 \text{ mA}/\mu\text{m}$ at $V_{DS} = 0.8 \text{ V}$
- High transconductance: $g_{\text{mpk}} = 2.75 \text{ mS}/\mu\text{m}$ at $V_{DS} = 0.8 \text{ V}$
- $V_T \approx 0 \text{ V}$, $R_{\text{ON}} = 280 \Omega \cdot \mu\text{m}$

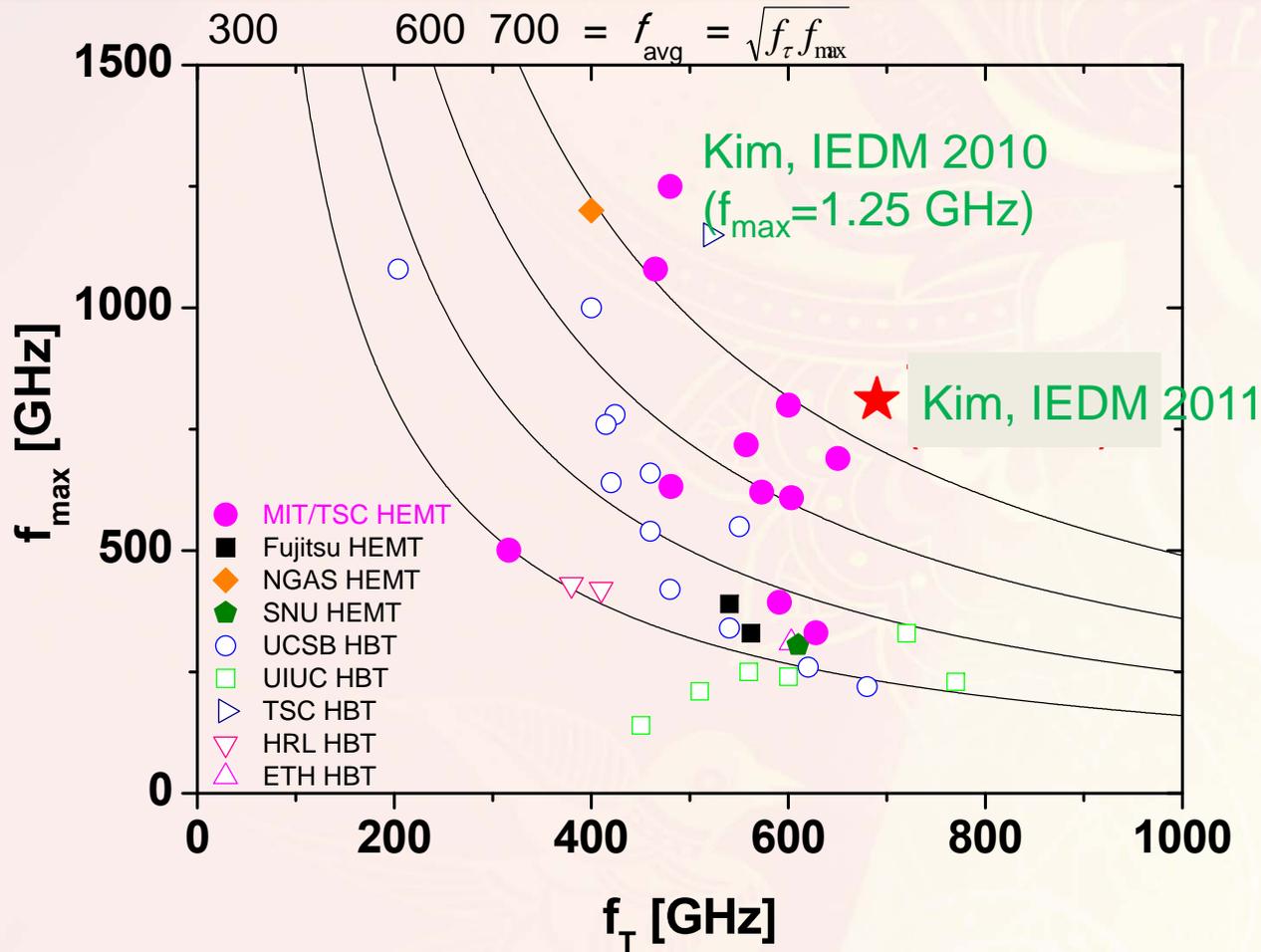
High-frequency characteristics



- Only transistor of any kind with both f_T and $f_{max} > 680\text{ GHz}$
- Obtained at same bias point, $V_{DS}=0.6\text{ V}$

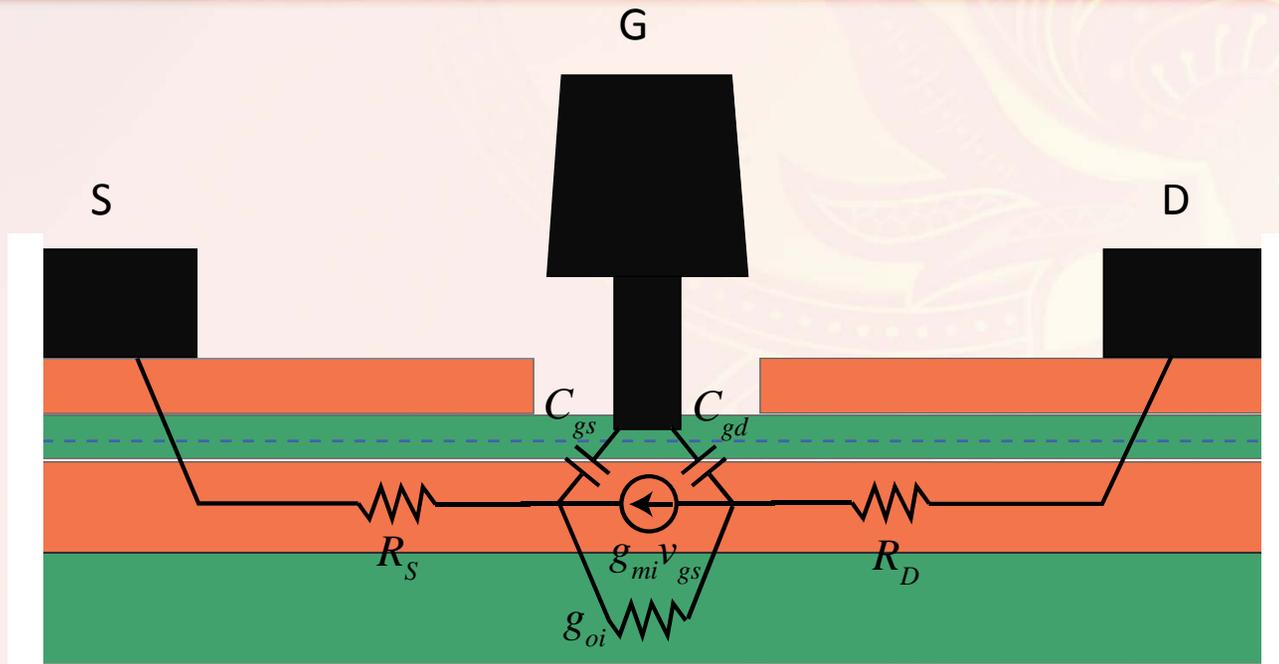
Kim, IEDM 2011

f_T VS. f_{max}



- Record f_T FET
- Best-balanced f_T and f_{max} transistor

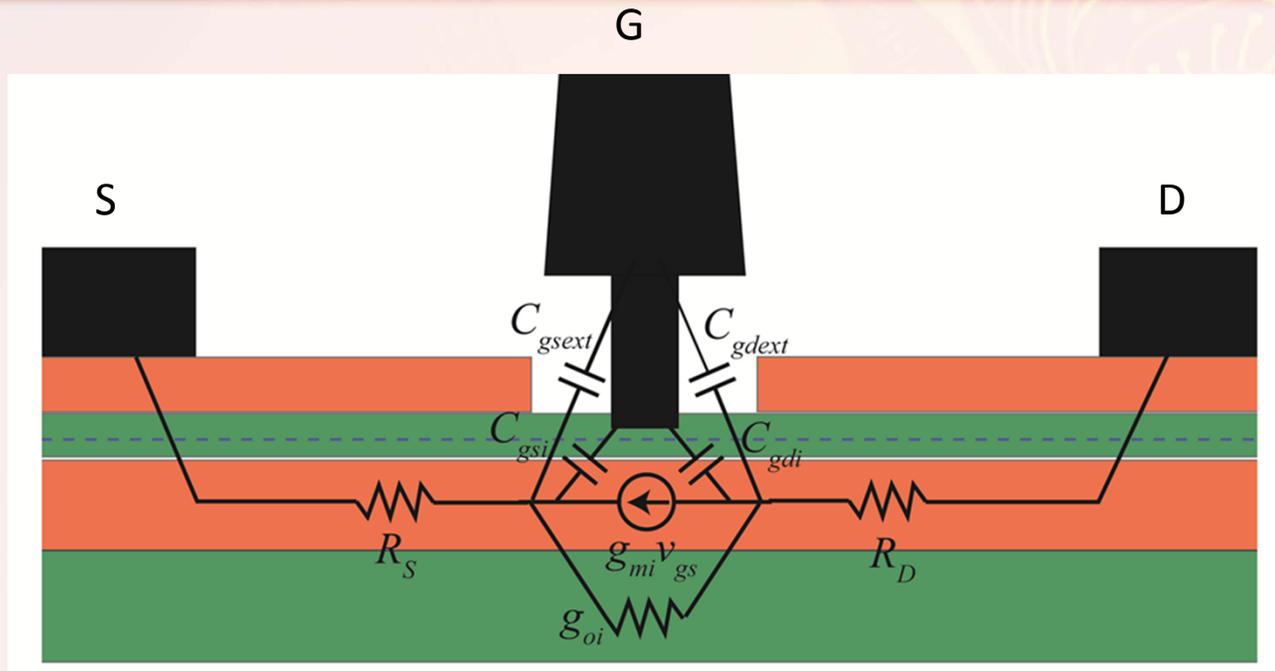
f_t analysis



- First-order f_T expression for HEMT:

$$f_T = \frac{1}{2\pi} \frac{g_{mi}}{C_{gs} + C_{gd} + g_{mi}(R_S + R_D) \left[C_{gd} + (C_{gs} + C_{gd}) \frac{g_{oi}}{g_{mi}} \right]}$$

Break out extrinsic capacitances



- Capacitance components:

$$C_{gs} = C_{gsi} + C_{gsext}$$

$$C_{gd} = C_{gdi} + C_{gdext}$$

Delay time analysis

- Delay time:

$$\tau = \frac{1}{2\pi f_T} = \tau_t + \tau_{ext} + \tau_{par}$$

- Components of delay time:

$$\tau_t = \frac{C_{gsi} + C_{gdi}}{g_{mi}} = \frac{L_g}{\langle v_e \rangle}$$

Intrinsic delay
(transit time)

Extrinsic
delay

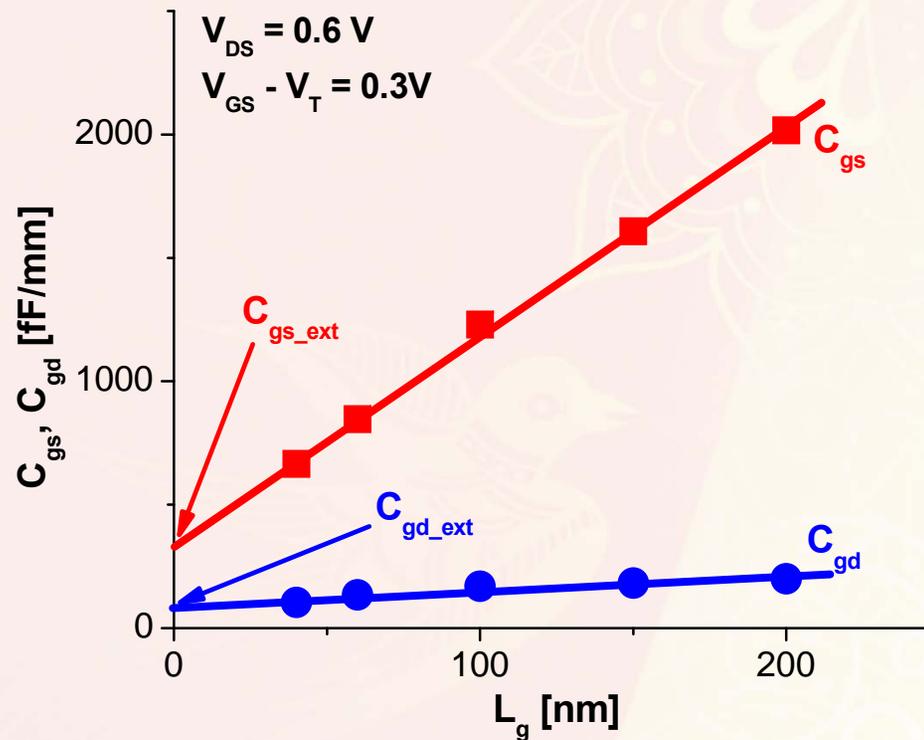
$$\tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}}$$

Parasitic
delay

$$\tau_{par} = (R_S + R_D) \left[C_{gd} + (C_{gs} + C_{gd}) \frac{g_{oi}}{g_{mi}} \right]$$

Extraction of parasitic capacitances

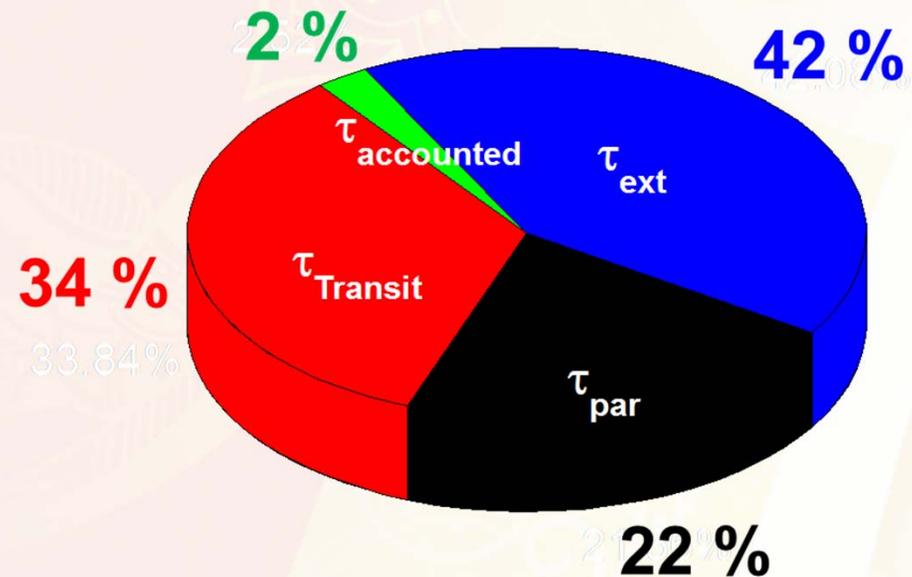
- Need devices with different L_g
- Bias them at same V_{GS} overdrive around peak f_T point
- Extract small-signal equivalent circuit models
- Study L_g scaling behavior of C_{gs} and C_{gd}



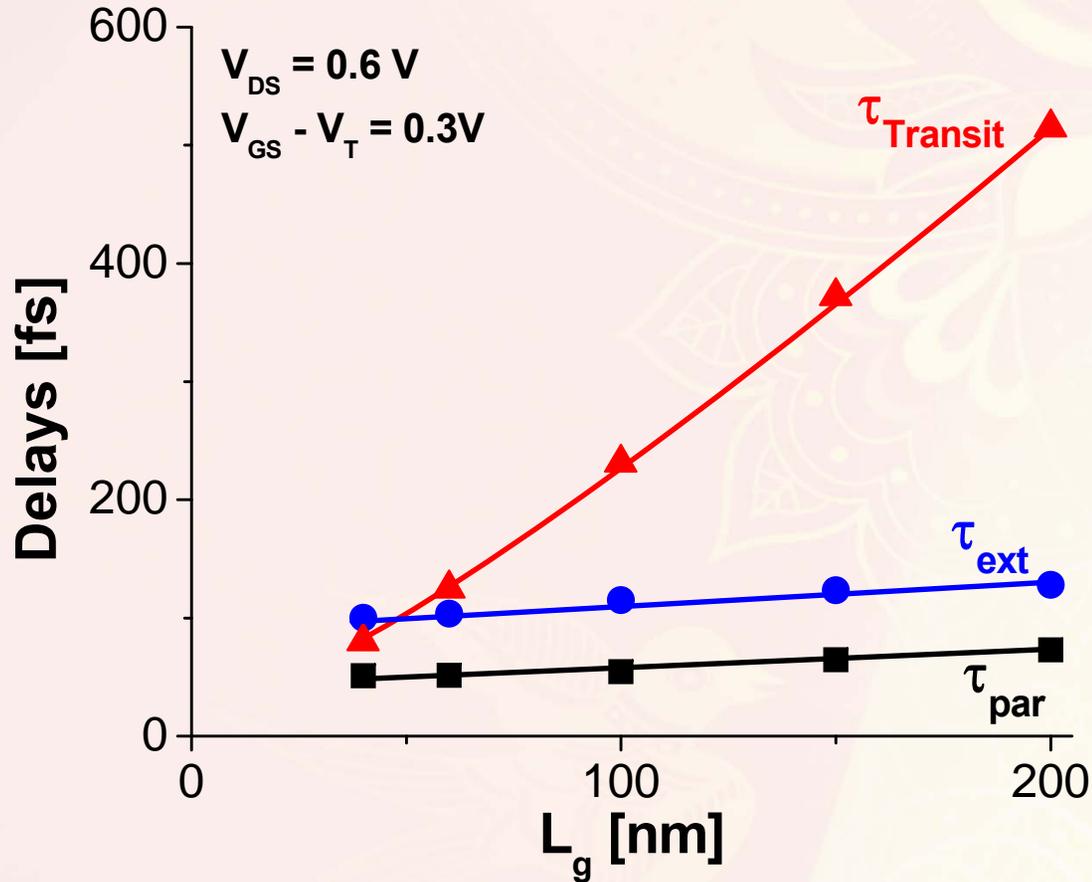
Delay components of $L_g = 40$ nm InGaAs HEMT

Delay time from f_T : ~ 231 fs

- Intrinsic delay: ~ 81 fs \leftarrow yields $\langle v_e \rangle = 5 \times 10^7$ cm/s
- Extrinsic delay: ~ 99 fs \leftarrow most significant
- Parasitic delay: ~ 50 fs
- Unaccounted: ~ 9 fs

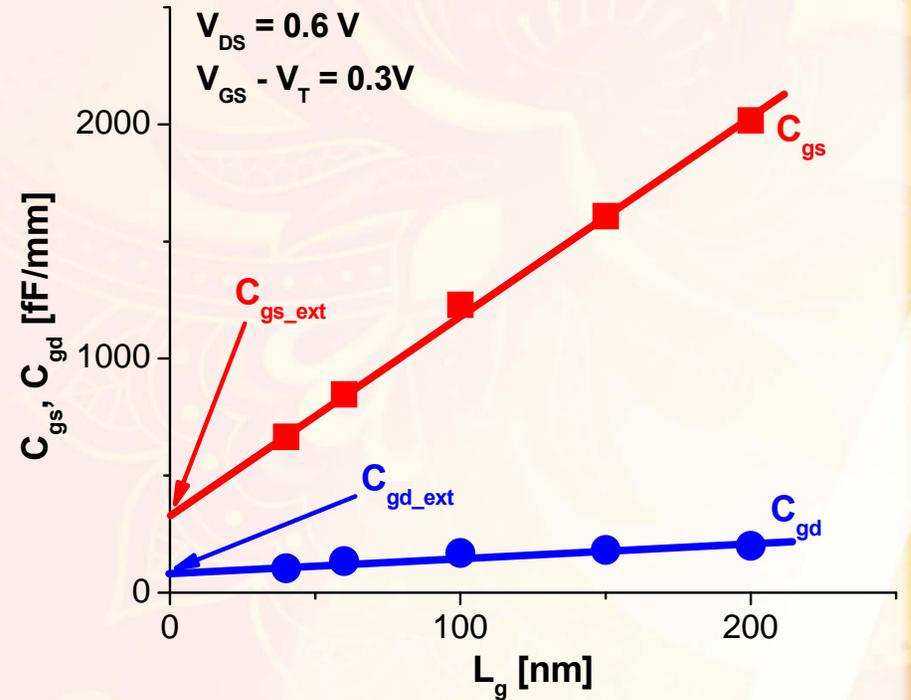
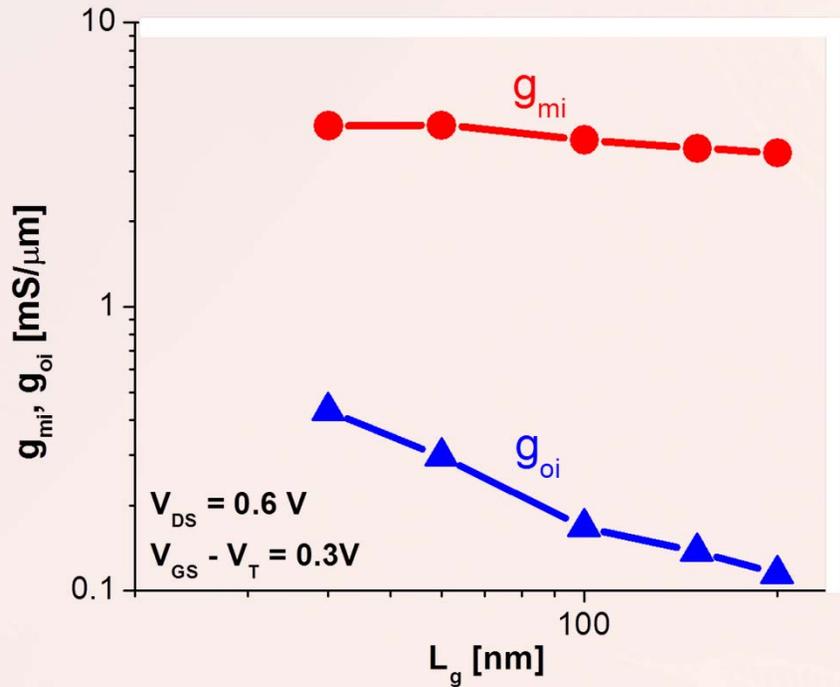


Scaling of delay components



τ_{ext} and τ_{par} do not scale, become dominant for $L_g < 50$ nm

Scaling of small-signal components



As $L_g \downarrow$:

do not scale

$$\tau_{ext} = \frac{C_{gs_ext} + C_{gd_ext}}{g_{mi}}$$

do not scale

$$\tau_{par} = (R_S + R_D) \left[C_{gd} + (C_{gs} + C_{gd}) \frac{g_{oi}}{g_{mi}} \right]$$

3. The path to THz operation

- Intrinsic delay ↓ → L_g ↓

- Extrinsic delay ↓:

$$\tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}}$$

→ C_{gsext}, C_{gdext} ↓ → gate engineering

→ g_{mi} ↑ → harmonious scaling

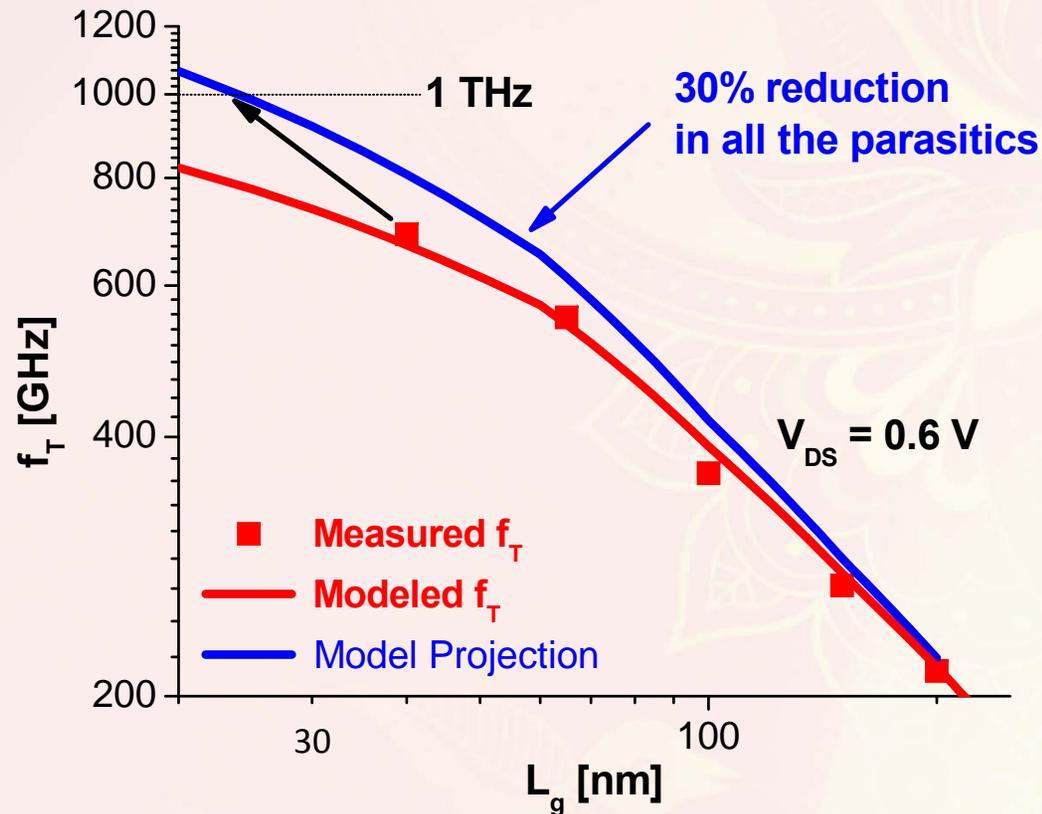
- Parasitic delay ↓:

$$\tau_{par} = (R_S + R_D) \left[C_{gd} + (C_{gs} + C_{gd}) \frac{g_{oi}}{g_{mi}} \right]$$

→ $R_S + R_D$ ↓ → S/D engineering

→ g_{oi}/g_{mi} ↓ → harmonious scaling

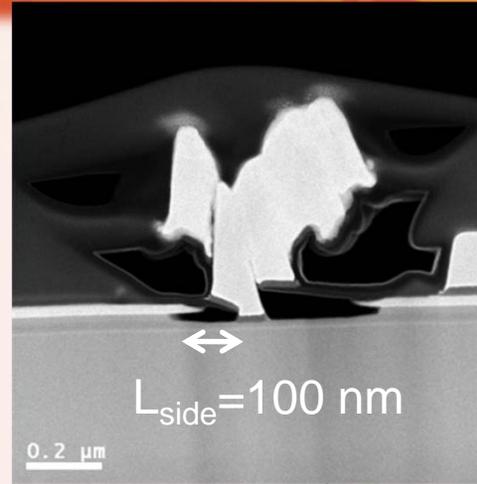
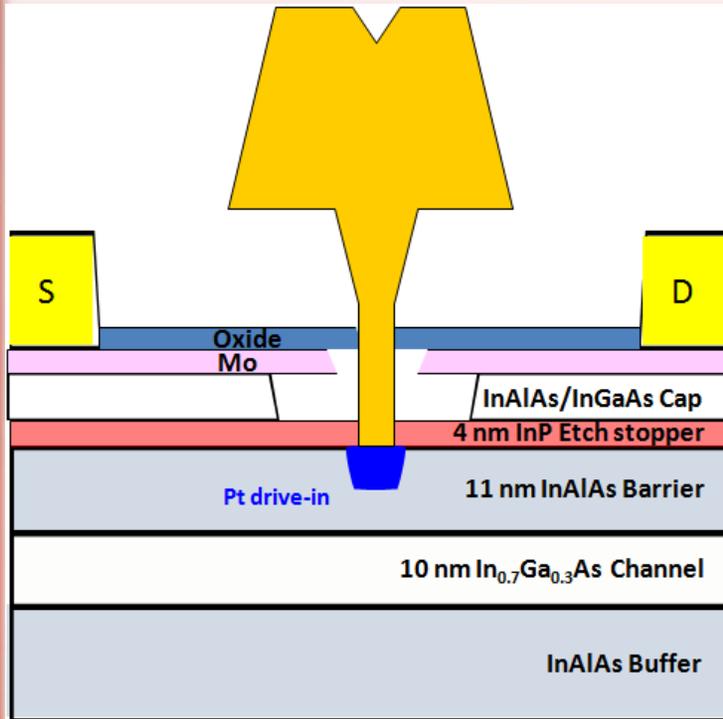
How to reach $f_t = 1$ THz?



$f_T = 1$ THz feasible by:

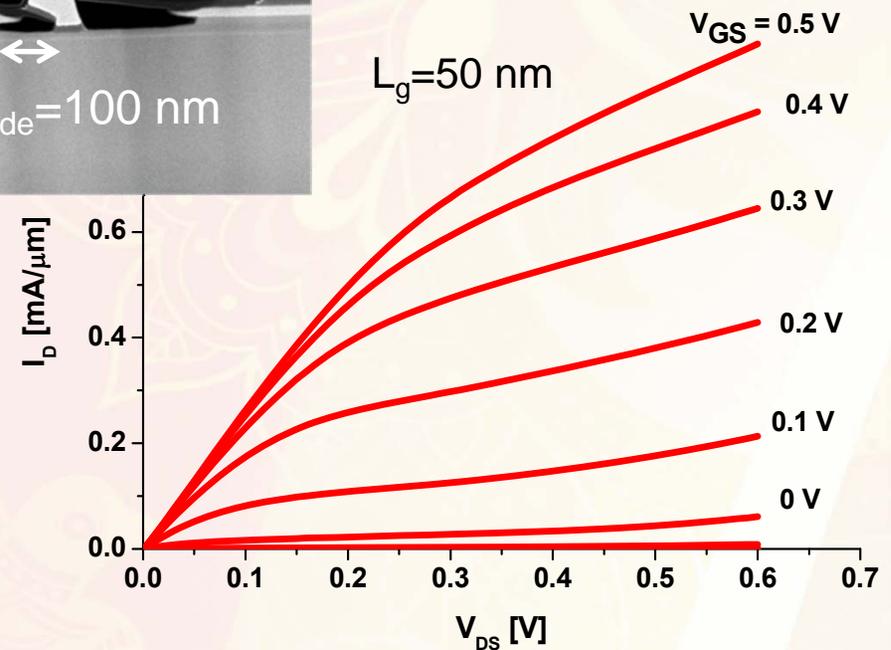
- scaling to $L_g \approx 25$ nm
- ~30% parasitic reduction

Approach to $R_S + R_D \downarrow$: self-aligned process



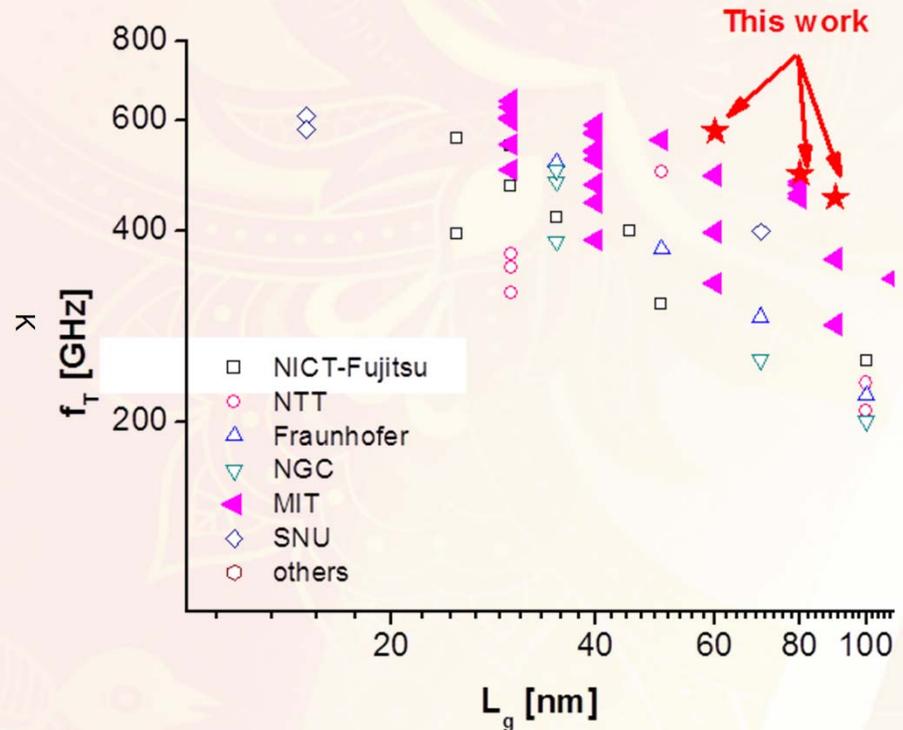
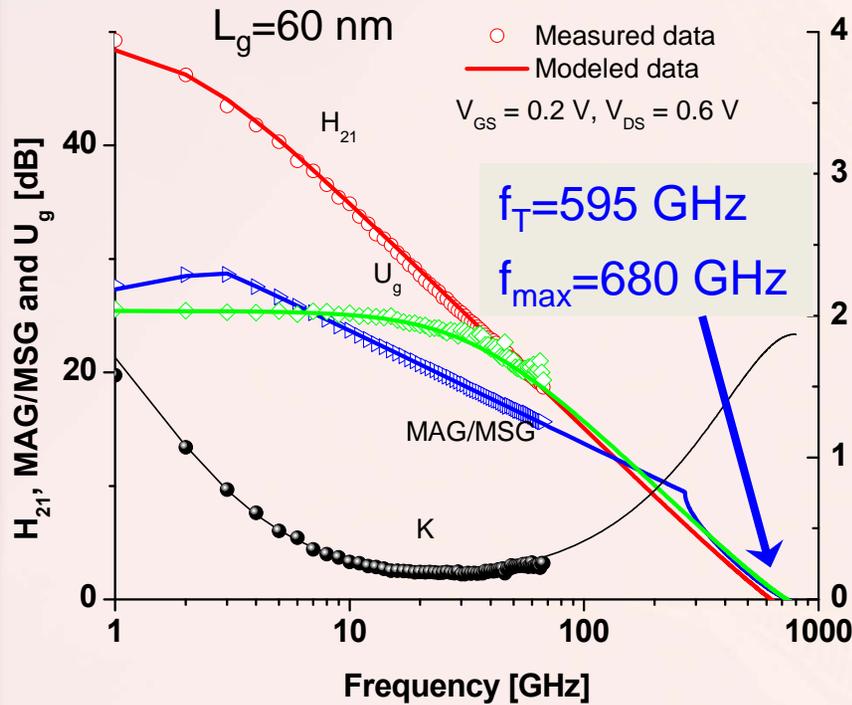
Kim, IEDM 2010

Waldron, TED 2010



- Dry-etched Mo contacts: $R_c = 7 \Omega \cdot \mu\text{m}$
- $L_g = 50 \text{ nm}$, $R_{ON} = 290 \Omega \cdot \mu\text{m}$, $g_{\text{mpk}} = 2.2 \text{ mS}/\mu\text{m}$ @ $V_{DS} = 0.5 \text{ V}$

$L_g = 60$ nm self-aligned $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ HEMT

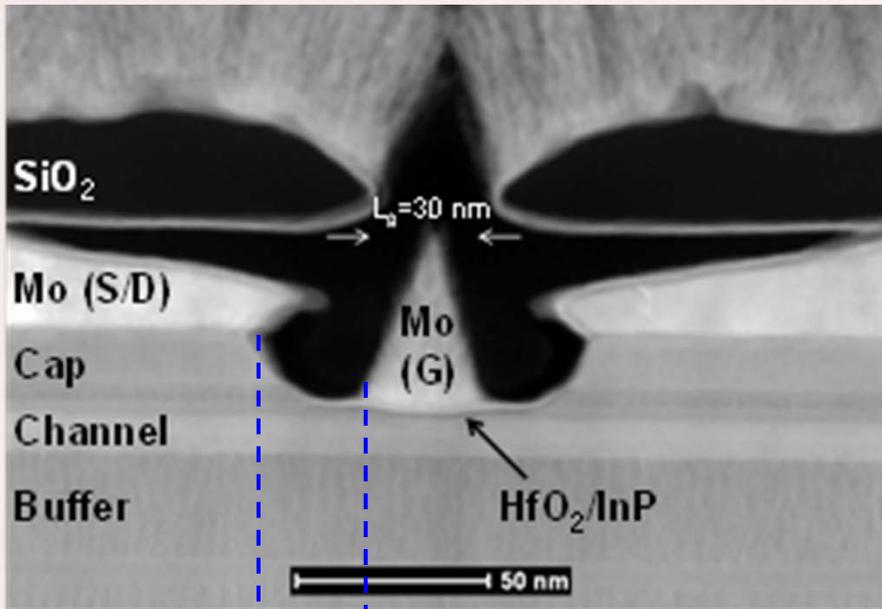


Kim, IEDM 2010

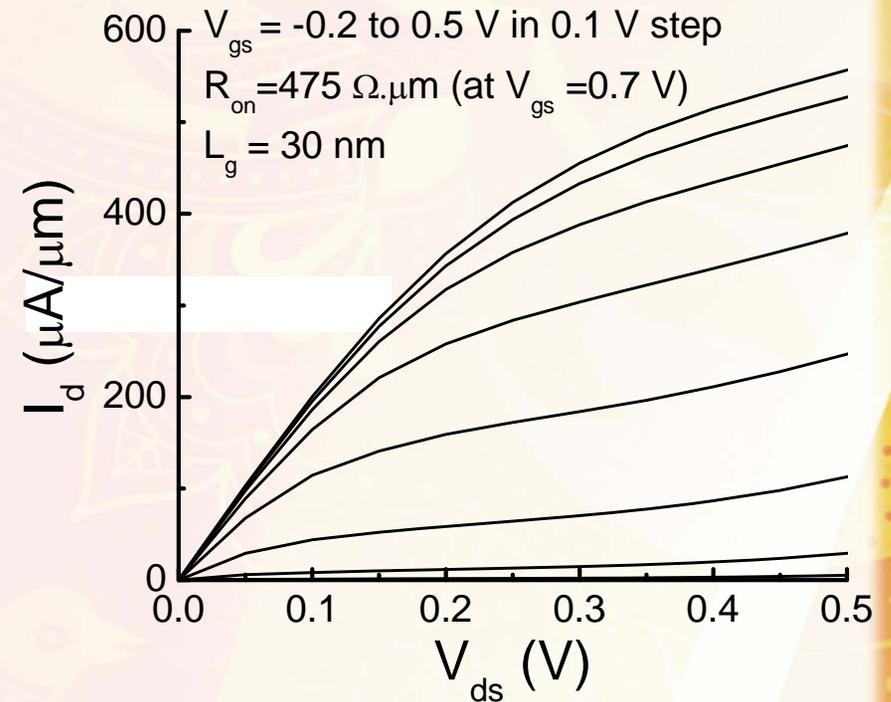
Highest f_T and f_{max} of any FET at $L_g \geq 60$ nm

$L_g = 30$ nm self-aligned InGaAs MOSFET with $L_{side} \sim 30$ nm

Lin, IEDM 2012



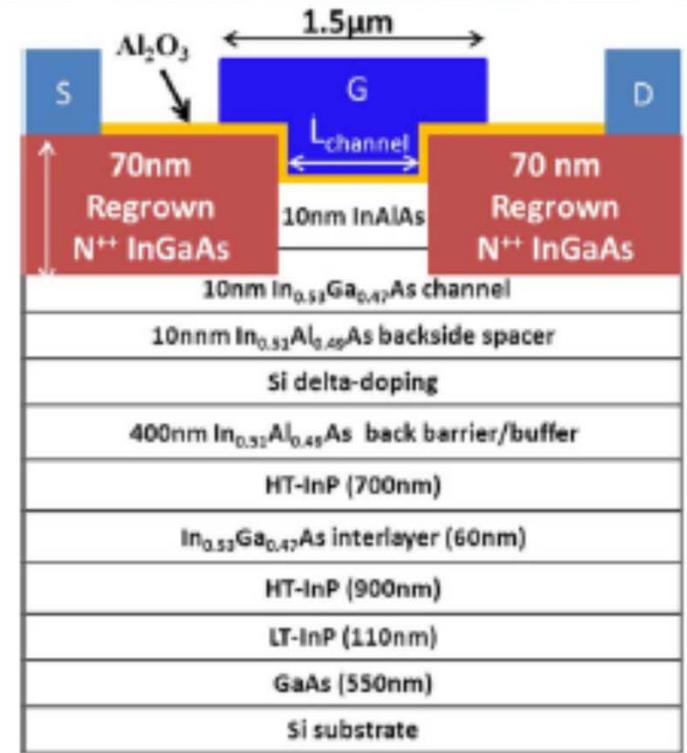
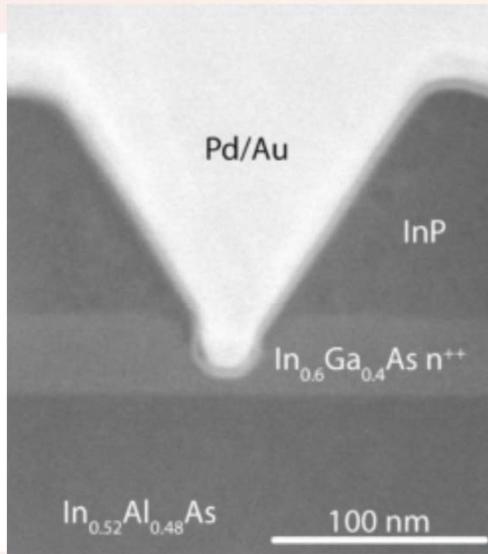
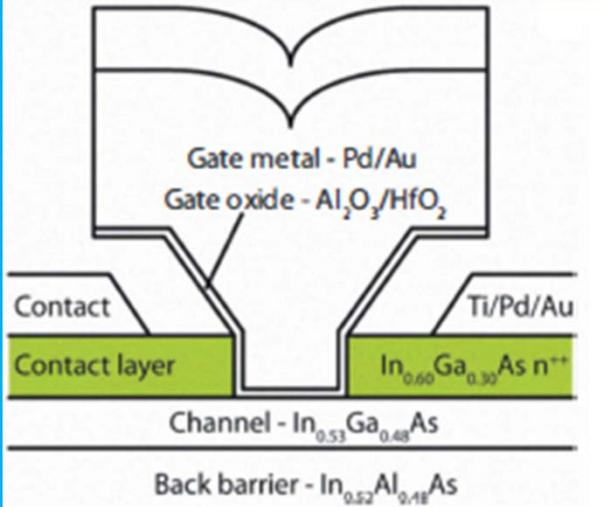
$L_{side} \sim 30$ nm



$$g_{mpk} = 1.4 \text{ mS}/\mu\text{m}$$

$R_{ON} = 475 \Omega \cdot \mu\text{m} \rightarrow$ access region design critical!

Regrown source and drain regions



$L_{ch} = 55$ nm InGaAs MOSFET:

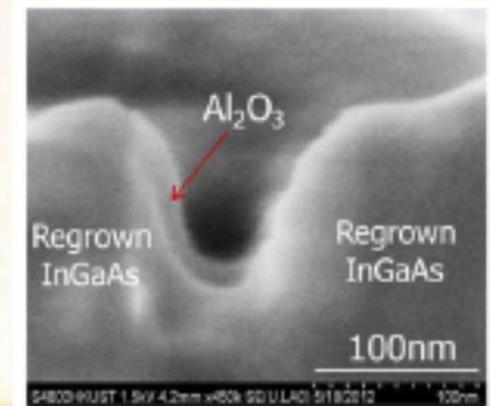
$R_{ON} = 199 \Omega \cdot \mu m$

Egard, IEDM 2011

$L_{ch} = 30$ nm InGaAs MOSFET:

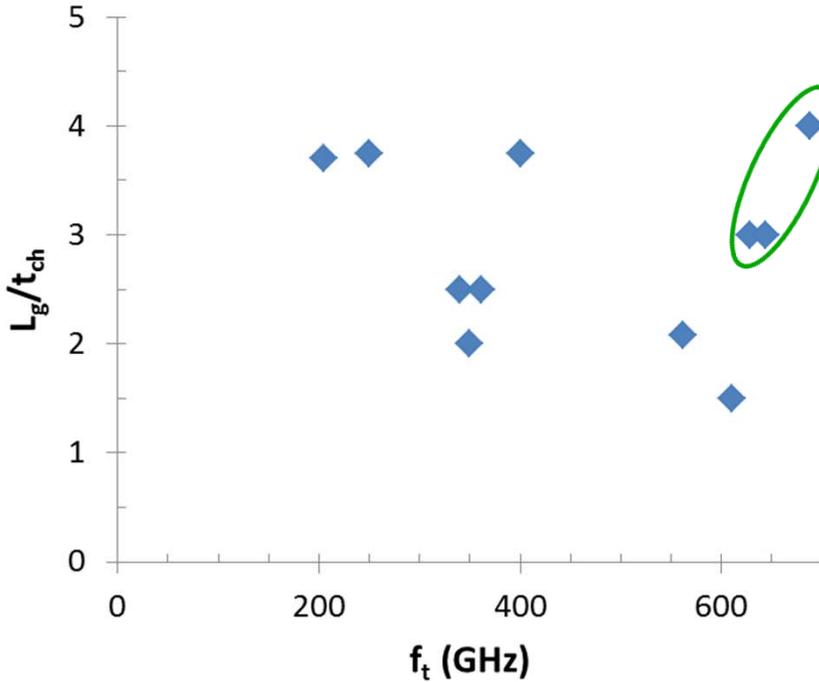
$R_{ON} = 133 \Omega \cdot \mu m$

Zhou, EDL 2012

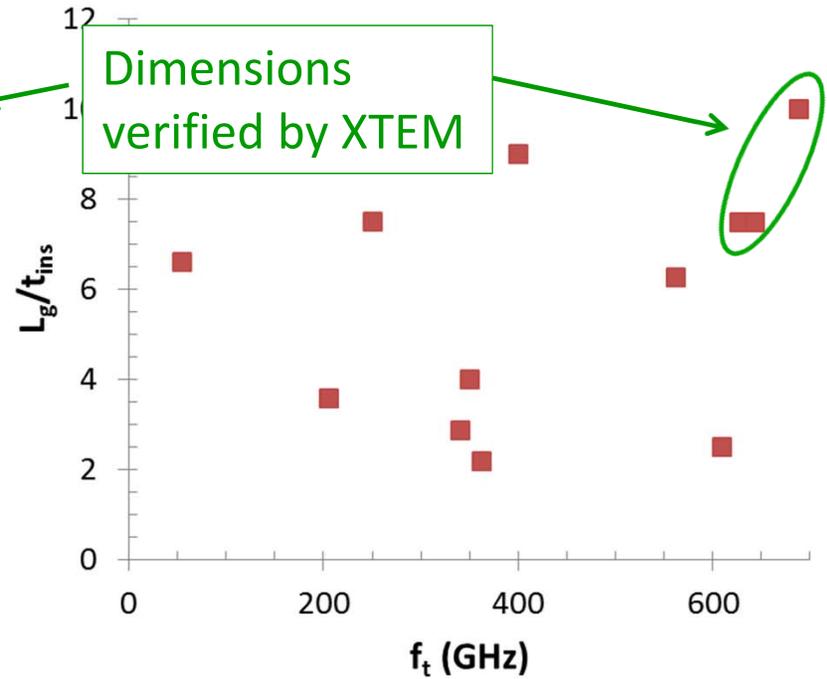


Harmonious scaling: aspect ratio of record f_t devices

Channel Aspect Ratio: L_g/t_{ch}



Insulator Aspect Ratio: L_g/t_{ins}



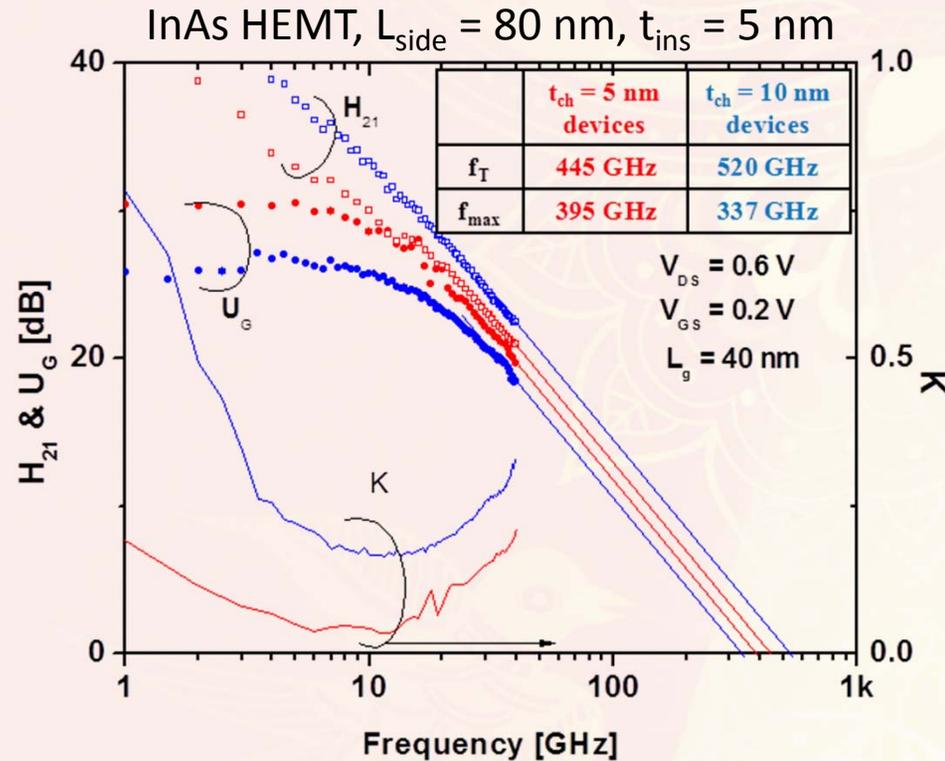
- Channel AR: 3 ~ 4
- Insulator AR: 7 ~ 10

For $L_g=25$ nm:
 $\rightarrow t_{ch} \sim 7$ nm, $t_{ins} \sim 3$ nm

Issues in channel scaling

Deep channel thickness scaling degrades performance:

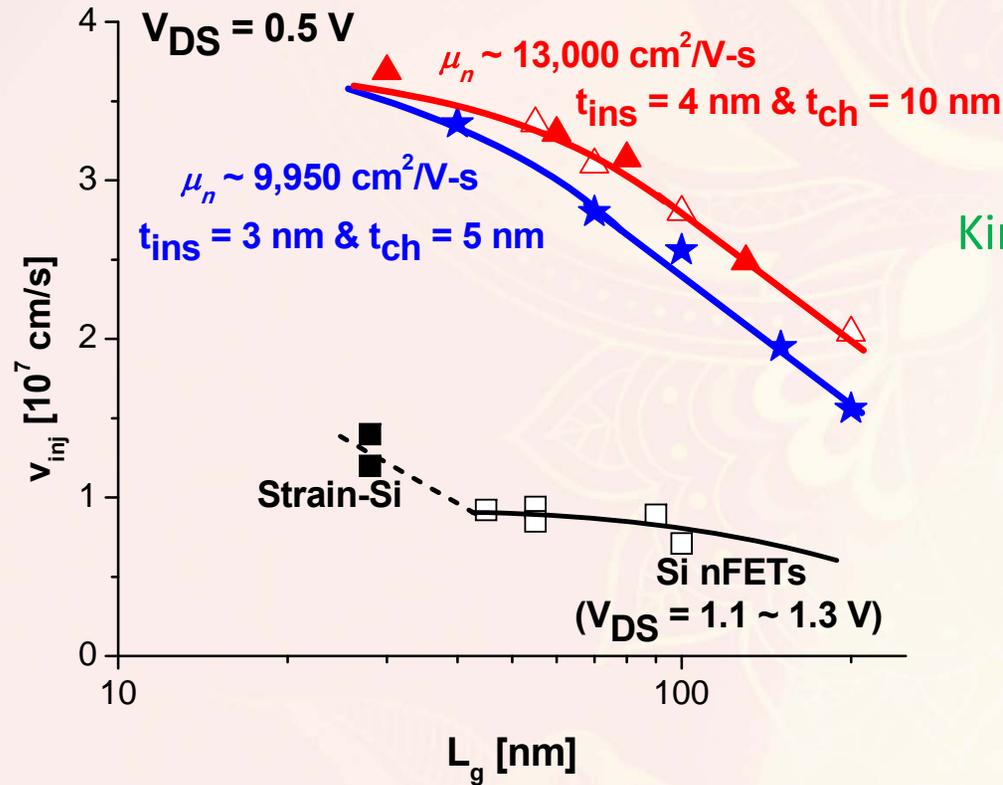
→ $R_s \uparrow \rightarrow f_T \downarrow$



Noticeable mobility degradation: $t_{\text{ch}} = 10 \text{ nm} \rightarrow \mu_e = 13,500 \text{ cm}^2/\text{V}\cdot\text{s}$

$t_{\text{ch}} = 5 \text{ nm} \rightarrow \mu_e = 9,950 \text{ cm}^2/\text{V}\cdot\text{s}$

V_{inj} - impact of channel thickness



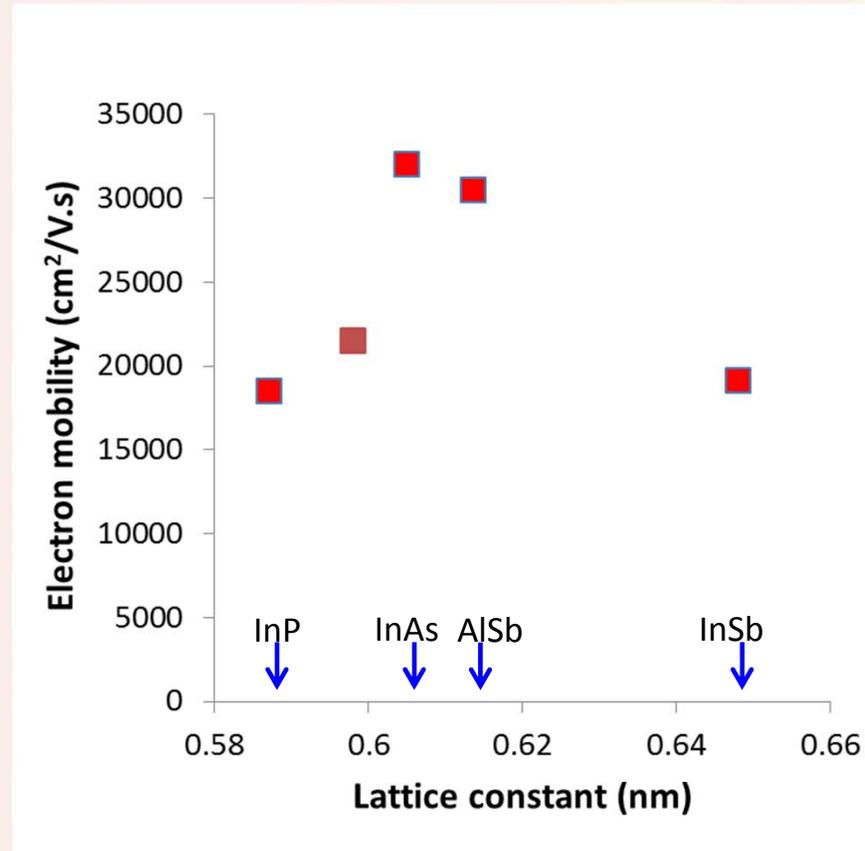
Kim, IEDM 2009

In thin-channel devices:

- Long L_g : v_{inj} decreases right along with μ_e (~23%)
- Short L_g : v_{inj} relatively unaffected
 → consistent with near ballistic transport

Channel transport enhancement through strain engineering

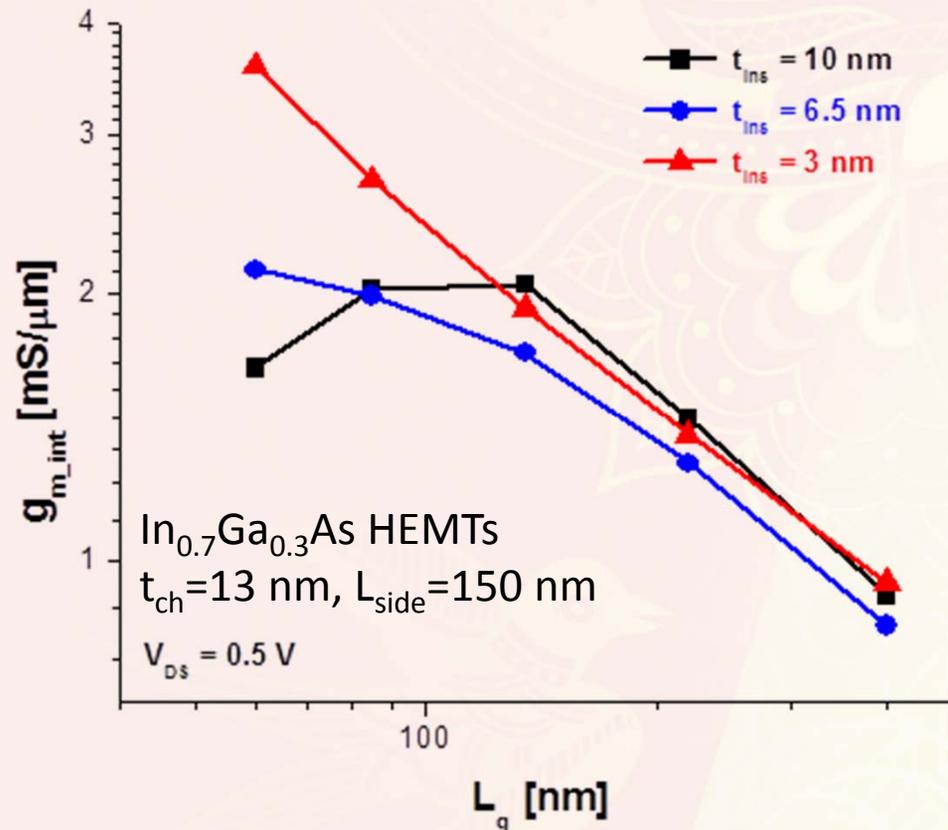
InAs 300 K quantum-well mobility vs. lattice constant:



Independent control of channel strain and composition:
 → new possibilities for channel design

Issues in barrier scaling

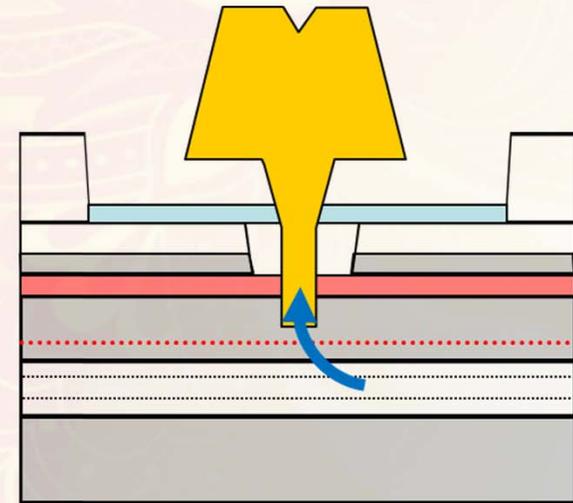
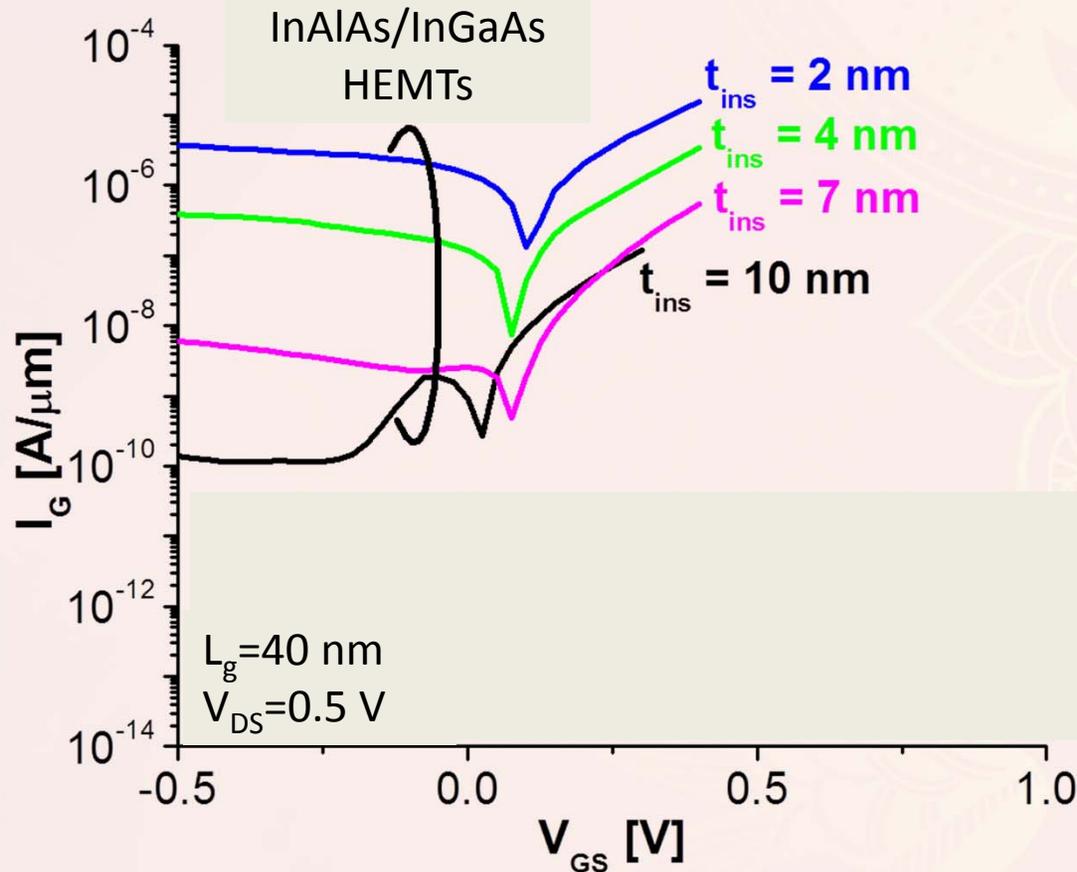
Want to scale L_g without degrading g_m or g_o



Kim, TED 2008

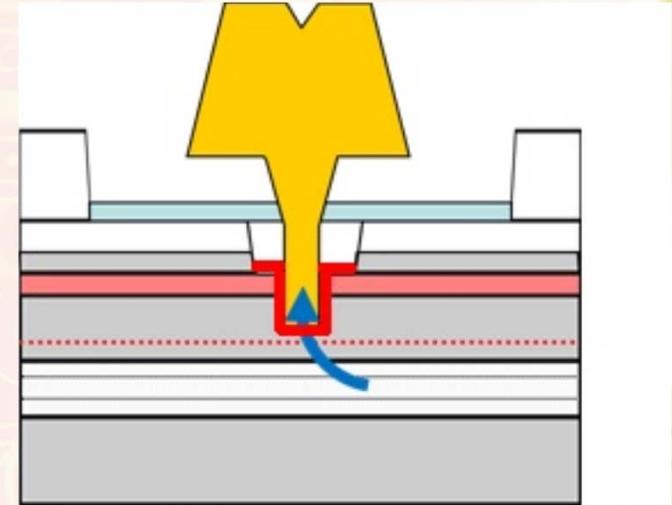
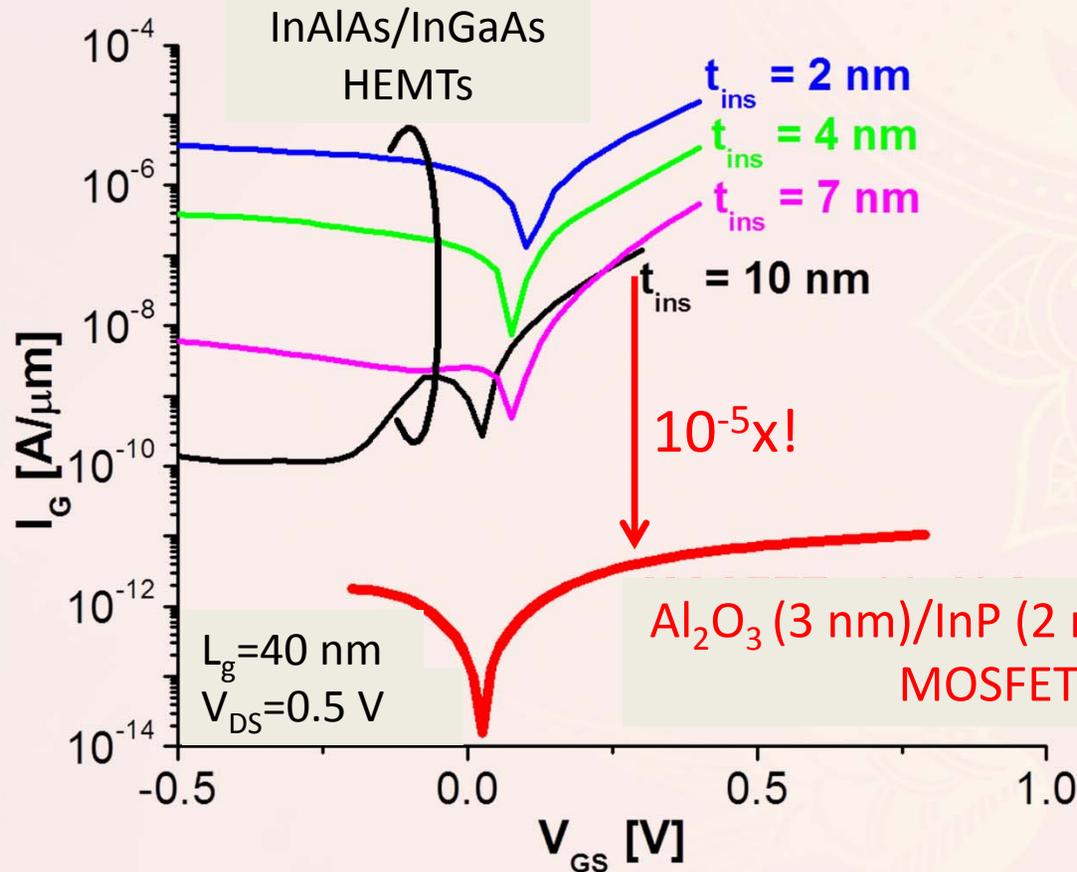
For harmonious scaling: as $L_g \downarrow \rightarrow t_{ins} \downarrow$

Limit to HEMT barrier scaling: gate leakage current



At $L_g = 40$ nm, modern HEMTs are at the limit of scaling!

Limit to HEMT barrier scaling: gate leakage current



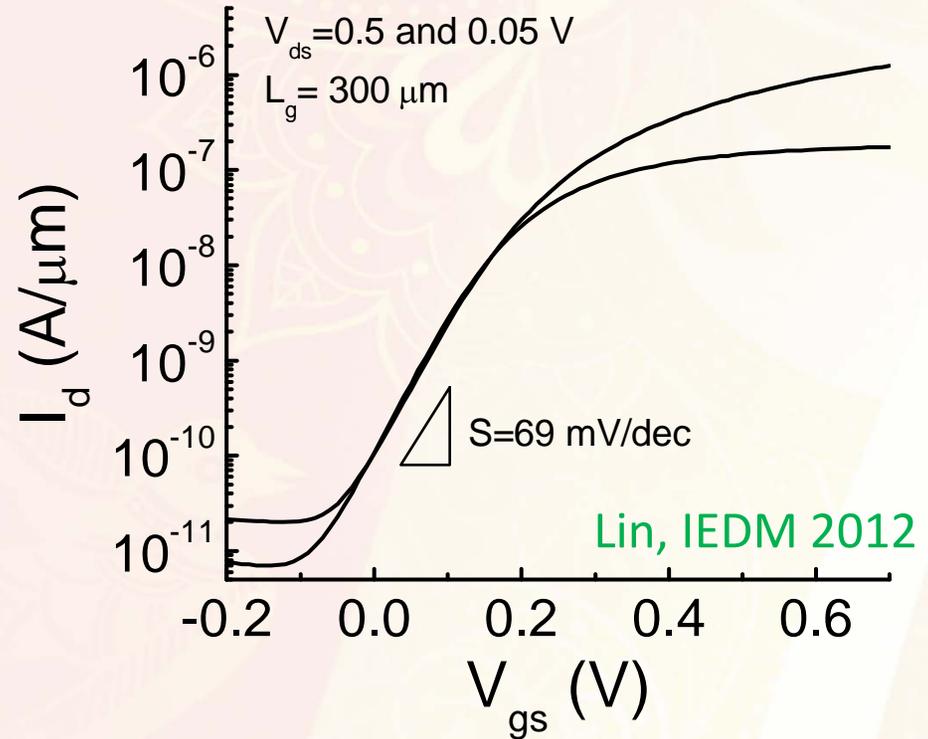
Need high-K gate dielectric: HEMT \rightarrow MOSFET!

III-V MOSFET: deep scaling possible

InP (1 nm) + Al₂O₃ (0.4 nm) + HfO₂ (2 nm) → EOT ~ 0.9 nm
 [vs. 4 nm InAlAs → EOT = 1.3 nm]
 → should bring us to L_g=20 nm

↑
 Equivalent oxide thickness

Long-channel
 In_{0.53}Ga_{0.47}As MOSFET
 μ_e ≈ 2700 cm²/V.s

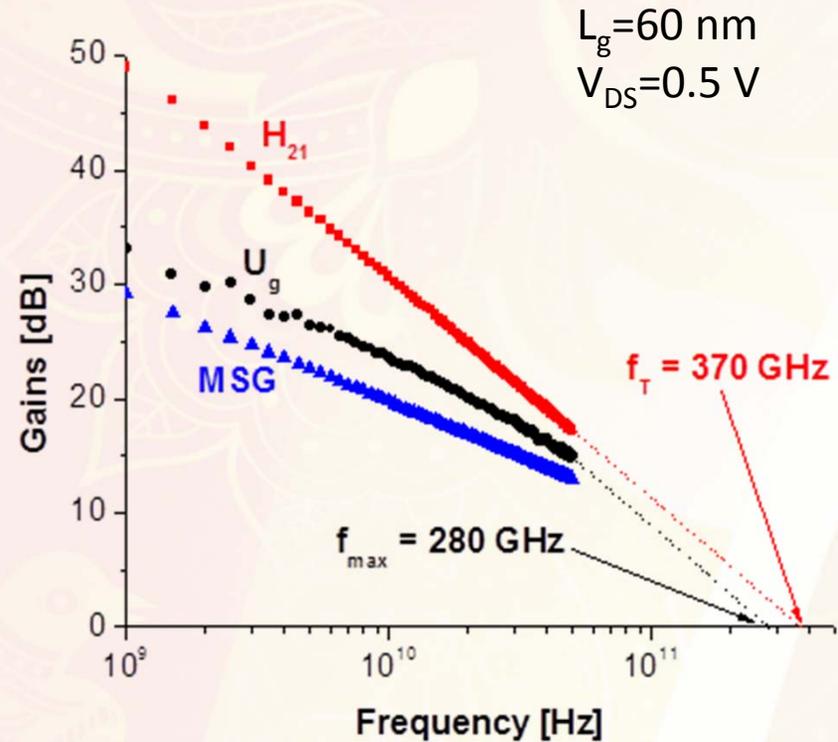
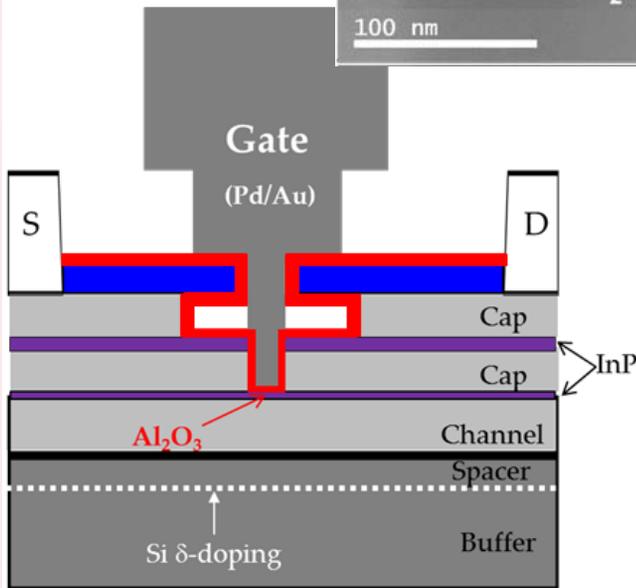
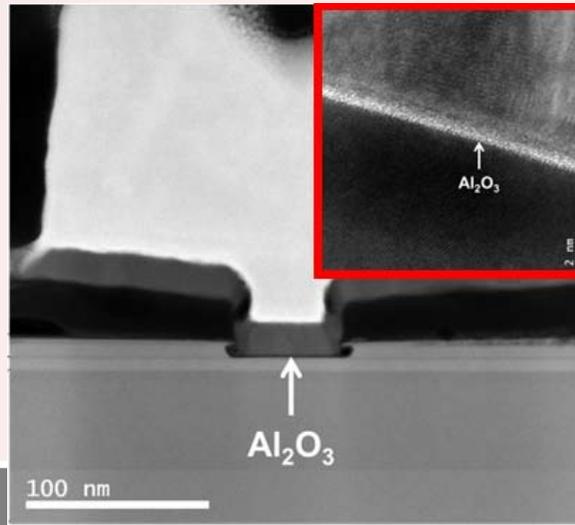


S=69 mV/dec → Low D_{it} at MOS interface demonstrated

High-frequency InGaAs MOSFETs

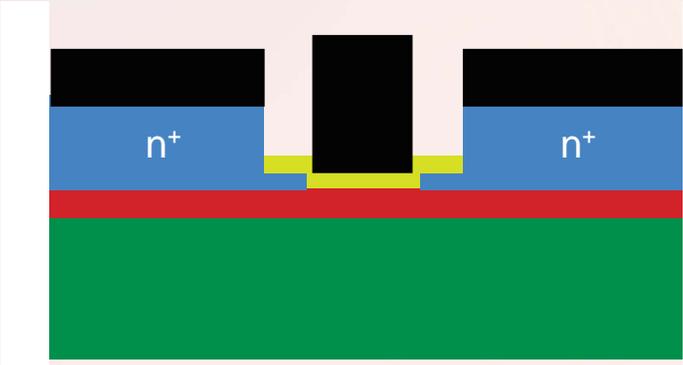
$L_g = 60$ nm InGaAs MOSFET with $L_{side} \sim 5$ nm, EOT = 1.2 nm

Kim, APL 2012

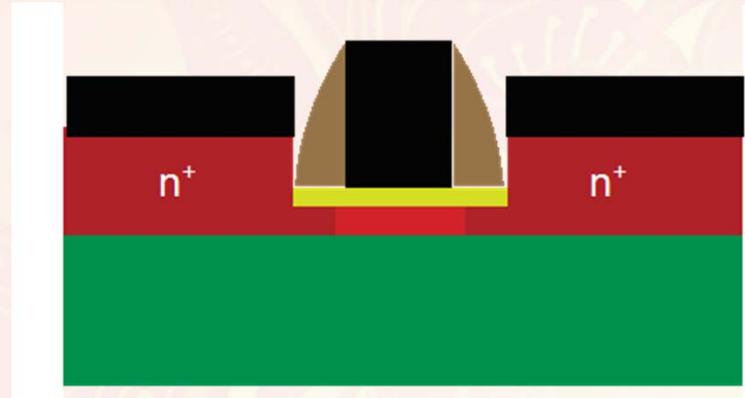


$f_t = 370$ GHz, $R_{ON} = 220 \Omega \cdot \mu\text{m}$,
 $g_m = 2.0$ mS/ μm , $S = 110$ mV/dec

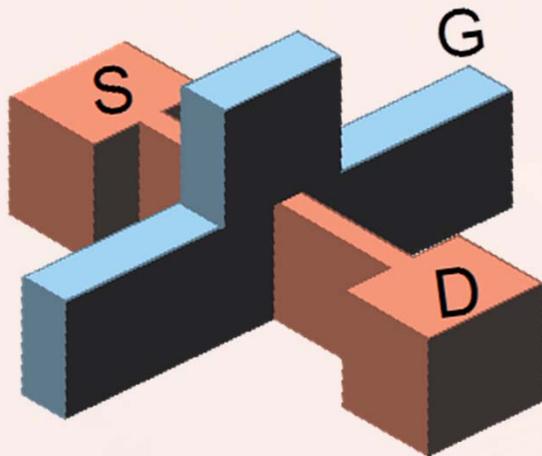
THz MOSFETs: possible designs



Etched S/D QW-MOSFET



Regrown S/D QW-MOSFET



FinFET



Gate-all-around nanowire FET

Conclusions

- THz III-V FETs just around the corner
 - need to reduce parasitics
 - need to scale harmoniously
- Exploding interest on III-V CMOS: huge opportunity for THz III-V electronics!
 - fast technology progress
 - new processes and tools
 - fundamental research on transport, interface, etc.
 - Si as substrate for THz electronics