III-Vs for CMOS Beyond Silicon

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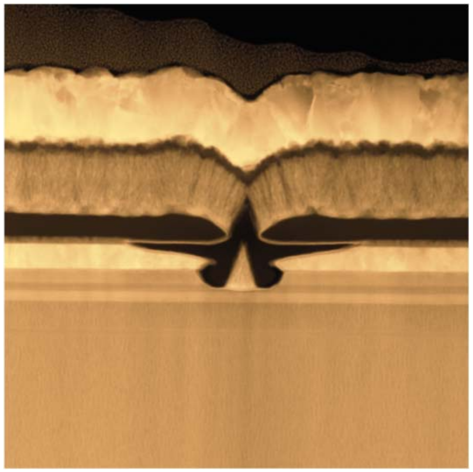
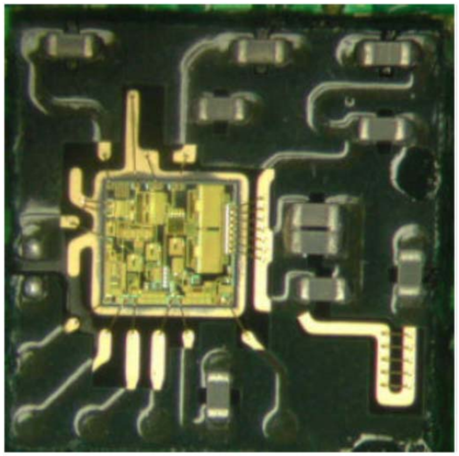


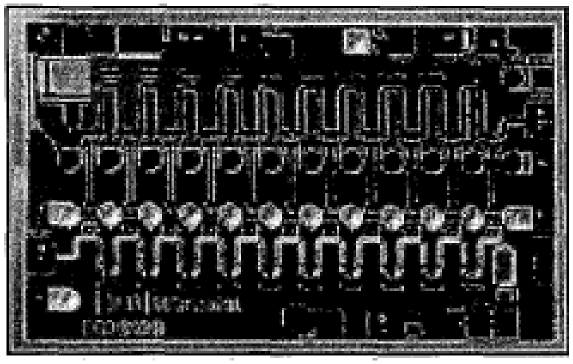
III-V HEMT Electronics Today

TriQuint and Skyworks Power iPhone 5



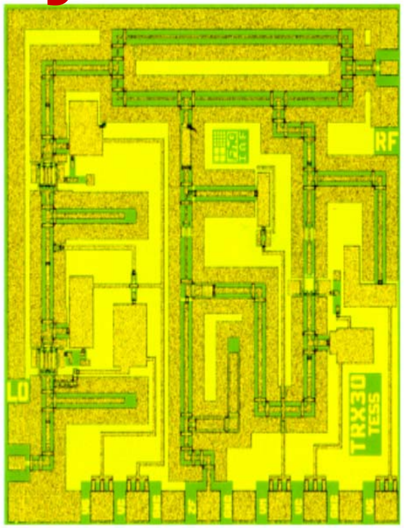
UMTS-LTE PA module

Chow, MTT-S 2008



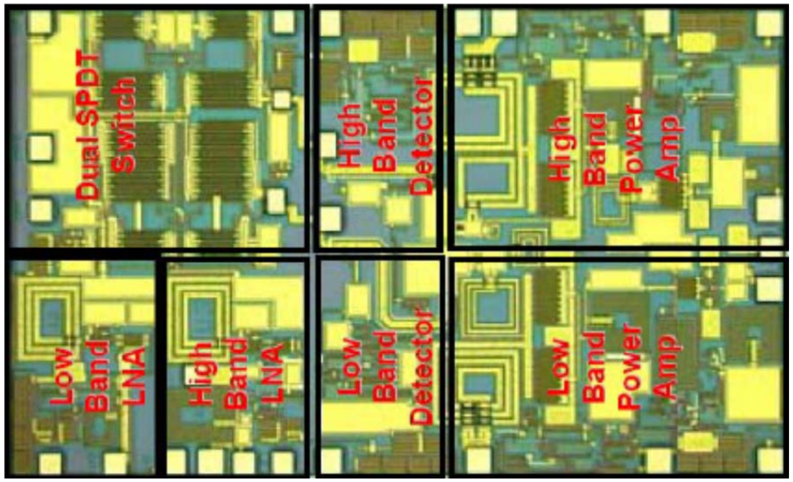
40 Gb/s modulator driver

Carroll, MTT-S 2002



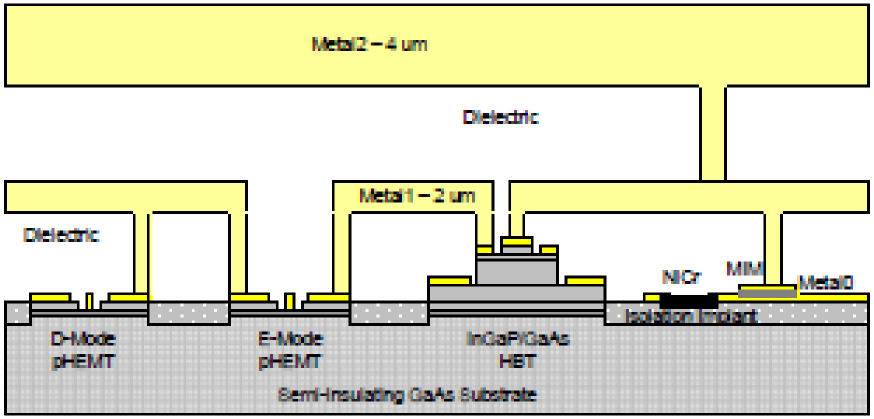
77 GHz transceiver

Tessmann, GaAs IC 1999



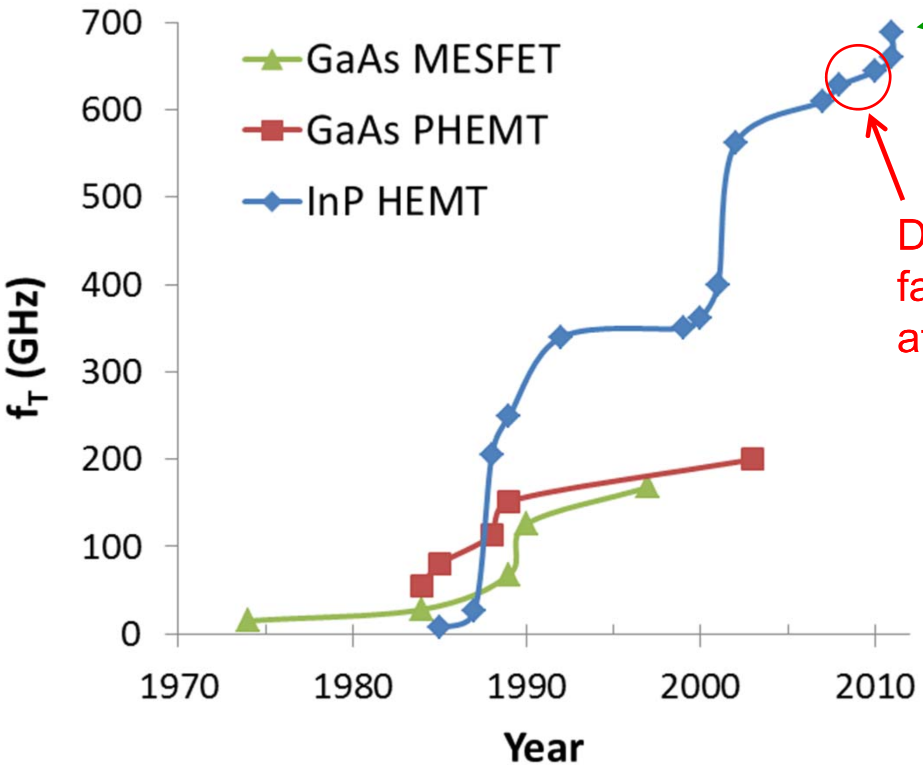
Single-chip WLAN MMIC, Morkner, RFIC 2007

Bipolar/E-D PHEMT process



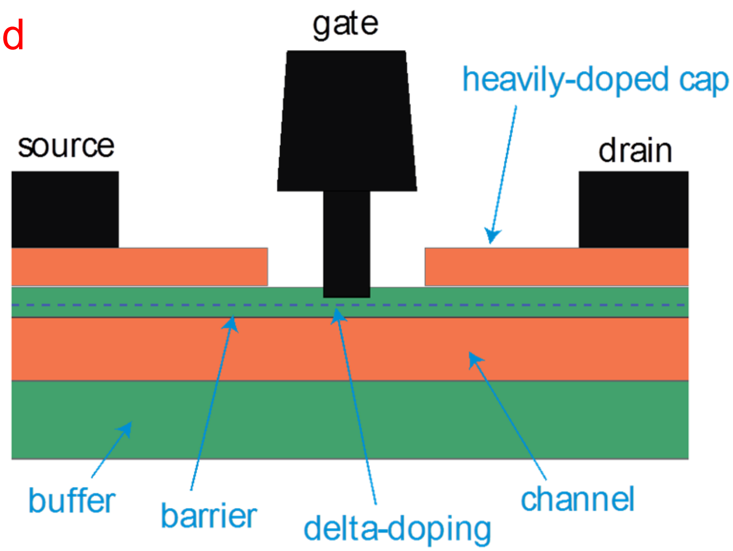
Henderson, Mantech 2007

III-V HEMT: record f_T vs. time



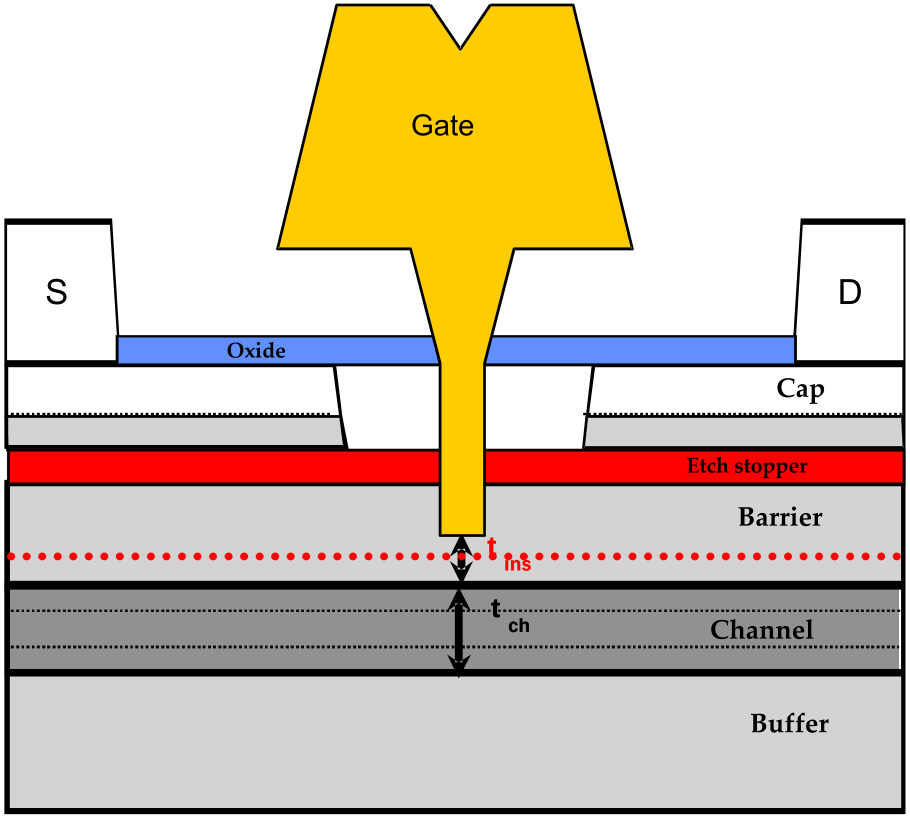
Current record:
f_T=688 GHz
f_{max}=800 GHz
Kim IEDM 2011
(Teledyne/MIT)

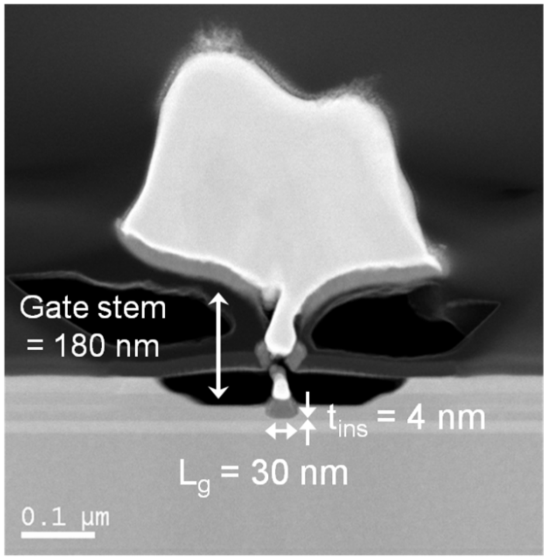
Devices fabricated at MIT



- For >20 years, record f_T obtained on InGaAs-channel HEMTs
- InGaAs-channel HEMTs offer record balanced f_T and f_{max}

InAlAs/InGaAs HEMTs at MIT

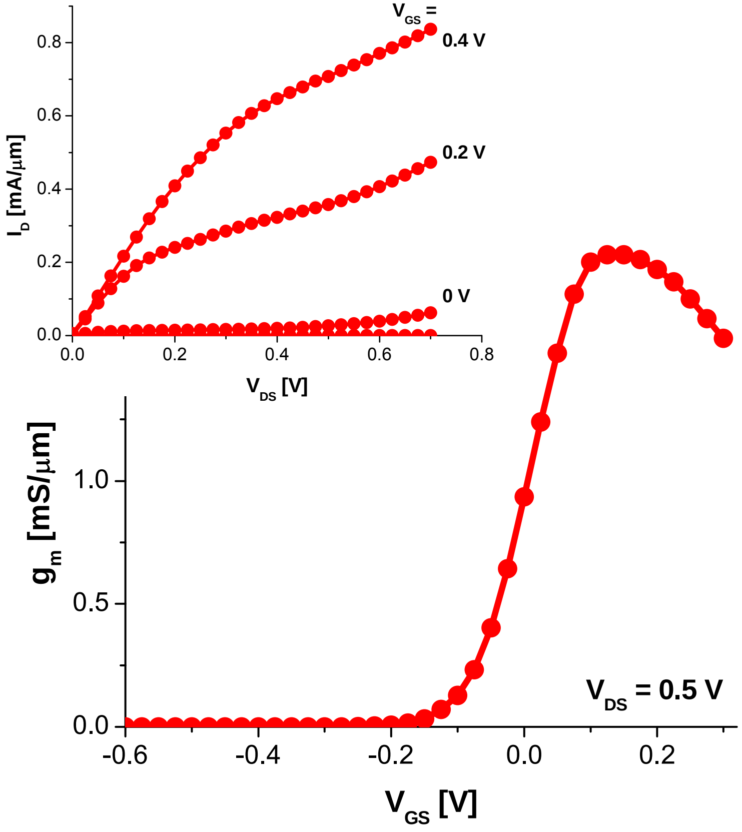




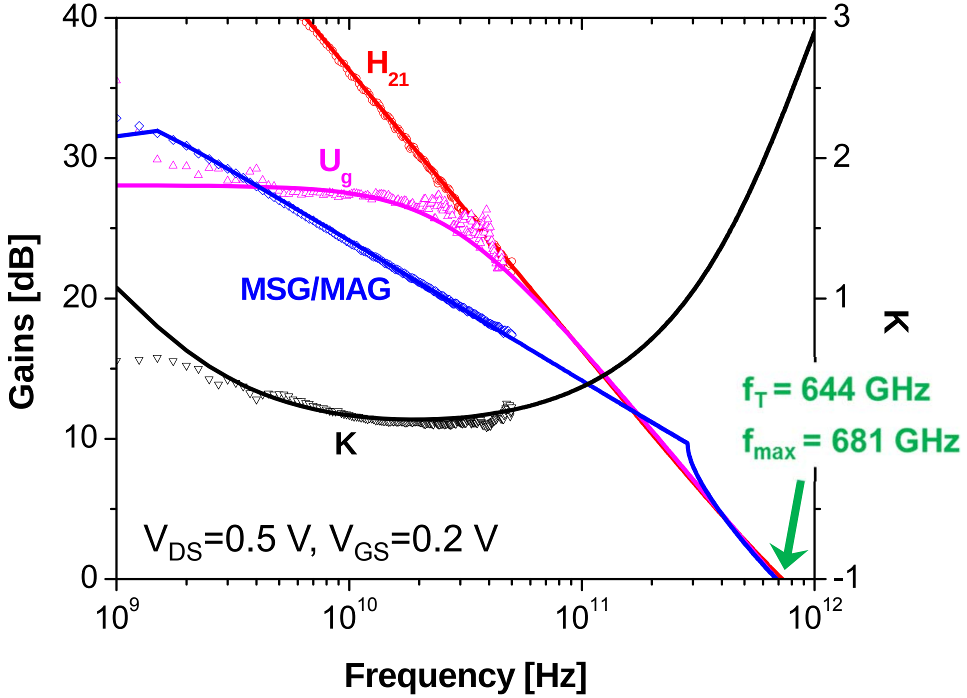
- QW channel (t_{ch} = 10 nm):
  - InAs core
  - InGaAs cladding
- $\mu_{n,Hall}$ = 13,200 cm^2/V-sec
- InAlAs barrier (t_{ins} = 4 nm)
- L_g=30 nm

Kim, EDL 2010

L_g=30 nm InGaAs HEMT



Kim, EDL 2010

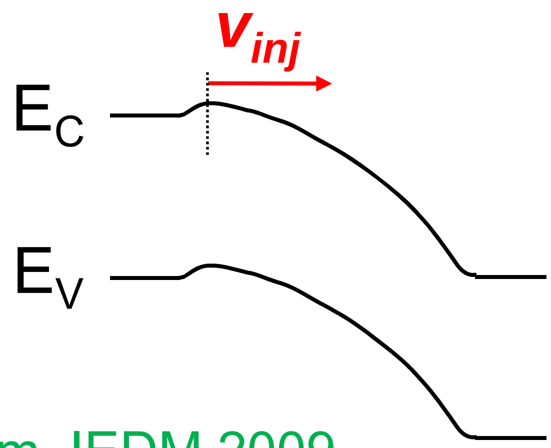


f_T = 644 GHz

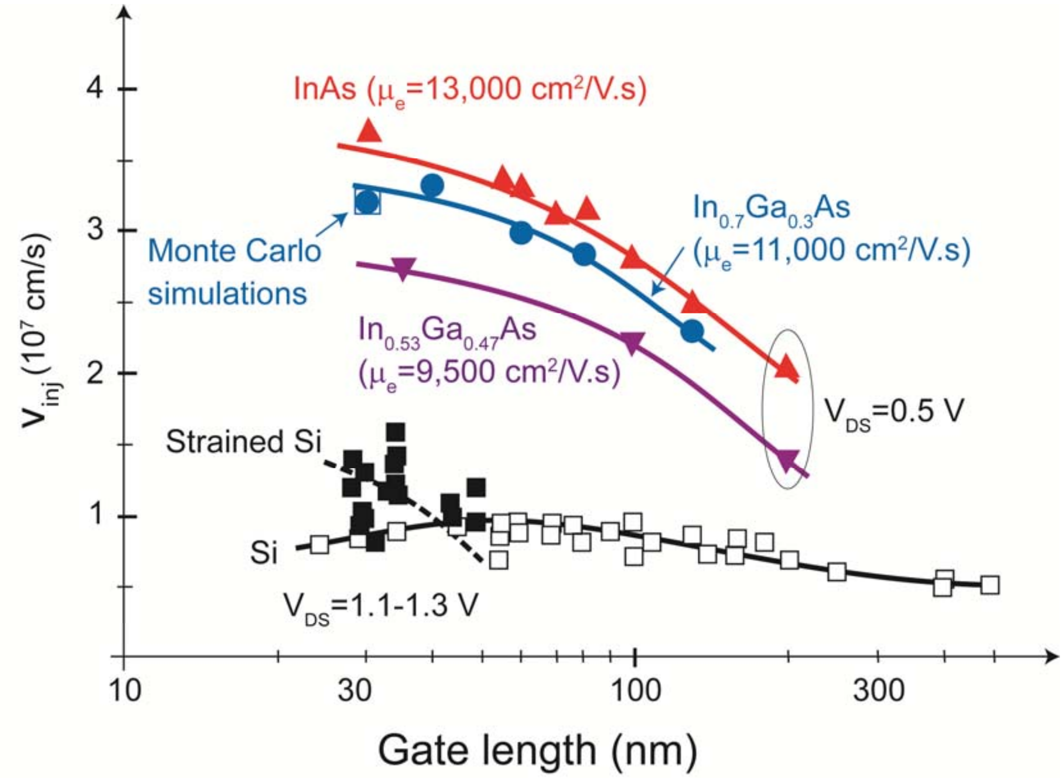
f_{max} = 681 GHz

- High transconductance: g_{mpk}= 1.9 mS/µm at V_{DD}=0.5 V
- First transistor of any kind with both f_T and f_{max} > 640 GHz (current record is f_T, f_{max}>688 GHz in Teledyne/MIT collaboration)

InGaAs Electron Injection Velocity



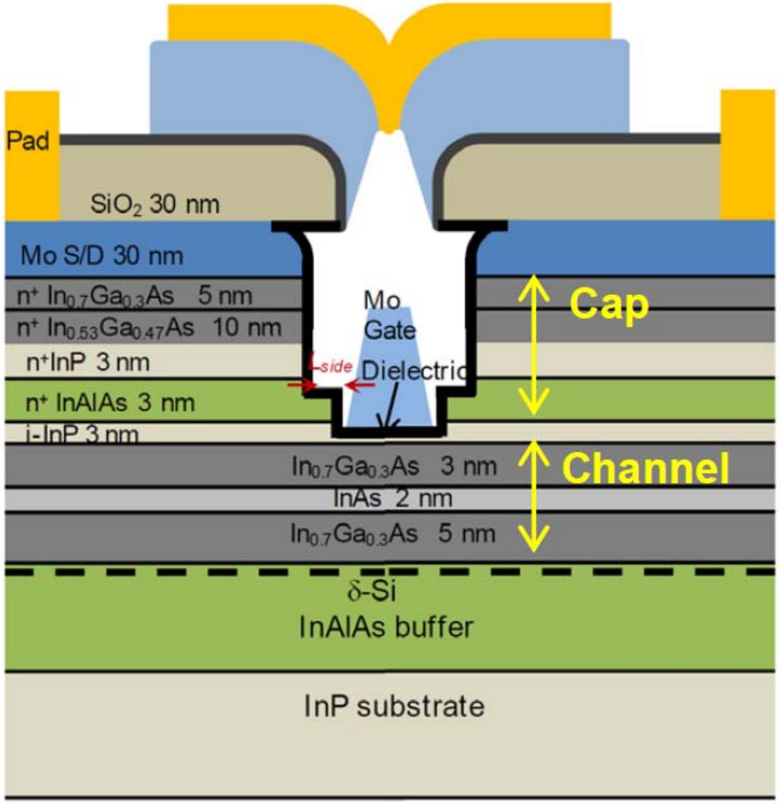
Kim, IEDM 2009
Liu, Springer 2010
Khakifirooz, TED 2008
del Alamo, Nature 2011

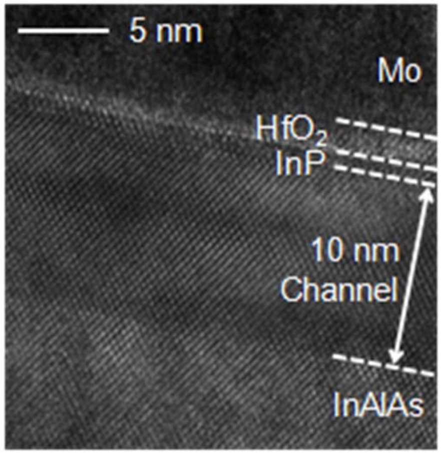


- v_{inj}(InGaAs) increases with InAs fraction in channel
- v_{inj}(InGaAs) > 2v_{inj}(Si) at less than half V_{DD}
- ~100% ballistic transport at L_g~30 nm

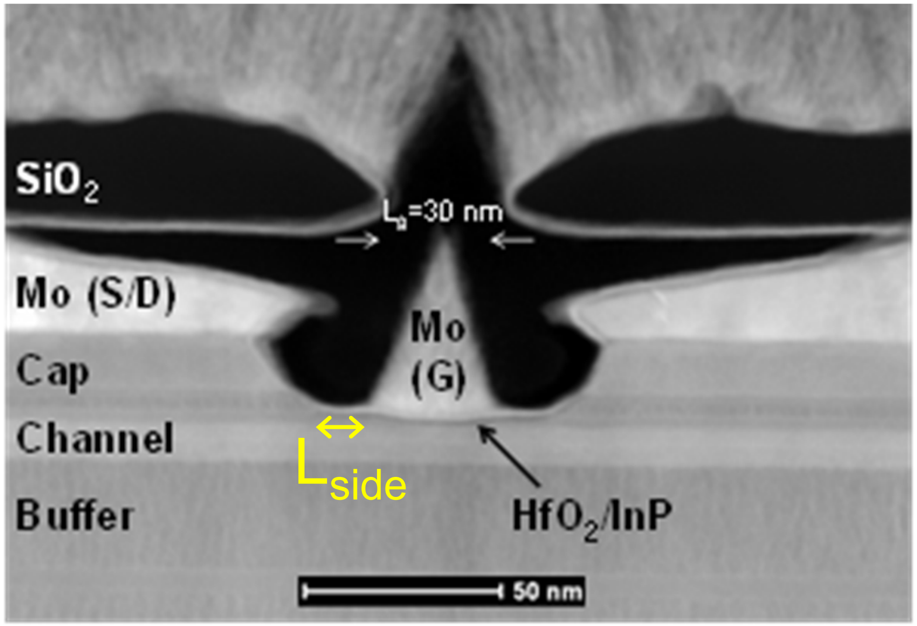
Self-Aligned InGaAs QW-MOSFETs

- Scaled barrier (InP: 1 nm + HfO_2: 2 nm) [EOT~0.8 nm]
- 10 nm thick channel with InAs core
- Tight S/D spacing (L_{side} =20~30 nm)
- Process designed to be compatible with Si fab

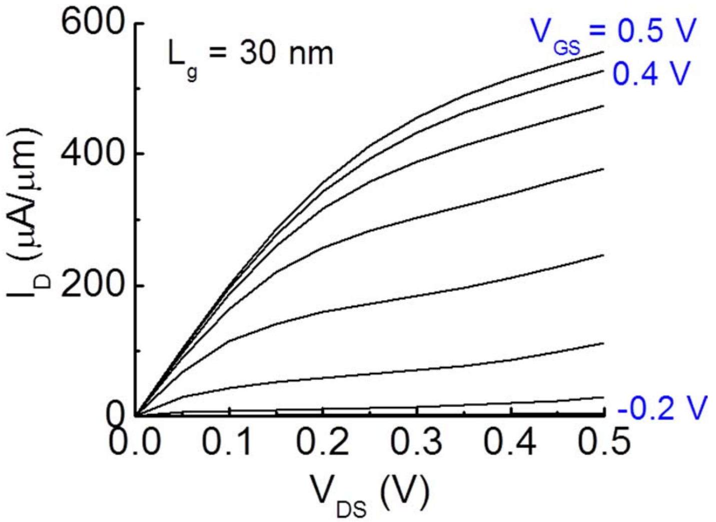


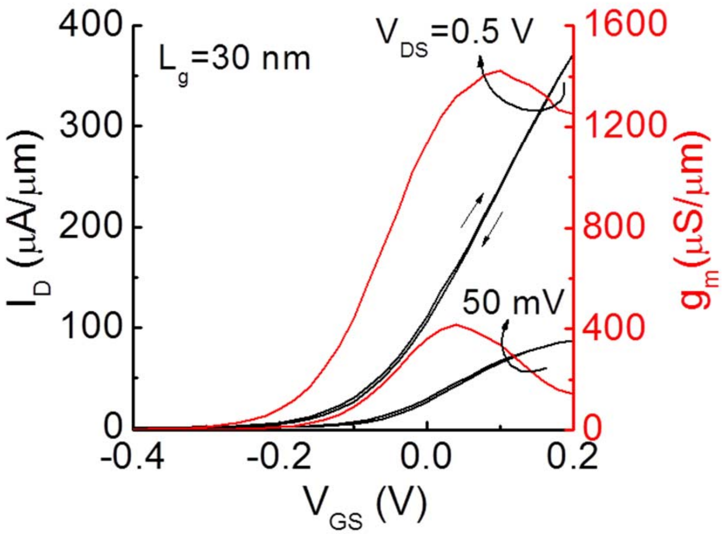


Lin, IEDM 2012



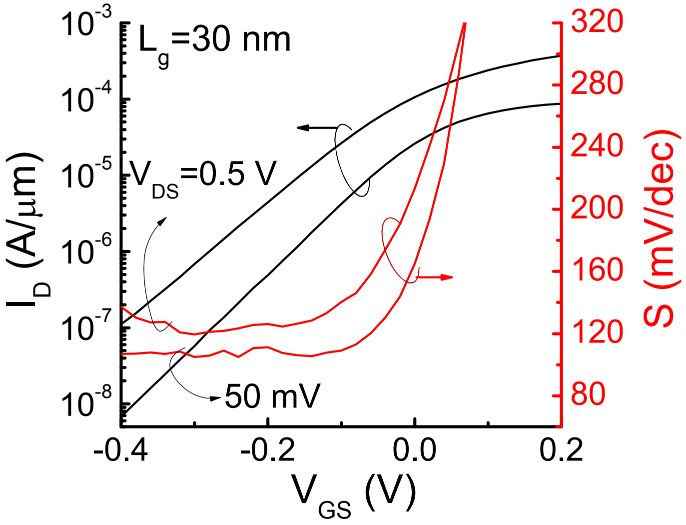
L_g=30 nm Self-aligned QW-MOSFET





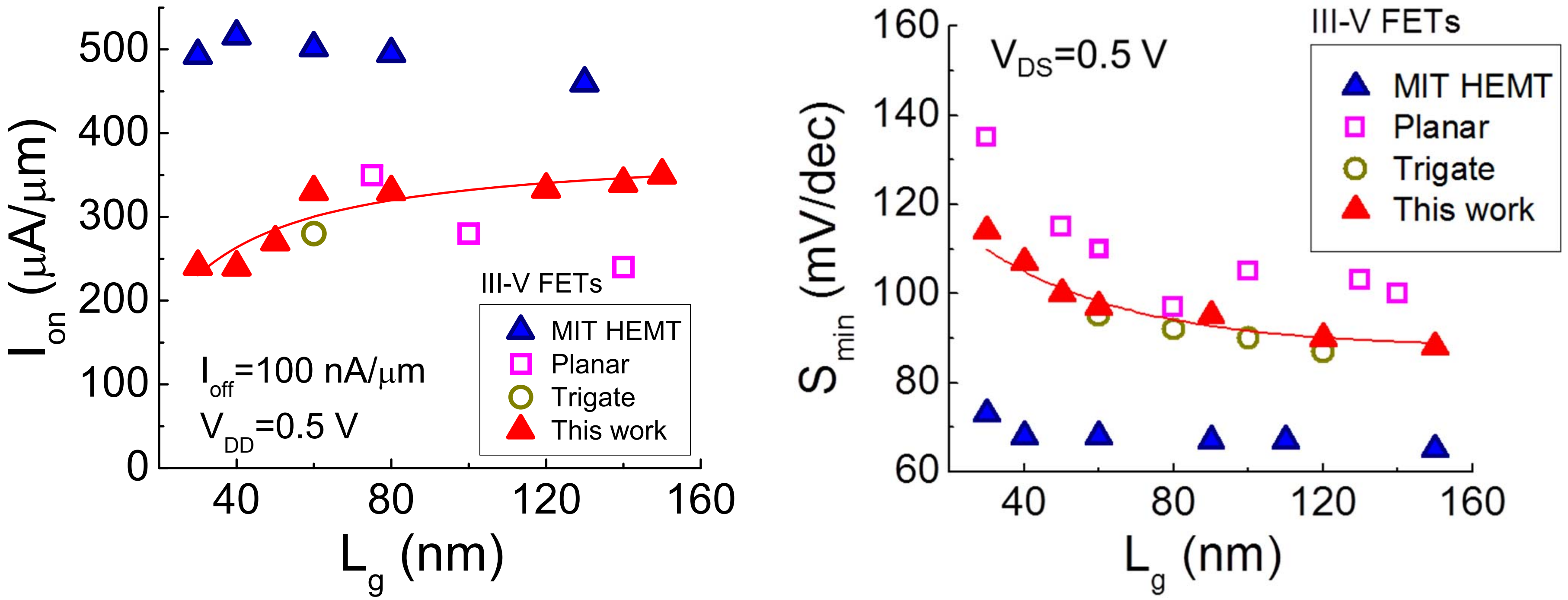
At V_{DS}=0.5 V:

- g_m = 1.4 mS/μm
- S=114 mV/dec
- I_g<1 nA/μm
- R_{on} = 470 Ω.μm



Lin, IEDM 2012

Scaling and benchmarking

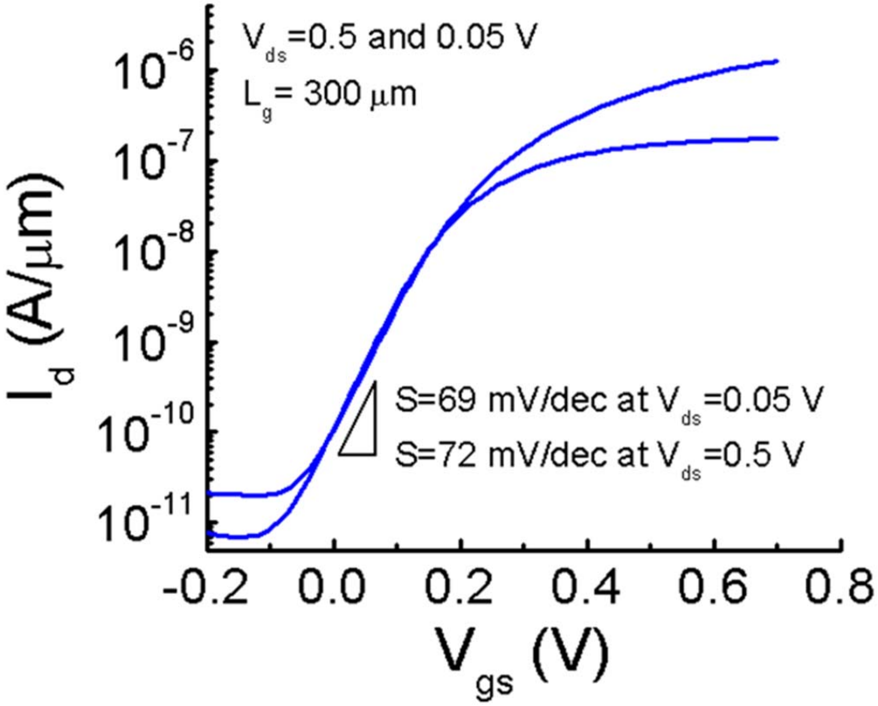


Lin, IEDM 2012

- Superior behavior to any planar III-V MOSFET to date
- Matches performance of III-V Trigate MOSFETs [Radosavljevic, IEDM 2011]

Long-channel InGaAs MOSFET

InP (1 nm) + Al_2O_3 (0.4 nm) + HfO_2 (2 nm) → EOT~0.9 nm



Lin, IEDM 2012

- S=69 mV/dec at V_{DS}=50 mV
- Close to lowest S reported in any III-V MOSFET: 66 mV/dec (EOT=1.2 nm) [Radosavljevic, IEDM 2011]

Ongoing research

- N-channel InGaAs MOSFETs:
  - Planar InGaAs MOSFET with improved access region for reduced resistance
  - Trigate InGaAs MOSFET with self-aligned contacts
  - Nanowire MOSFET with enhanced subthreshold swing
  - Ohmic contacts to InGaAs MOSFET
- P-channel InGaSb MOSFETs:
  - Planar InGaSb MOSFET with uniaxial compressive strain for enhanced hole transport
  - Ohmic contacts to InGaSb MOSFET