Strain and Temperature Dependence of Defect Formation at AlGaN/GaN High-Electron-Mobility Transistors on a Nanometer Scale

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***Abstract*—We use depth-resolved cathodoluminescence spectroscopy (DRCLS), Kelvin probe force microscopy (KPFM), and surface photovoltage spectroscopy (SPS) on a nanometer scale to map the temperature, strain, and defects inside GaN high-electron-mobility transistors. DRCLS maps temperature at localized depths, particularly within the 2-D electron gas region during device operation. KPFM maps surface electric potential across the device, revealing lower potential patches that decrease rapidly with increasing OFF-state stress. CL spectra acquired at these patches exhibit defect emissions that increase with both ON- and OFF-state stresses and that increase with decreasing surface potential. SPS also reveals features of deep level gap states generated after device operation that reduce near-band-edge emission and increase surface band bending. Our nanoscale measurements are consistent with defect generation by inverse piezoelectric field-induced stress at the gate edge on the drain side at high voltage.**

***Index Terms*—AlGaN/GaN high-electron-mobility transistor (HEMT), defect characterization, depth-resolved cathodoluminescence spectroscopy (DRCLS), HEMT, Kelvin force probe microscopy, strain mapping, surface photovoltage spectroscopy (SPS), temperature mapping.**

I. Introduction

For high-power and high-speed applications, GaN-based semiconductor devices are promising candidates for high-electron-mobility transistors (HEMTs). This is due to GaN's high breakdown field, superior carrier saturation velocity, and combination of high electron mobility and 2-D electron gas (2-DEG) density [1]. However, high channel temperatures and electric fields under high-power operation accelerate physical and electrical device degradation.

Notwithstanding extensive studies by many groups, the physical mechanisms underlying GaN HEMT reliability remain elusive, in large part due to the interactions between high electric fields, mechanical stress, and temperature inside the device structure.

Temperature distributions of GaN-based HEMTs have been measured by various methods such as micro-Raman method [2], scanning thermal microscopy [3], and depth-resolved cathodoluminescence spectroscopy (DRCLS) [4]. There is a general consensus that temperatures reach a maximum near the drain-side edge of the gate. Likewise, high electric fields may induce point defects or structural damage at device surface/subsurface regions that degrades reliability [5]–[20]. While it has been postulated that defects are generated as a result of OFF- and ON-state stresses [9], [10], [12]–[16], a direct mapping of these defects has not been done. Furthermore, 3-D distributions of temperature and electric field have not been measured on a nanometer scale in order to address these physical failure mechanisms.

In this paper, we use several techniques to monitor electronic and mechanical properties inside operating GaN HEMTs under both ON- and OFF-state stresses: 1) DRCLS of defect emissions, cross-sectional temperature, and stress distributions; 2) Kelvin probe force microscopy (KPFM) of surface electric potential and band bending; 3) surface photovoltage spectroscopy (SPS) of defect levels within the GaN band gap. These provide direct evidence for device failure associated with the creation of electrically active defects in AlGaN/GaN HEMTs localized at the gate edge close to the AlGaN/GaN interface due to the inverse piezoelectric effect [11].

II. Experimental Setup

Here, we present results for three GaN HEMT devices termed U-01, U-08, both grown on sapphire with gate length of ~1.25 μm and gate width of ~70 μm, and M-01, grown on a SiC substrate with gate length of ~0.25 μm and gate width of ~40 μm. U-01 and U-08 heterostructures consist of an unintentionally doped GaN layer, a 40-nm $Al_{0.22}Ga_{0.78}N$, and

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a 10-nm Si-doped graded $Al_xGa_{1-x}N$ layer $(0 \leq x \leq 0.22)$ sandwiched by a 0.7-nm AlN interfacial layer and a 250-nm GaN cap. The GaN cap layer was etched to form drain (D), gate (G), and source (S) contacts. M-01 consists of a thick GaN buffer layer, followed by 1-nm AlN, 16-nm $Al_{0.28}Ga_{0.72}N$, a 3-nm GaN cap, and a Si_3N_4 passivation layer. Thus, the etched U-01 and U-08 samples are nearly equivalent in structure to the M-01 heterostructure. Furthermore, devices U-01 and U-08 have similar material and electrical properties.

In order to measure defect generation and cross-sectional temperature distribution on a nanometer scale, we use a JEOL JAMP-7800F ultrahigh vacuum (UHV) scanning electron microscopy (SEM) with beam energy 5 keV $\leq E_B \leq$ 22 keV and temperature 12 K $< T <$ 300 K. An $E_B = 5$ keV beam excites the 2-DEG in the U-series, whereas the thicker overlayer of the M-series requires 10 keV. DRCL spectra provide local temperature at the GaN layer since its near band edge (NBE) emission varies systematically with temperature [24]

$$E_g(T) = E_g(0) - (5.98 \pm 0.12 * 10^{-6}) * T \qquad (1)$$

where $E_g(0)$ is the GaN band gap at 0 K. We used multilayer Monte Carlo [21] simulations to select an E_B that probes the 2-DEG region and to estimate penetration depths for mapping 2-D cross-sectional temperature distributions. Experimental details can be found elsewhere [22]–[24]. A Park XE-70 AFM/KPFM with ~20-nm lateral resolution, tungsten lamp, and monochromator provided simultaneous topography, potential maps, and surface photovoltage (SPV) spectra. An Agilent 4145B analyzer enabled device operation and dc ON- (high I_D, low V_{DS}) and OFF-state (low I_D, high V_{DS}) stresses during measurements. The ON-state device conditions were as follows: $V_{DS} = 10$ V, $V_{GS} = -2$ V, $I_D = 0.47$ A/mm (M-01) for 12 h or $V_{DS} = 6$ V, $V_{GS} = 0$ V, and $I_D = 0.75$ A/mm (U-01) for 11 min. The longer stress time for the device on SiC is to ensure a similar degree of degradation as in the device on sapphire. The OFF-state stress conditions were as follows: $V_{DS} =$ 10–30 V, increasing in 2-V steps in order to insure a transition through the critical voltage point [25], $V_{GS} = -6$ V, and $I_D = 5 * 10^{-6}$ A/mm. Each step period was ~1 min. Experiments were performed on unpackaged on-wafer devices and at room temperature. Details of electrical characterization results such as gate leakage current I_{G-off} and I_{D-max} are described elsewhere [15]. The OFF-state stress measurements permit us to factor out temperature effects since heating is negligible with the minimal currents involved.

III. Results and Discussion

A. Temperature

1) Across Extrinsic Source and Drain: The study of device degradation at the nanoscale involves both ON- and OFF-state conditions which give rise to temperature and strain effects, respectively. First, we consider the effects of temperature under ON-state conditions. We then examine the effects of strain under OFF-state conditions. Fig. 1 shows a temperature distribution with 100-nm spatial resolution for virgin device M-01 operating at $V_{DS} = 6$ V, $V_{GS} = -1$ V, and $I_D = 1$ A/mm with beam current I_B ~4.5 nA. Regions between the gate–source and gate–drain are termed “extrinsic source” and “extrinsic drain,” respectively. Peak electron-hole excitation depth U_0 derived from a Monte Carlo simulation for $E_B = 10$ keV is 655 nm below the Si_3N_4 passivation surface, i.e., close to the 2-DEG channel region. The red dashed lines show the edge of the gate. The temperature increases from the drain side to the gate overhang edge at the extrinsic drain region. The temperature distribution at the extrinsic source region exhibits a similar trend. Furthermore, the temperature is higher within the extrinsic drain region compared with the extrinsic source region. These results agree with the results extracted by a micro-Raman method [2]. Note that the electron beam-induced current under our measurement conditions ($I_B = 4.5$ nA, $E_B = 10$ keV) is ~0.04 A/mm, which is negligible compared with device currents so that localized electron beam heating is not significant. Likewise, piezoelectric strain can also shift the NBE emission peak [26], but its effect is very small at $V_{DS} = 6$ V and does not affect our temperature measurement. Neither this current nor this strain has a measurable effect on the NBE emission energy.

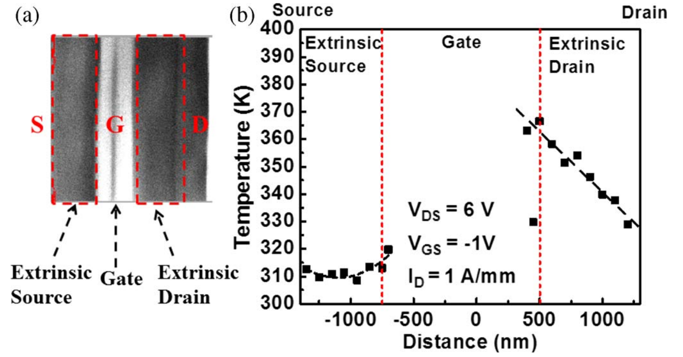

Fig. 1. (a) SEM image of virgin sample M-01 source–gate–drain areas across which temperatures were measured. Dashed red rectangles mark extrinsic drain and source areas. (b) Temperature distribution across extrinsic drain and source area at $V_{DS} = 6$ V, $V_{GS} = -1$ V, and $I_D = 1$ A/mm with $E_B = 10$ keV. Dashed black lines are guides to the eye. Temperature increases monotonically from drain to gate overhang edge.

2) Across Extrinsic Source and Drain in Depth: DRCLS measurements also provided *in situ* measurements of temperature versus depth across the extrinsic source and drain, in effect yielding cross-sectional temperature maps during device operation, e.g., in Fig. 2. U_0 from the top of the Si_3N_4 passivation layer with E_B between 10 and 22 keV in 2-keV step are 655, 770, 920, 1070, 1250, 1460, and 1730 nm, respectively, while we used $E_B = 8$ keV to probe the GaN cap surface. The corresponding positions are also marked in Fig. 2(a) and (b). The lateral and depth resolution for 8 keV is ~100 nm, proportionally larger for higher beam energies. According to the contour map, the temperature distribution varies from 300 K to 370 K (27 °C–97 °C). Monte Carlo simulations show that the rate of CL excitation peaks at characteristic depths, increasing with increasing incident beam voltage E_B [22]. Since electron-hole recombination at shallower depths contributes to the CL spectra, we subtract these contributions with spectra at slightly lower E_B to achieve even finer depth resolution of the temperature distribution inside the device. Fig. 2(b) shows a magnified view of the region close to the edge of the gate overhang. Here,

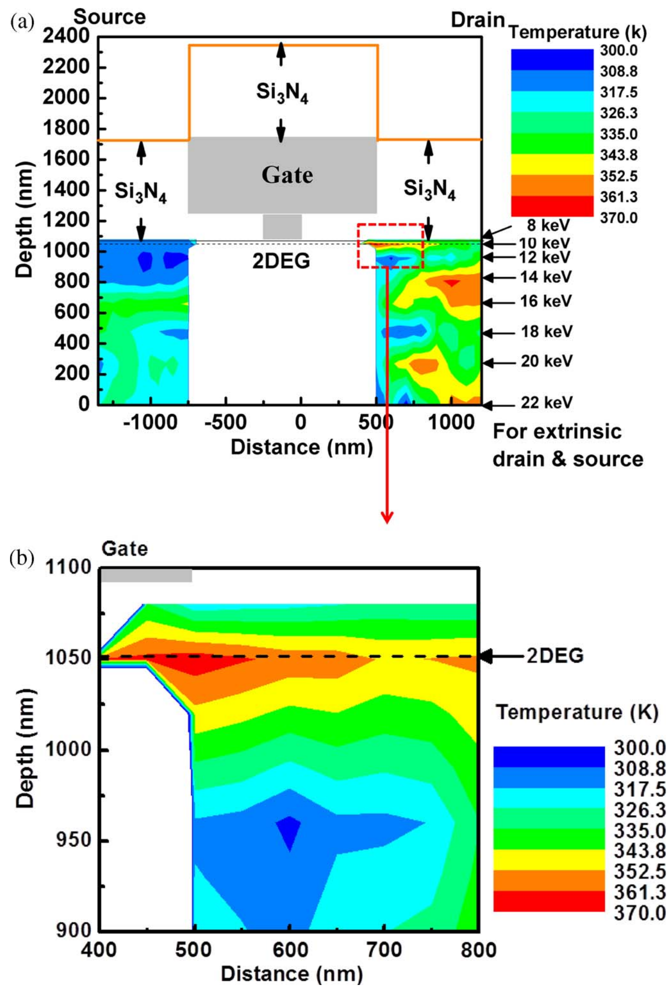

Fig. 2. DRCLS cross-sectional temperature distribution of sample M-01: (a) Whole device and (b) device drain side close to gate overhang. $V_{\mathrm{DS}} = 6$ V, $V_{\mathrm{GS}} = -1$ V, $I_{\mathrm{D}} = 1$ A/mm, and $8 < E_{\mathrm{B}} < 22$ keV. Multiple hot spots are apparent.

multiple hot spots are evident inside the operating GaN HEMT. One is near the gate overhang edge, where electric field and current density are high. The other two are 260 and 800 nm below the extrinsic-drain-side 2-DEG channel. Pomeroy *et al.* [27] proposed that hot spots will form around defects in GaN HEMTs. We suggest that point defects or dislocations may impede thermal transfer, leading to hot spots.

B. Stress Distribution

Fig. 3 shows the field-induced-stress distribution caused by the external bias from source to drain with various bias conditions of a virgin device at U-01. With $E_{\mathrm{B}} = 5$ keV, we are able to probe the region close to the 2-DEG region. In order to prevent any self-heating effects, the gate voltage (V_{GS}) was kept at -6 V to limit the channel current to $< 5 * 10^{-6}$ A/mm. DRCLS measures the field-induced stress at the AlGaN/GaN interface under OFF-state stress condition from NBE peaks, which shift by 26 meV/GPa [28] with no self-heating. DRCLS shows a 7.6-meV blueshift corresponding to a 0.29-GPa compressive stress in the GaN layer at the gate-edge drain side with $V_{\mathrm{DS}} = 26$ V. The line scan results also show that the field-induced

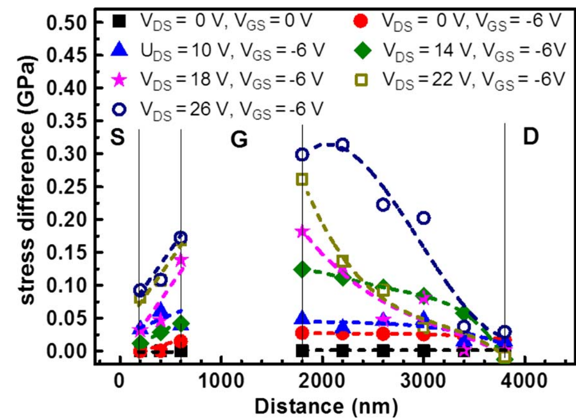

Fig. 3. Field-induced-stress distribution of a virgin device caused by applied bias under OFF-state stress. S, G, and D denote source, gate, and drain metal contacts. Dashed lines are guides to the eye. A maximum ~0.29-GPa compressive stress increase is evident at the gate-edge drain-side area. Field-induced OFF-state stress increases the most at drain-side gate-edge region.

stress increases faster at gate-edge drain-side regions than at regions close to the drain metal contact. Del Alamo *et al.* proposed an inverse piezoelectric degradation mechanism to explain the device performance deterioration due to high applied bias [10], [11]. The high field can induce mechanical stress that exceeds the crystal's elastic energy, creating lattice defects, particularly at the gate-edge drain-side area. While field-induced stress appears on both sides of the gate, Fig. 3 shows that the external stress is highest at the AlGaN/GaN interface close to the gate-edge drain-side area, so it is the likeliest place for defects to appear first. Regarding the effect of stress on our temperature measurements, Fig. 3 shows that the field-induced stress is negligible for the bias voltage used for our temperature distribution measurements ($V_{\mathrm{DS}} = 6$ V, $V_{\mathrm{GS}} = -1$ V). The piezoelectric strain can shift NBE energies by 26 meV/GPa = 43.5 °C/GPa. The field-induced-stress distribution in this case should be close to the $V_{\mathrm{DS}} = 0$ V, $V_{\mathrm{GS}} = -6$ V condition in Fig. 3 so that the temperatures extracted from DRCLS require little or no correction (0.03 GPa = ~1.3 °C). However, the thermal strain acts to impact the measure temperature by DRCLS by ~6.5 °C at 370 K, proportionally lower at lower temperature [30].

C. Surface Potential

Reliability is an important concern in GaN-based HEMTs due to the extreme current densities and strain under operation at high applied bias. Fig. 4 shows the AFM/KPFM results used to monitor unpassivated device characteristics with different stress conditions. Our previous results showed that there is a clear surface potential evolution with increasing OFF-state stress accompanied with an increase in gate leakage current [15]. With increased stress voltage, these low surface potential patches first form under or close to the gate, then shift to the drain-side gate edge, and then expand to extend across the extrinsic drain area. Finally, device failure occurs with crater formation close to the lowest surface potential area [15]. Although the surface potential changes dramatically as a result of high-voltage stress, no topography changes are observed before failure occurs and a crater appears. Fig. 4(b) and (c)

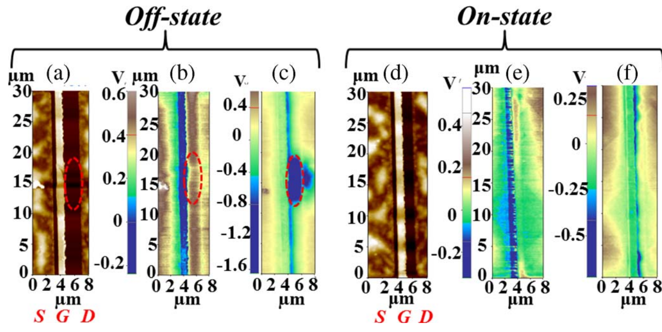

Fig. 4. AFM and KPFM results of GaN transistors before and after ON- and OFF-state stresses from representative areas. (a) and (d) Show AFM topography of source (S), gate (G), and drain (D), which are uniform before stress. (b) and (c) Show KPFM surface potential distribution before and after 30-V OFF-state stress, respectively. The red dashed oval indicates the lowest potential area, where device failure occurs. (e) and (f) Show KPFM potential maps before and after 11-min ON-state stress, respectively. Surface potential varies less with ON-state versus OFF-state stress.

shows the surface potential changes before and after OFF-state stress.

Fig. 4(e) and (f) show surface potential changes before and after ON-state stress. For ON-state stress, similar surface potentials occur but without clear trend or expansion. Koley *et al.* found that low surface potential areas form close to the drain-side gate edge after stress, which they attribute to the accumulation of negative charge from gate tunneling electrons under high bias stress [28]. Instead, we propose that the appearance of low surface potential patches is due to ON- and OFF-state stress-induced defect formation.

D. Stress-Induced Defects

DRCLS measurements within the extrinsic source and drain provide further evidence for stress-induced defect formation that correlates with device degradation. The DRCLS spectrum in Fig. 5(a) shows a 2.2-eV yellow band (YB), a 2.8–3.0-eV blue band (BB), and a 3.45-eV NBE emission from our M-01 GaN HEMT devices before ON- and OFF-state stresses. Poststress DRCLS shows higher defect emissions [4]. YB emission is often associated with Ga vacancies where BB emission may be due to bulk or surface defects [31]. Fig. 5(b) shows a 10–100× increase in the gate current at reverse bias after ON-state operation for 12 h in room ambient. We used DRCLS to correlate defect emissions with the degradation of the gate-edge extrinsic drain during device operation with two neighboring devices on the same die termed "device under test" (DUT) and "reference" (Ref). The DUT device on sample M-01 was ON state stressed for 12 h versus the unstressed Ref device.

The labeled regions in Fig. 5(c) are as follows: #1 (extrinsic drain, DUT), #2 (under gate–drain side, DUT), #3 (under gate–source side, DUT), #4 (extrinsic drain, Ref), and #5 (under gate, Ref). A SEM image of the defined regions appears in [4]. The YB/NBE ratios in regions #2 and #3 increase 4.3X and 2.6X, respectively. In contrast, the inset in Fig. 5(c) shows much weaker correlations for BB/NBE ratios. These results demonstrate that stress during device operation generates defects. Furthermore, stress affects different defects preferentially.

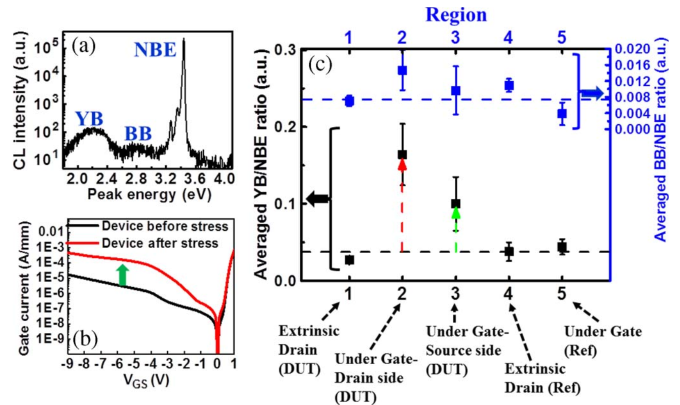

Fig. 5. (a) Representative prestress DRCLS spectra with YB, BB, and NBE peaks. (b) Gate current characteristics (black) before and (red) after stress of sample M-01. The increase of the gate leakage current indicates the degradation of gate Schottky contact after stress. (c) Position-dependent averaged YB/NBE ratio shows the largest increase at the region under gate–drain side after 12 h, $V_{\rm DS} = 10$ V, $V_{\rm GS} = -2$ V, and $I_{\rm D} = 0.47$ A/mm stress. Averaged BB/NBE ratio shows a much weaker response to local stress. The horizontal dashed lines represent the reference points.

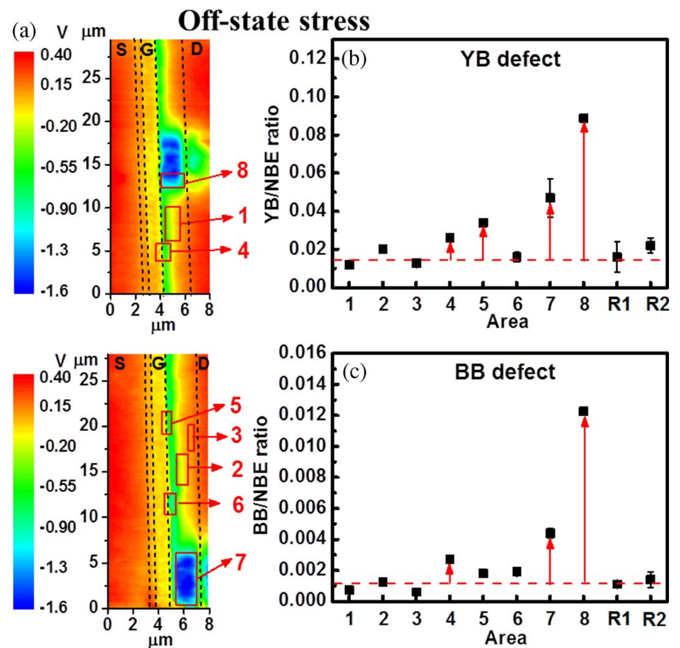

Fig. 6. (a) KPFM maps of sample U-01 from two representative areas of the same device along the width of the transistors show surface potential distribution and averaged defect emission after OFF-state stress. The device layout is indicated in the figure: Source (S), gate (G), and drain (D). (b) and (c) Averaged YB and BB/NBE ratios correspond to areas denoted in (a). In general, regions with lower potential correlate with higher YB or BB defect emission. The horizontal dashed lines represent the reference points.

Figs. 6 and 7 show the correlation between surface potential and defect emission of sample U-01 from two representative areas of the same device along the width of the transistors before and after ON-state ($V_{\rm DS} = 6$ V, $V_{\rm GS} = 0$ V, $I_{\rm D} = 0.75$ A/mm, 11 min) and OFF-state ($V_{\rm DS} = 10$–30 V in 2 V/step, $V_{\rm GS} = -6$ V, $I_{\rm D} = 5 * 10^{-6}$ A/mm) stresses. Potential maps and defect intensity increases for OFF- and ON-state stresses in Figs. 6 and 7 show that decreasing surface potential correlates with increased YB and BB intensities. Each data point of defect

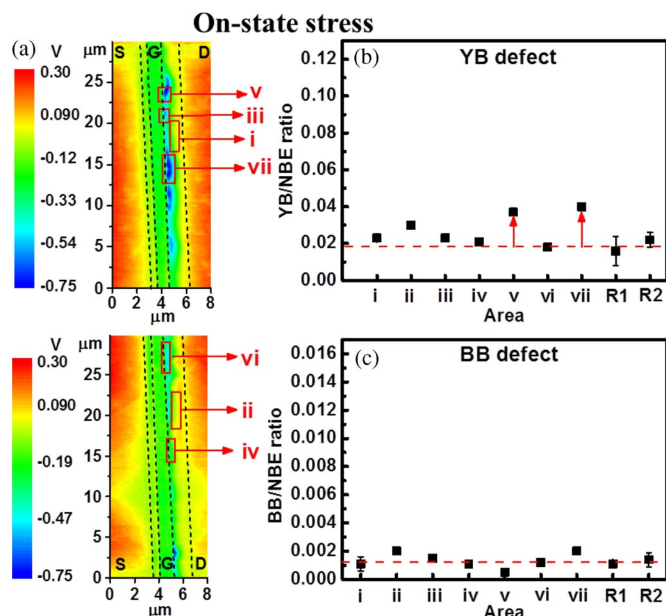

Fig. 7. (a) KPFM maps of sample U-01 from two representative areas of the same device along the width of the transistors show surface potential distribution after ON-state stress. The device layout is indicated in the figure: Source (S), gate (G), and drain (D). (b) and (c) Averaged YB and BB defect emissions correspond to areas denoted in (a). The horizontal dashed lines represent the reference points.

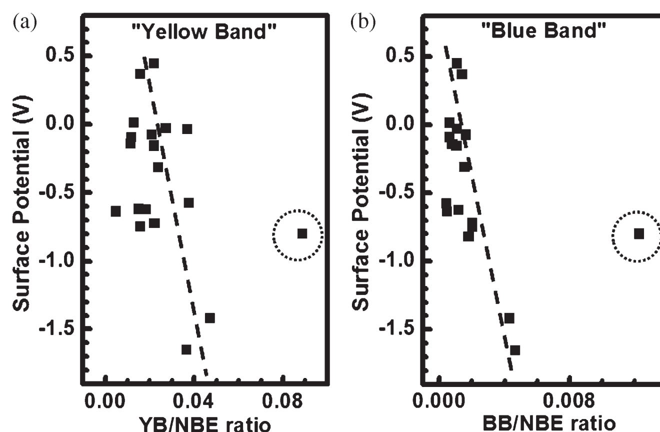

Fig. 8. Combined OFF- and ON-state surface potential versus (a) YB/NBE and (b) BB/NBE ratios from *individual* point spectra. Dashed lines are guides to the eye. The $\sim +0.4$-V surface potential corresponds to prestress potential, e.g., R1 and R2. The dashed circle denotes the FEA where defect emissions are strongly perturbed by catastrophic lattice disruption. In general, YB/NBE and BB/NBE ratios increase linearly as surface potential decreases.

emission in Figs. 6 and 7 represents an average of multiple spectra. For the OFF-state stressed device, areas 1, 2, and 3 are in the middle of the extrinsic drain and region close to the drain side where surface potential is higher (~ -0.008 V). Areas 4, 5, and 6 are at the gate-edge drain side with -0.52 V and ~ -0.8 V potentials. Area 7 has the second lowest potential (~ -1.6 V). Area 8 is at the crater edge where device failure occurs [failure edge area (FEA)]. For ON-state stress, areas (i) and (ii) are the middle of the extrinsic drain (~0.06 V), areas (iii) and (iv) are the gate-edge drain-side area with higher surface potential (~ -0.2 V), and areas (v), (vi), and (vii) are the gate-edge drain-side area with lower surface potential (~ -0.5 V). Regions 4, 5, 7, and 8 exhibit monotonically increasing YB and BB defect intensities with decreasing potential.

Areas 1, 2, and 3 exhibit negligible defect increases along with higher surface potential (~0.45 V), consistent with the defect versus potential correlation. Unstressed devices (R1 and R2) exhibit comparable defect emission to areas 1 and 2. Figs. 6 and 7 also show that ON-state potential changes are less pronounced and indicate correspondingly smaller defect increases. We observe no BB increases with ON-state stress. Sample M-01 and U-01 results show that device performance degrades during device operation (i.e., under ON- and OFF-state stresses) due to defect formation, and Fig. 5 shows that stress enhances defect emission preferentially. Within the same OFF- and ON-state stress duration (11 min), the device subjected to OFF-state stress exhibits larger variation in surface potential than that with ON-state stress. This is due to either the time of ON-state stress being not long enough to generate defects or the OFF-state stress having much more prominent effect on degrading device properties. We believe that the voltage stress [10] is the primary force causing device failure rather than the current or time. The effect of stress on $I_{\mathrm{G-off}}$ and $I_{\mathrm{D-max}}$ is described in [15].

Fig. 8 shows a systematic correlation between surface potential and YB/NBE as well as the BB/NBE ratios of individual spectra. We observed a clear trend of stronger defect emission with decreasing surface potential.

This agrees with previous simulation results showing how an increasing electrically active acceptor defect density near the midgap lowers the surface Fermi level [15]. These potential–defect density correlations mean the following: 1) KPFM can map where defects are generated at or close to the device surface, and 2) such maps provide a predictive tool for device failure by illustrating the region of lowest potential and highest defect density that corresponds to the initial point of failure.

Furthermore, these defect features exhibit a strong increase above a critical voltage [15] similar to the device results of [10] and [11]. In general, an increase of $I_{\mathrm{G-off}}$ and a decrease of $I_{\mathrm{D-max}}$ can be observed after ON- and OFF-state stresses. Thus, after OFF-state stress, Figs. 6 and 7 show 2.2X YB/NBE and 3.7X BB/NBE increases at the gate-edge drain side. The increase is even more obvious at the FEA, i.e., 4.7X YB/NBE and 10.4X BB/NBE ratio increases.

We used DRCLS and KPFM to correlate the defect emissions with potential changes further. Here, U-08 was operated to failure ($V_{\mathrm{DS}} = 3.5$ V, $V_{\mathrm{GS}} = 0$ V, $I_{\mathrm{D}} = 0.63$ A/mm, 4 h), i.e., crater formation, under UHV condition ($2 * 10^{-9}$ torr). UHV avoids uncertainties due to heating in air. The SEM image [4] shows that failure occurs at a "crater" at the extrinsic drain region. Fig. 9(a) shows the DRCLS spectrum acquired at 12 K with $E_{\mathrm{B}} = 5$ keV in region (1) before stress. The two major peaks are due to GaN with phonon replica (~3.45 eV) and AlGaN (~4.08 eV). No defect-related peaks are evident. Before device operation, the NBE emission is distributed uniformly. After device operation to failure, the DRCLS map shown in the center part of Fig. 9(c) with $E_{\mathrm{B}} = 5$ keV of GaN NBE (3.45 eV) intensity reveals major lateral variations, e.g., bright and darker regions (1) and (2), respectively, and the darkest

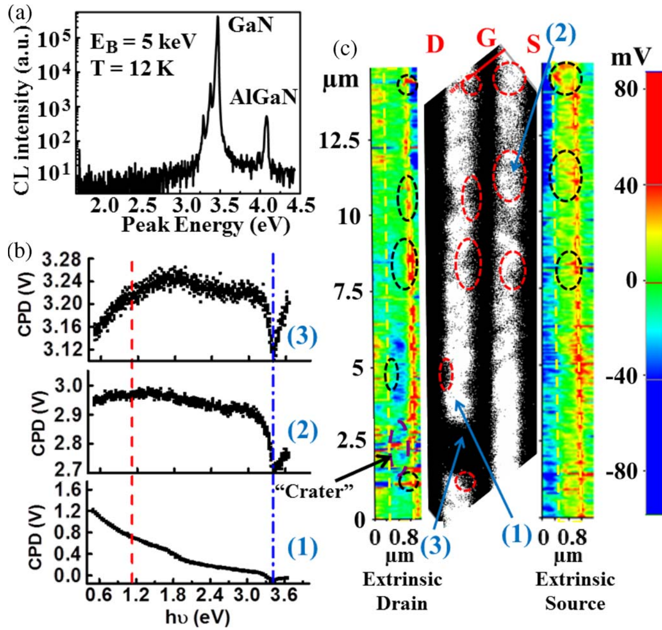

Fig. 9. (a) DRCLS results of sample U-08 taken at region (1) with $E_B =$ 5 keV at 12 K. (b) SPS maps taken from regions (1)–(3). (c) (Middle) CL map of NBE emission and (side) KPFM map of potential. Dashed lines delineate extrinsic drain and source areas. Both red and black circles show similar higher defect and higher potential regions for CL and KPFM maps. SPS spectra reveal a defect that is 1.2 eV above the valence band that increases with DRCLS defect emission intensities linked to device degradation.

region (3). NBE emission intensity decreases as defect density and alternate recombination pathways increase. The NBE and AlGaN peak intensities decrease 10–1000X between regions (1) and (3), indicating that a high density of nonradiative defects accumulate around/inside the crater region. Straddling the DRCLS maps in Fig. 9(c) are KPFM potential distributions at extrinsic drain and source regions, marked with dashed yellow rectangles, without any external bias. Here, surface potential varies by ±80 mV with higher potential regions aligning with reduced NBE emissions. These are outlined by red and black ellipses.

E. Defect Energy Level

We used SPS to determine the subband gap defect position of sample U-08 operated to failure. Fig. 9(b) shows, for all regions, a clear SPV change at ∼3.4 eV (blue dash-dotted line), assigned to the GaN band gap at room temperature.

SPS spectra acquired from regions (1), (2), and (3) display an increasing slope change at ∼1.2 eV (denoted by red dashed line) with proximity to the failure site. The sign of the slope change at this energy corresponds to a defect level located 1.1 eV above the valence band [32]. This result agrees with our DRCLS mapping result that defect densities are lower in brighter areas, e.g., region 1. With device operation, defects (native point defects and/or dislocations) may increase locally, decreasing or eliminating NBE luminescence. Significantly, the 2.2-eV YL defect emission from DRCLS and the ∼1.2-eV SPS feature of the same regions are near complements of the 3.45-eV GaN band gap, indicating a DRCLS optical transition from the conduction band 2.2 eV above. For sample U-08, the additional slope change at ∼1.6 eV in region (3) may be related to subsurface features created by the crater formation.

IV. Discussion

Our results relate directly to the various models proposed for AlGaN/GaN HEMT degradation. High mechanical stress during device operation generates electrically active defects [10], [11], [18]. These defects reduce I_D and increase I_{G-off}, and they become more evident if critical voltage is exceeded. Hot-electron effects also contribute to device degradation [9], [20], [33]. Here, "semi-on" conditions generate the highest hot-electron rate and the maximum degradation. Defect diffusion can also cause devices to fail [12], [14], [17]. Charged surface traps can diffuse into the device along dislocations and degrade device performance by altering channel potentials. This process may also be enhanced by an inverse piezoelectric effect, temperature, and leakage current.

Our observations of the device after OFF-state stress in this paper provide strong support for the inverse piezoelectric effect: 1) the increase in stress with OFF-state operation and its localization at the drain-side gate as evidenced by Fig. 3 which show that stress can preferentially exceed crystal elastic energy at certain areas; 2) the strong and localized changes in electric potential produced by OFF-state stress as evidenced by Figs. 4 and 6 and the failure due to crater formation that occurs at the lowest potential induced by stress; 3) the formation and intensity increase of electrically active defects in the areas exhibiting large potential decreases as shown by Fig. 6; 4) the increase in these defect emissions with proximity to the point of lattice disruption as illustrated by Fig. 6; and 5) the systematic correlation between potential changes and defect intensities shown in Fig. 8 that are consistent with surface band bending and increased free carrier recombination that are induced by charged acceptor states.

The bias-induced stress of 0.3 GPa is well below the critical resolved sheer stress value of 3.3 GPa or higher [34]–[37] needed to cause lattice disruption and defect formation. However, we calculate the built-in stress due to $Al_{0.25}Ga_{0.75}N$/GaN lattice mismatch to be 2.7 GPa, similar to other recent calculations [11]. Therefore, the bias-induced stress added to the built-in stress may account for our observation of native point defects above the bias threshold reported here [11]. Other mechanisms that may play a role include thermally induced stress and impurity diffusion [17].

Our observations of devices after ON-state stress show that "semi-on" and high-temperature conditions can produce hot electron and diffusion degradation from the following: 1) the localized potential changes in Fig. 4; 2) the device failure without high stress apparent in Fig. 9; and 3) the defect increases over time shown in Figs. 5 and 9. The ON-state stressing results also reveal that the device on SiC is more reliable compared to the device grown on the sapphire substrate with comparable operating power (M-01 versus U-01). Figs. 4–7 show that both ON- and OFF-state operating conditions give rise to degradation that manifested itself by electronic changes—the appearance of deep level defects and related changes in potential. However, for the realistic OFF-state and high-current ON-state operating

conditions reported here, we find that OFF-state conditions induce stronger defect features associated with device failure. These observations provide a self-consistent picture for the device degradation reported in [10], [11], and in this paper.

V. Conclusion

We have demonstrated the DRCLS capability to measure the temperature, strain, and defect distributions inside state-of-the-art GaN HEMT devices under realistic operating conditions. Both 1-D and cross-sectional characterizations are consistent with the previous literature. Cross-sectional temperature mapping shows not only the "hot" spot location predicted by simulation but also additional hot regions inside the operating device. DRCLS spectra and maps correlated with KPFM mapping show that defects can accumulate locally to change the surface Fermi level position, band bending, and, hence, surface potential after device operation. Our nanoscale external stress measurements are consistent with defects generated by inverse piezoelectric field-induced stress at the gate-edge drain-side area. The OFF-state stress degrades devices faster and generates both YB and BB defects, while the ON-state stress generates only YB defects. SPS identifies defects that are 1.2 eV above the GaN valence band that accumulate at failure (FEA) and other areas within the device after long-time ON-state stress. These results show a strong correlation between stress, surface potential, defect, and device failure. Overall, the nanoscale depth-resolved optical and scanning probe techniques can be used to describe GaN-based HEMT failure mechanisms and predict the first-to-failure area under realistic situations.

References

[1] Y. F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chacarkar, T. Wisleder, U. K. Mishra, and P. Parikh, "30 W/mm GaN HEMTs by field plate optimization," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 117–119, Mar. 2004.

[2] A. Sarua, H. Ji, M. Kuball, M. L. J. Uren, T. Martin, K. P. Hilton, and R. S. Balmer, "Integrated micro-Raman/infrared thermography probe for monitoring of self-heating in AlGaN/GaN transistor structures," *IEEE Trans. Electron Devices*, vol. 53, no. 10, pp. 2438–2447, Oct. 2006.

[3] R. Aubry, J.-C. Jacquet, J. Weaver, O. Durand, P. Dobson, G. Mills, M.-A. di Forte-Poisson, S. Cassette, and S.-L. Delage, "SThM temperature mapping and nonlinear thermal resistance evolution with bias on AlGaN/GaN HEMT devices," *IEEE Trans. Electron Devices*, vol. 54, no. 3, pp. 385–390, Mar. 2007.

[4] C.-H. Lin, T. A. Merz, D. R. Doutt, M. J. Hetzer, J. Joh, J. A. del Alamo, U. K. Mishra, and L. J. Brillson, "Nanoscale mapping of temperature and defect evolution inside operating AlGaN/GaN high electron mobility transistors," *Appl. Phys. Lett.*, vol. 95, no. 3, pp. 033510-1–033510-3, Jul. 2009.

[5] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the dc and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, Mar. 2001.

[6] Y. Dora, A. Chakraborty, S. Heikman, L. McCarthy, S. Keller, S. P. Denbaars, and U. K. Mishra, "Effect of ohmic contacts on buffer leakage of GaN transistors," *IEEE Electron Device Lett.*, vol. 27, no. 7, pp. 529–531, Jul. 2006.

[7] R. J. Simms, J. W. Pomeroy, M. J. Uren, T. Martin, and M. Kuball, "Current collapse in AlGaN/GaN transistors studied using time-resolved Raman thermography," *Appl. Phys. Lett.*, vol. 93, no. 20, pp. 203510-1–203510-3, Nov. 2008.

[8] U. Chowdhury, J. L. Jimenez, C. Lee, E. Beam, P. Saunier, T. Balistreri, S.-Y. Park, T. Lee, J. Wang, M. J. Kim, J. Joh, and J. A. del Alamo, "TEM observation of crack- and pit-shaped defects in electrically degraded GaN HEMTs," *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1098–1100, Oct. 2008.

[9] G. Meneghesso, G. Verzellesi, F. Danesin, R. Rampazzo, A. Tazzoli, M. Meneghini, and E. Zanoni, "Reliability of GaN high-electron-mobility transistors: State of the art and perspectives," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 2, pp. 332–343, Jun. 2008.

[10] J. A. del Alamo and J. Joh, "GaN HEMT reliability," *Microelectron. Reliab.*, vol. 49, no. 9–11, pp. 1200–1206, Jul. 2009.

[11] J. Joh, F. Gao, T. Palacios, and J. A. del Alamo, "A model for the critical voltage for electrical degradation of GaN high electron mobility transistors," *Microelectron. Reliab.*, vol. 50, no. 6, pp. 767–773, Mar. 2010.

[12] M. Ťapajna, U. K. Mishra, and M. Kuball, "Importance of impurity diffusion for early state degradation in AlGaN high electron mobility transistors upon electrical stress," *Appl. Phys. Lett.*, vol. 97, no. 2, pp. 023503-1–023505-3, Jul. 2010.

[13] S. Y. Park, C. Floresca, U. Chowdhury, J. L. Jimenez, C. Lee, E. Beam, P. Saunier, T. Balistreri, and M. J. Kim, "Physical degradation of GaN HEMT devices under high drain bias reliability testing," *Microelectron. Reliab.*, vol. 49, no. 5, pp. 478–483, Mar. 2009.

[14] K. V. Smith, S. Brierley, R. McAnulty, C. Tilas, D. Zarkh, M. Benedek, P. Phalon, and A. Hooven, "GaN HEMT reliability through the decade," *ECS Trans.*, vol. 19, no. 3, pp. 113–121, May 2009.

[15] C.-H. Lin, D. R. Doutt, U. K. Mishra, T. A. Merz, and L. J. Brillson, "Field-induced strain degradation of AlGaN/GaN high electron mobility transistors on a nanometer scale," *Appl. Phys. Lett.*, vol. 97, no. 3, pp. 223502-1–223502-3, Nov. 2010.

[16] A. R. Arehart, A. Sasikumar, G. D. Via, B. Winningham, B. Poling, E. Heller, and S. A. Ringel, "Spatially-discriminating trap characterization methods for HEMTs and their application to RF-stressed AlGaN/GaN HEMTs," in *Proc. IEEE IEDM*, Dec. 2010, p. 20.1.

[17] M. Kuball, M. Ťapajna, R. J. T. Simms, M. Faqir, and U. K. Mishra, "AlGaN/GaN HEMT device reliability and degradation evolution: Importance of diffusion processes," *Microelectron. Reliab.*, vol. 51, no. 2, pp. 195–200, Feb. 2011.

[18] J. Joh, J. A. del Alamo, K. Langworthy, S. Xie, and T. Zheleva, "Role of stress voltage on structural degradation of GaN high-electron mobility transistors," *Microelectron. Reliab.*, vol. 51, no. 2, pp. 201–206, Feb. 2011.

[19] E. A. Douglas, C. Y. Chang, D. J. Cheney, B. P. Cila, C. F. Lo, L. Lu, R. Holzworth, P. Whiting, K. Jones, G. D. Via, J. Kim, S. Jang, F. Ren, and S. J. Pearton, "AlGaN/GaN high electron mobility transistor degradation under on- and off-state stress," *Microelectron. Reliab.*, vol. 51, no. 2, pp. 207–211, Feb. 2011.

[20] M. Meneghini, A. Stocco, N. Ronchi, F. Rossi, G. Salviati, G. Meneghesso, and E. Zanoni, "Extensive analysis of the luminescence properties of AlGaN/GaN high electron mobility transistors," *Appl. Phys. Lett.*, vol. 97, no. 6, pp. 063508-1–063508-3, Aug. 2010.

[21] CASINO. [Online]. Available: http://www.gel.usherbrooke.ca/casino

[22] L. J. Brillson, "Nanoscale luminescence spectroscopy of defects at buried interfaces and ultra thin films," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 19, no. 5, pp. 1762–1768, Oct. 2001.

[23] D. R. Doutt, C. Zgrabik, H. L. Mosbacker, and L. J. Brillson, "Impact of near-surface native point defects, chemical reactions, and surface morphology on ZnO interfaces," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 26, no. 4, pp. 1477–1482, Jul. 2008.

[24] A. P. Young and L. J. Brillson, "Luminescence spectroscopy of GaN in the high temperature regime from room temperature to 900 °C," *Appl. Phys. Lett.*, vol. 77, no. 5, pp. 699–801, Jul. 2000.

[25] J. Joh and J. A. del Alamo, "Critical voltage for electrical degradation of GaN high-electron mobility transistors," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 287–289, Apr. 2008.

[26] A. Sarua, H. Ji, M. Kuball, M. J. Uren, T. Martin, K. J. Nash, K. P. Hilton, and R. S. Balmer, "Piezoelectric strain in AlGaN/GaN heterostructure field-effect transistors under bias," *Appl. Phys. Lett.*, vol. 88, no. 10, pp. 103502-1–103502-3, Mar. 2006.

[27] J. W. Pomeroy, M. Kuball, D. J. Wallis, A. M. Keir, K. P. Hilton, R. S. Balmer, M. J. Uren, T. Martin, and P. J. Heard, "Thermal mapping of defect in AlGaN/GaN heterostructure field-effect transistors using micro-Raman spectroscopy," *Appl. Phys. Lett.*, vol. 87, no. 10, pp. 103508-1–103508-3, Sep. 2005.

[28] G. Koley, V. Tilak, L. F. Eastman, and M. G. Spencer, "Slow transients observed in AlGaN/GaN HFETs: Effects of SiN_x passivation and UV illumination," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 886–893, Apr. 2003.

[29] K. Wan, A. A. Porporati, G. Geng, H. Yang, and G. Pezzotti, "Biaxial stress dependence of the electrostimulated near-band-gap spectrum of GaN epitaxial film grown on (0001) sapphire substrate," *Appl. Phys. Lett.*, vol. 88, no. 25, pp. 251910-1–251910-3, Jun. 2006.

[30] T. Batten, J. W. Pomeroy, M. J. Uren, T. Martin, and M. Kuball, "Simultaneous measurement of temperature and thermal stress in AlGaN/GaN high electron mobility transistors using Raman scattering spectroscopy," *J. Appl. Phys.*, vol. 106, no. 9, pp. 094509-1–094509-3, Nov. 2009.

[31] M. A. Reshchikov and H. Morkoc, "Luminescence properties of defects in GaN," *J. Appl. Phys.*, vol. 97, no. 6, pp. 061301-1–061301-95, Mar. 2005.

[32] T. A. Merz, D. R. Doutt, T. Bolton, Y. Dong, and L. J. Brillson, "Nanostructure growth-induced defect formation at ZnO surfaces," *Surf. Sci.*, vol. 605, no. 9/10, pp. L20–L24, May 2011.

[33] Y. S. Oyzyerv, B. R. Tuttle, R. D. Schrimpf, D. M. Fleetwood, and S. T. Pantelides, "Theory of hot-carrier-induced phenomena in GaN high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 96, no. 5, pp. 053505-1–053505-3, Feb. 2010.

[34] T. H. Sung, J. C. Huang, J. H. Hsu, and S. R. Jian, "Mechanical response of GaN film and micropillar under nanoindentation and microcompression," *Appl. Phys. Lett.*, vol. 97, no. 17, pp. 171904-1–171904-3, Oct. 2010.

[35] S.-R. Jian, T.-H. Fang, and D.-S. Chuu, "Analysis of physical properties of III-nitride thin films by nanoindentation," *J. Electron. Mater.*, vol. 32, no. 6, pp. 496–500, Jan. 2003.

[36] F. J. Xu, B. Shen, M. J. Wang, J. Xu, L. Lu, Z. L. Miao, Z. J. Yang, Z. X. Quin, G. U. Zhang, B. Lin, and S. L. Bai, "Mechanical properties of AlxGa1-xN films with high Al composition grown on AlN/sapphire templates," *Appl. Phys. Lett.*, vol. 91, no. 9, pp. 091905-1–091905-3, Aug. 2007.

[37] D. Cáceres, J. Vergara, R. González, E. Monroy, F. Calle, Z. Muño, and F. Omnès, "Nanoindentation on AlGaN thin films," *J. Appl. Phys.*, vol. 86, no. 12, pp. 6773–6778, Dec. 1999.

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