Nanometer-Scale III-V CMOS

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Short Course on The Future of Semiconductor Devices and Integrated Circuits

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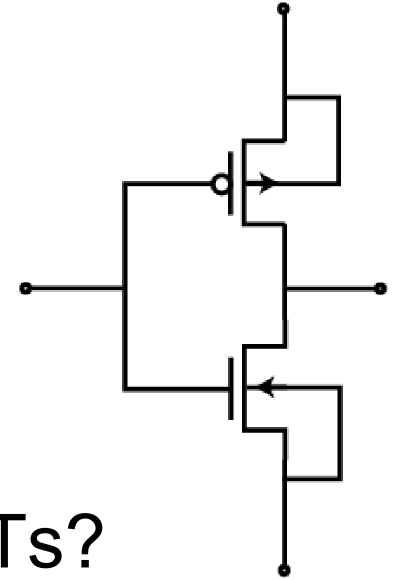
- D. Antoniadis, D.-H. Kim, T.-W. Kim, D. Jin, J. Lin, N. Waldron, L. Xia
- Sponsors: Intel, FCRP-MSD
- Labs at MIT: MTL, NSL, SEBL

Outline

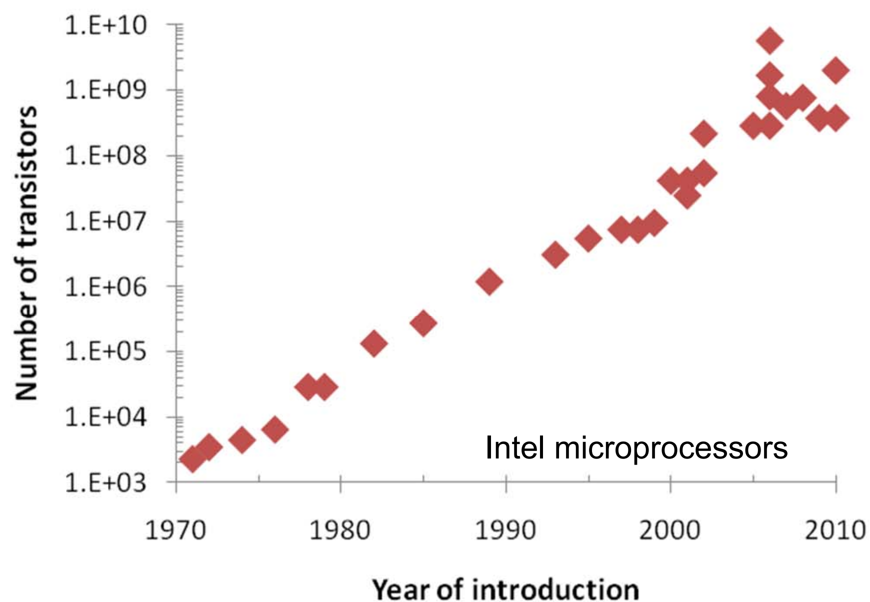


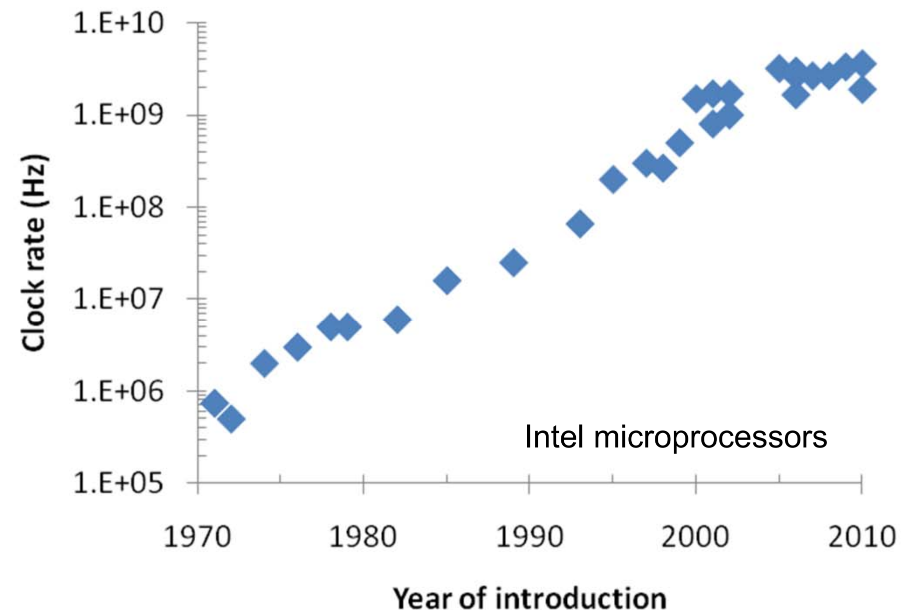
1. The CMOS revolution
2. Materials options for post-Si CMOS
3. What have we learned from III-V HEMTs?
4. III-V CMOS device design and challenges
   - Critical issue #1: the gate stack
   - Critical issue #2: the ohmic contacts
   - Critical issue #3: the p-channel device
   - Critical issue #4: non-planar MOSFET designs
   - Critical issue #5: co-integration of nFETs and pFETs
5. Concluding remarks

1. The CMOS Revolution:
Smaller is Better!

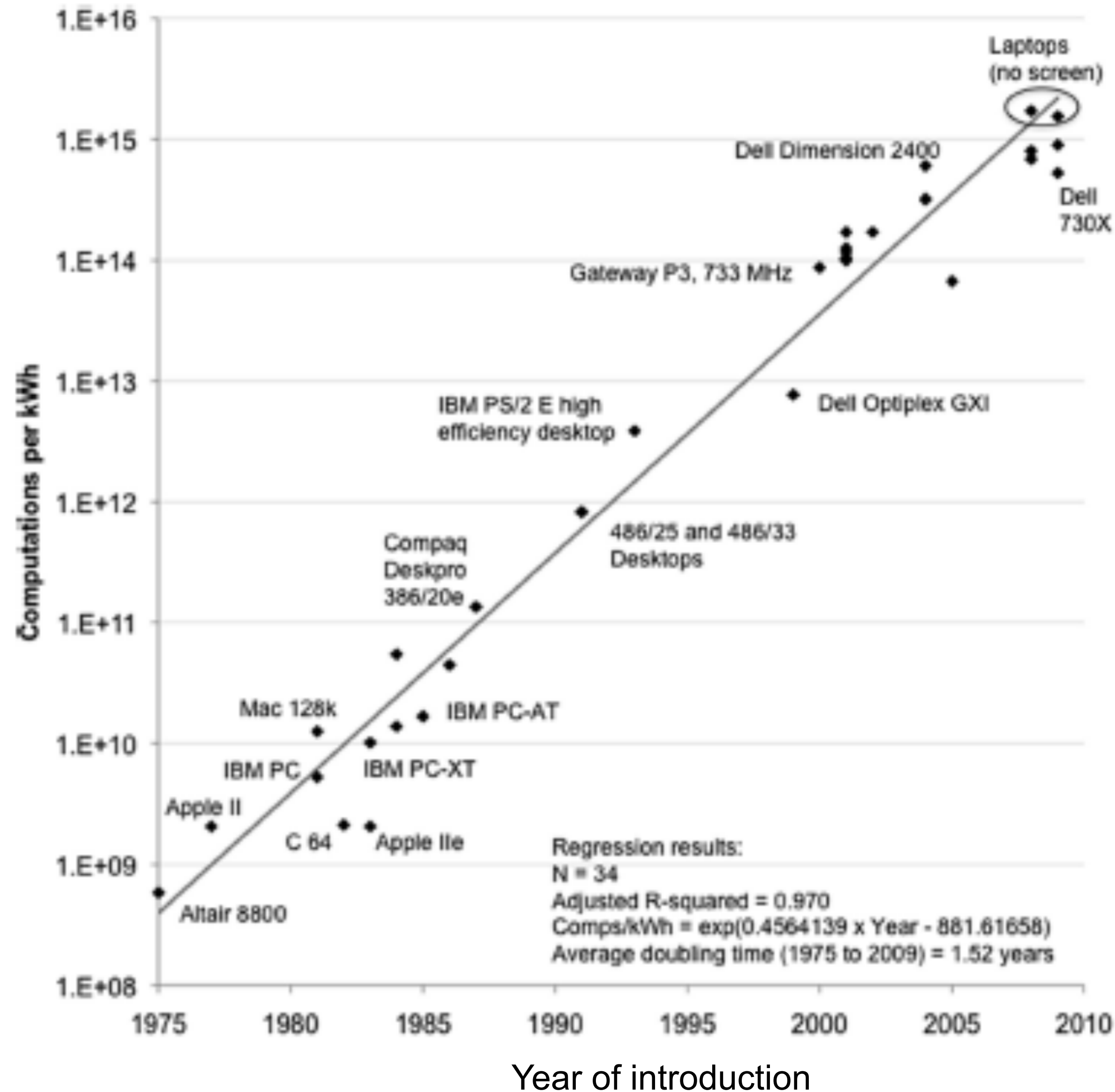
Virtuous cycle of scaling → exponential improvements in:

- *Transistor density* ("Moore's law")
- *Performance*
- *Power efficiency*





The Si CMOS Revolution: *Smaller is Better!*



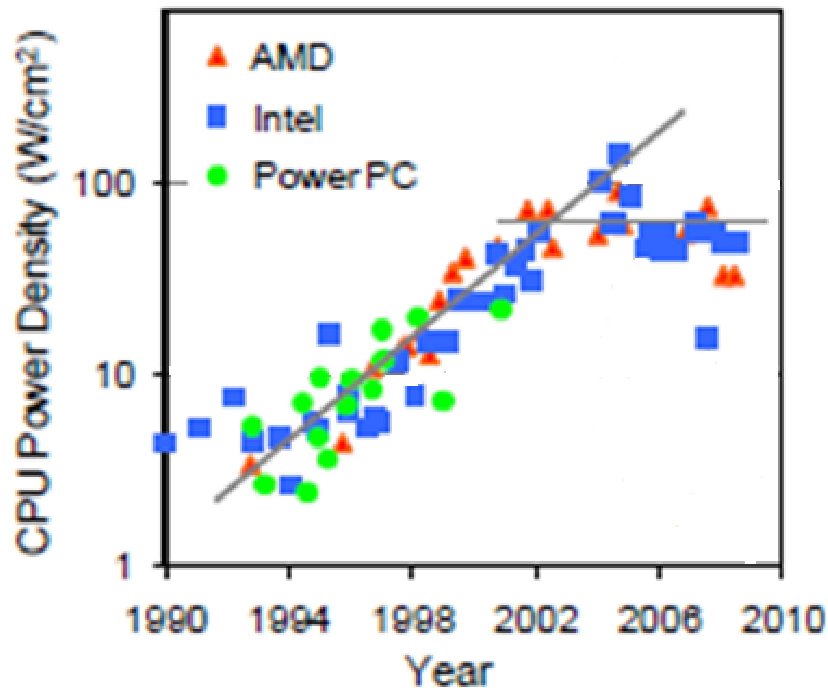
Year of introduction

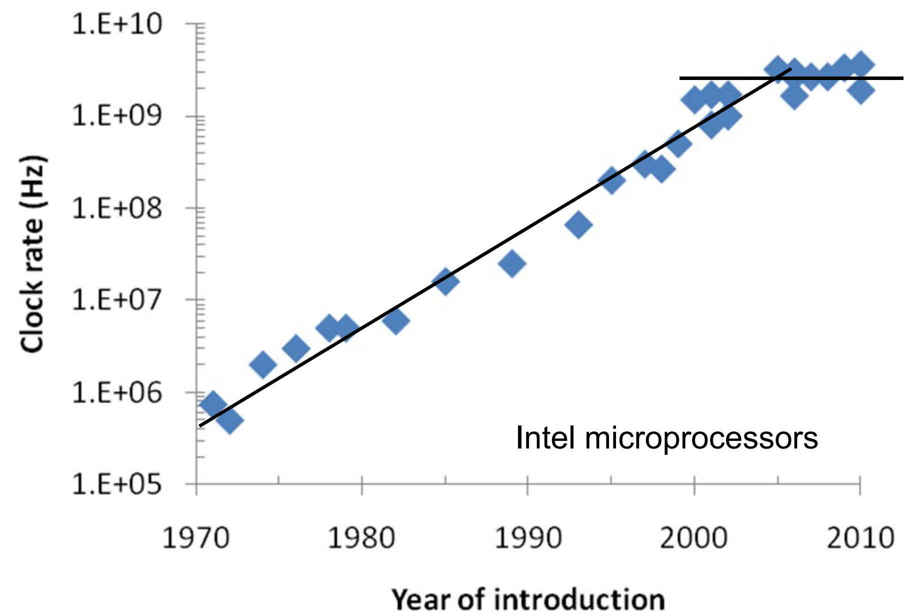
Koomey, Ann. Hist. Computing 2011

CMOS scaling in the 21st century

Si CMOS has entered era of *"power-constrained scaling":*

- Microprocessor power density saturated at ~100 W/cm^2
- Microprocessor clock speed saturated at ~ 4 GHz

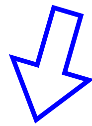


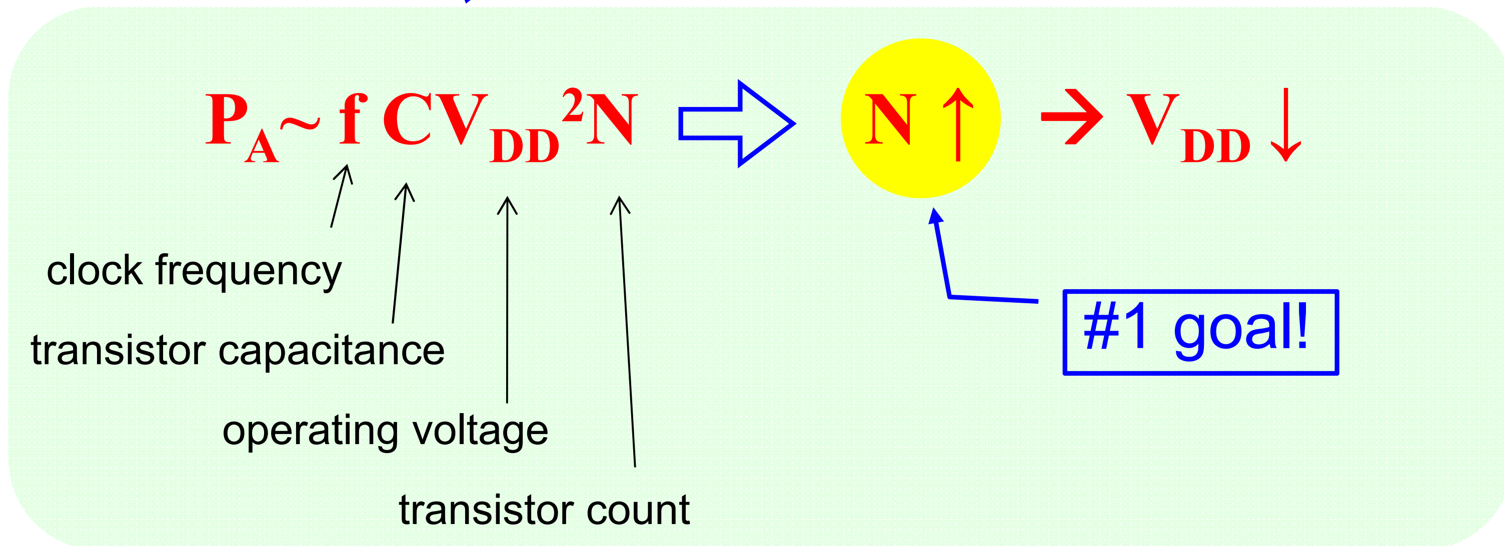


Pop, Nano Res 2010

Consequences of Power Constrained Scaling

Power = active power + stand-by power



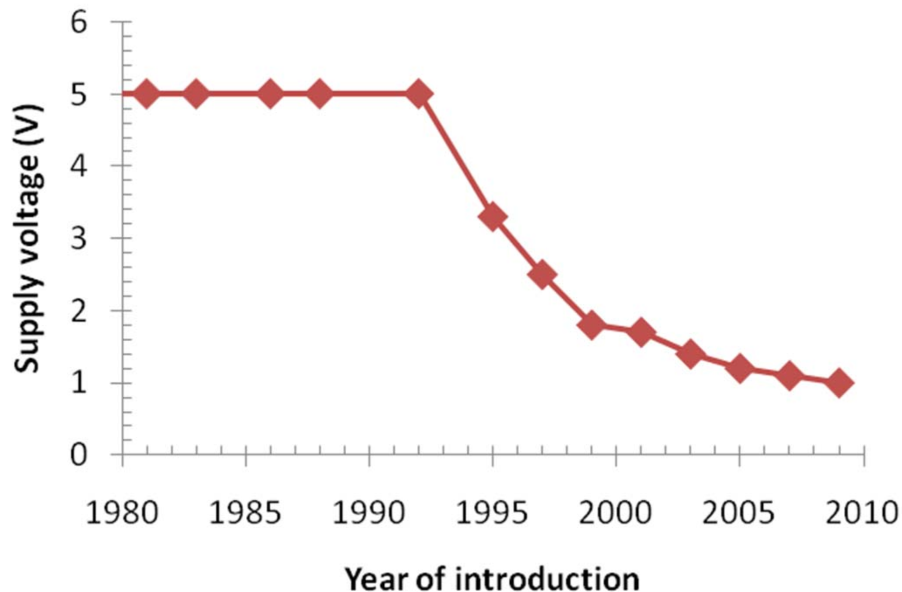


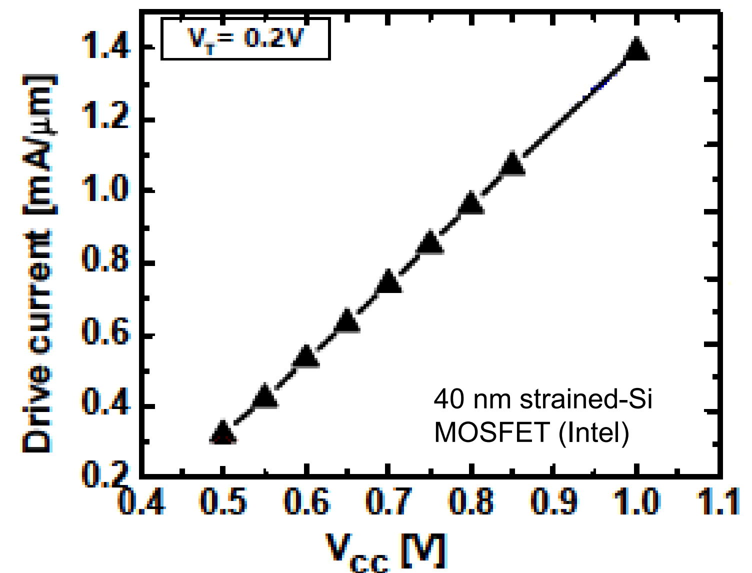
→ Transistor scaling requires reduction in supply voltage

CMOS power supply scaling

Recently, V_{DD} scaling very weakly…

… because Si performance degrades as V_{DD}↓



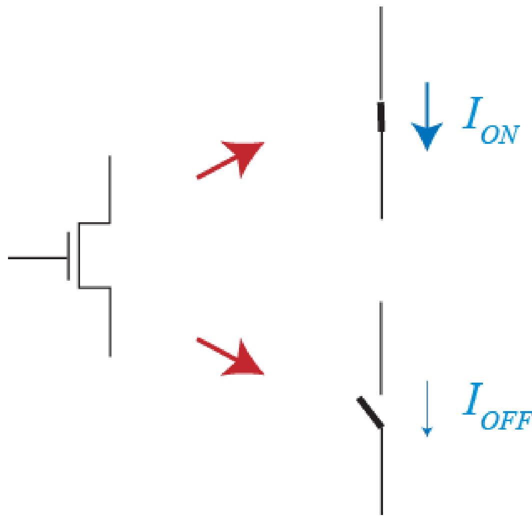


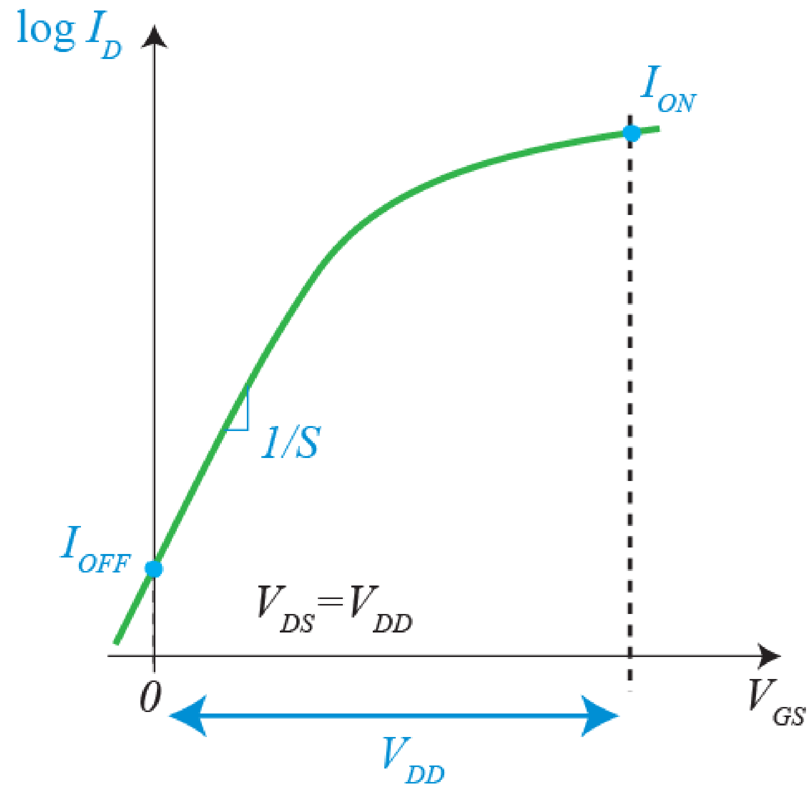
Dewey, IEDM 2009

→ Need scaling approach that allows V_{DD} reduction while enhancing performance

How to enable further V_{DD} reduction?

- Goals of scaling:
  - reduce transistor footprint
  - extract maximum I_{ON} for given I_{OFF}





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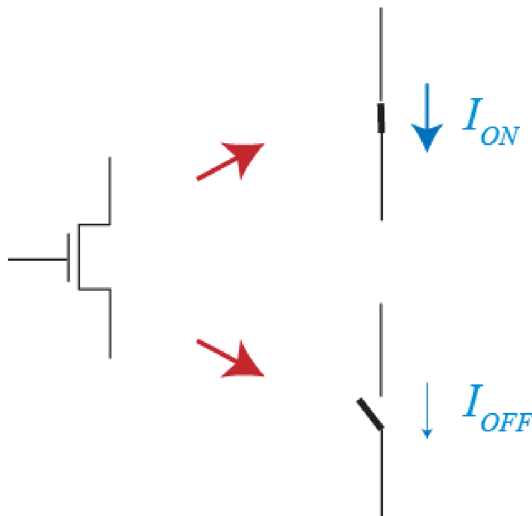
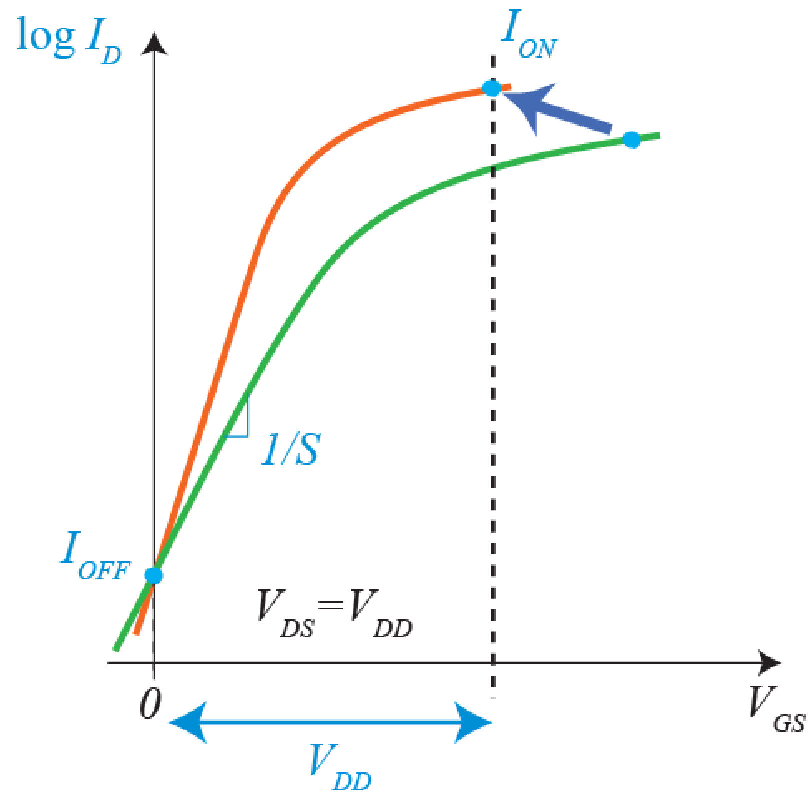




- The path forward:
  - increasing electron velocity → I_{ON} ↑
  - tighter carrier confinement → S ↓

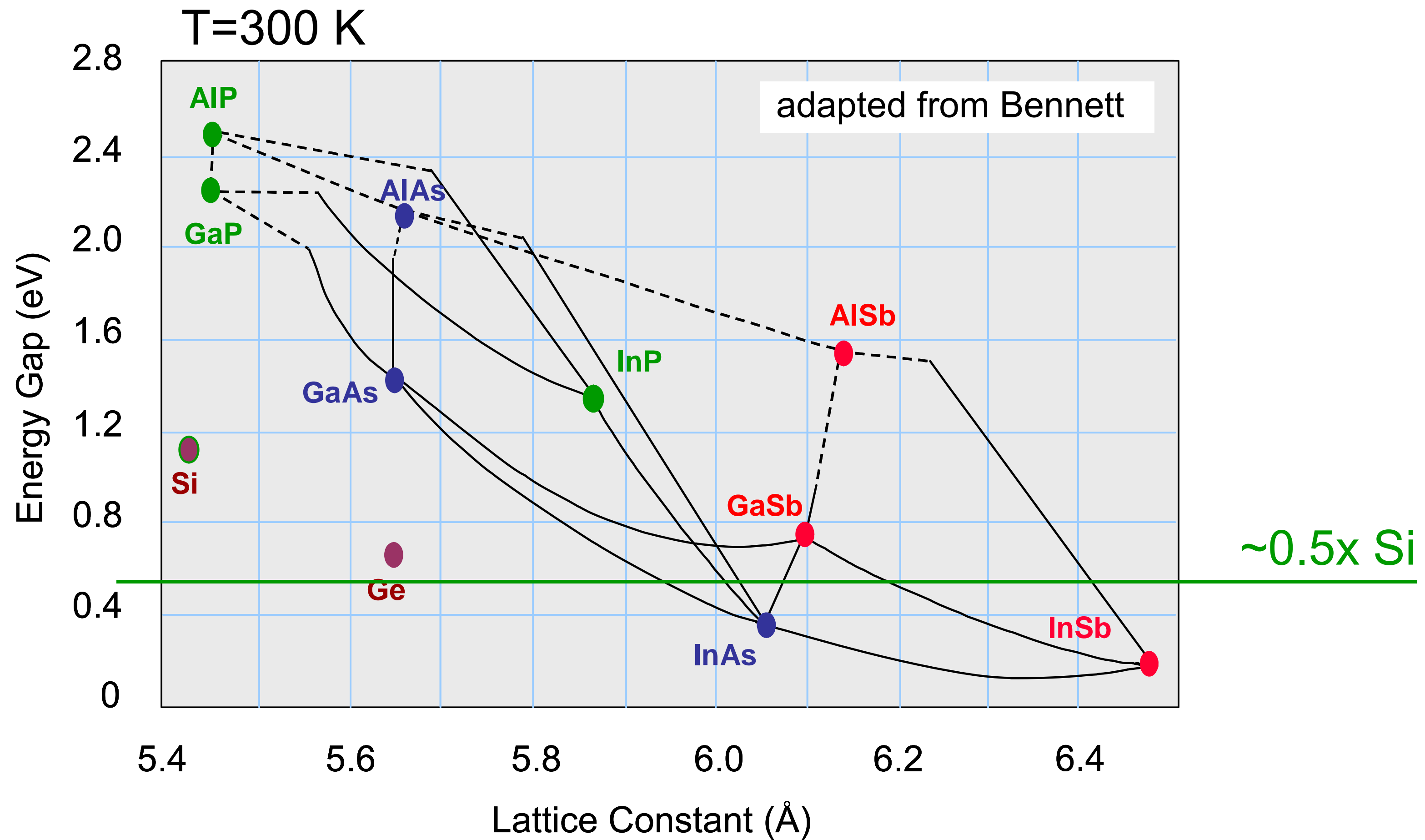
→ V_{DD} ↓

2. Materials options for post-Si CMOS

Ideally want:

- High electron and hole velocity
  - Si: v_e~1.5x10^7 cm/s, v_h~1.2x10^7 cm/s
- High sheet-carrier concentration at low voltage
  - Si: ~6x10^{12} cm^{-2} @1 V
- High enough bandgap energy
  - Si: E_g=1.1 eV
- High-quality, reliable MOS gate stack
  - Si: D_{it}~10^{11} $eV^{-1}.cm^{-2}$
- Same material for n-channel and p-channel device
- Easily integrable on Si substrate
- Manufacturable technology (top down, ex-situ dielectrics)

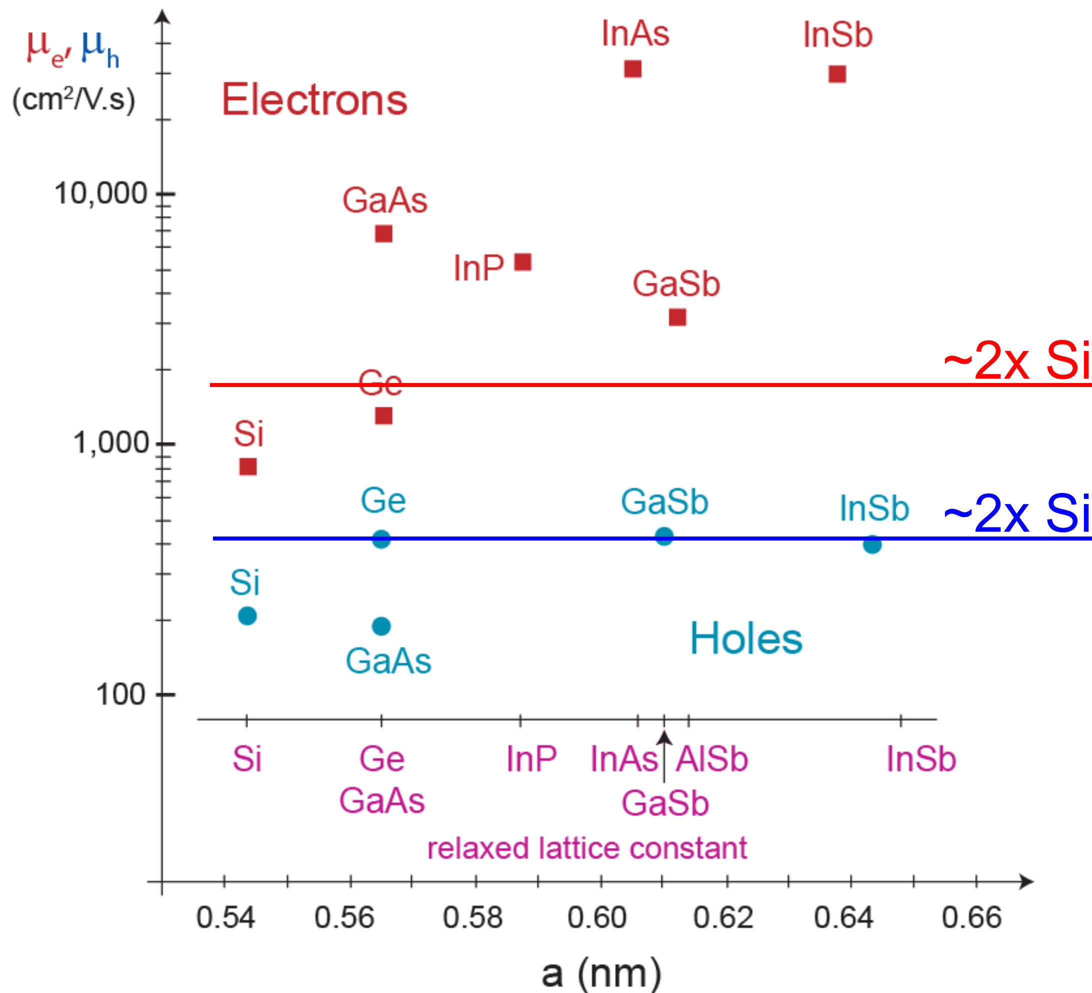
Bandgap energy



InAs, InSb problematic but strong quantum confinement can be used to enhance effective bandgap

Use mobility as proxy for velocity

300 K quantum-well or inversion layer mobility at any sheet carrier concentration:



GaAs, InP, GaSb: promising for nFET

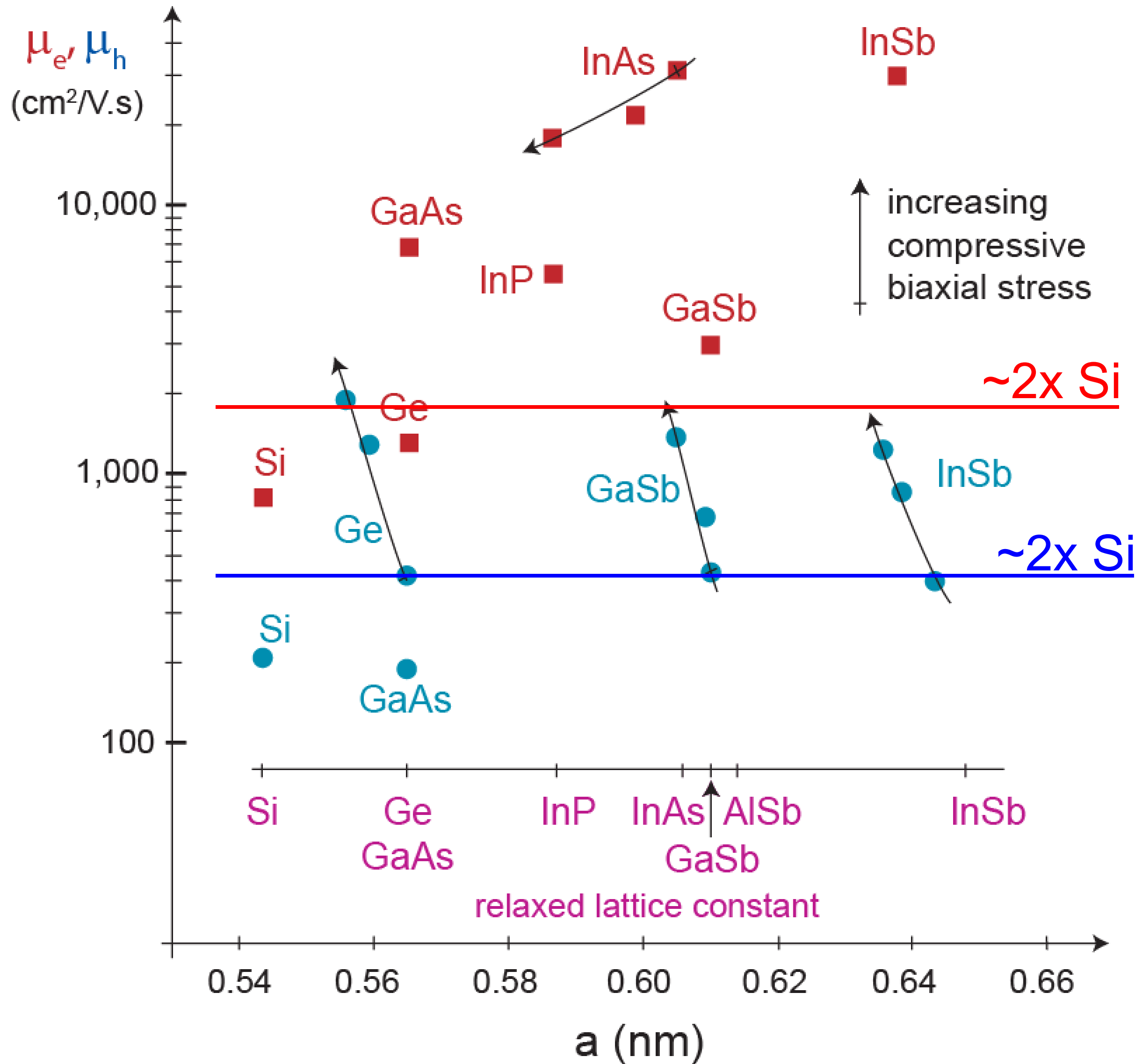
Ge: borderline nFET

Ge, GaSb, InSb: borderline pFET

GaAs: ruled out for pFET

del Alamo, Nature 2011

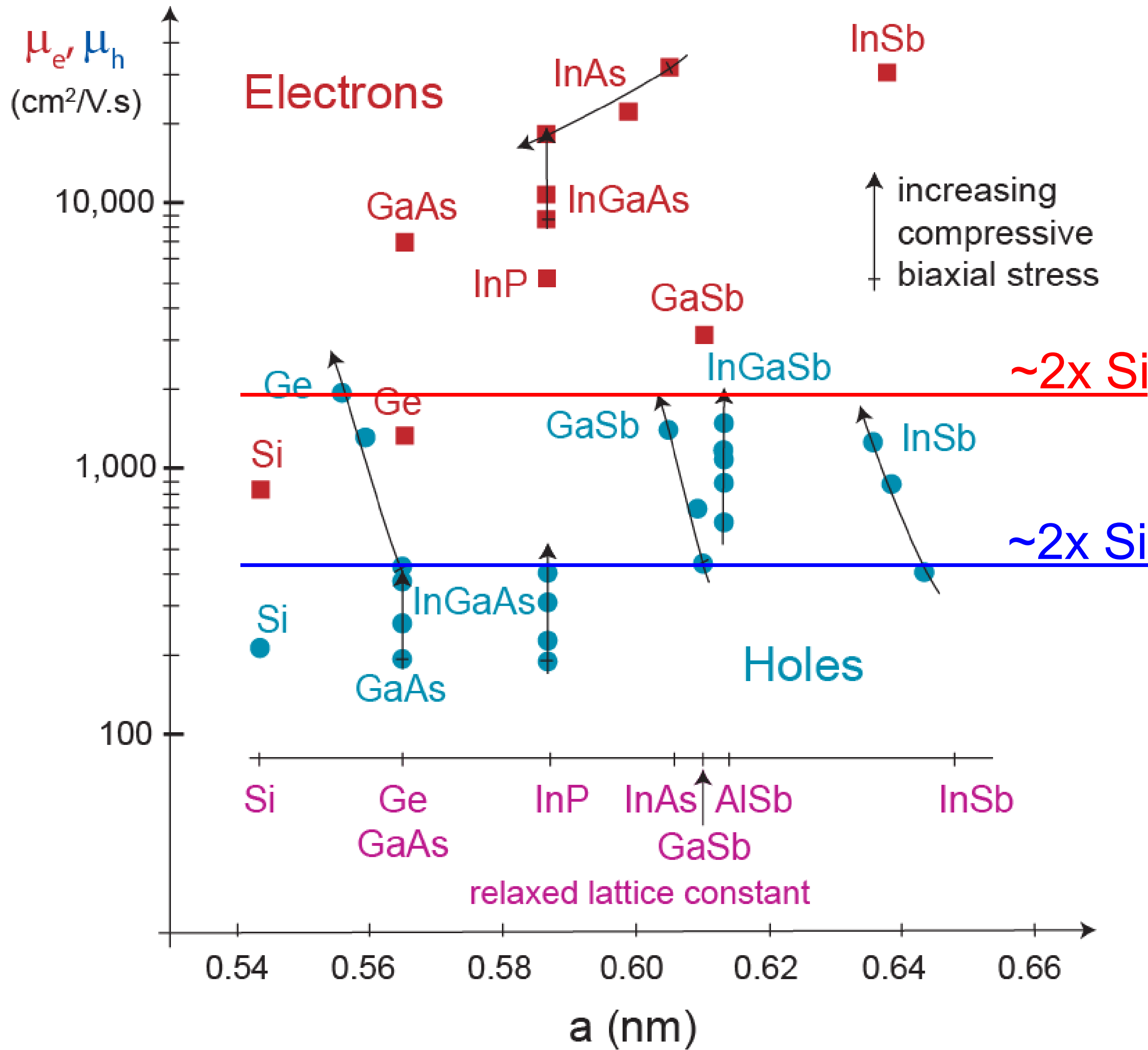
The role of compressive biaxial strain



InAs: hurts nFET (need tensile strain)

Ge, GaSb, InSb: big pFET improvement (μ>1,000 cm^2.V.s)

What about ternary III-Vs?

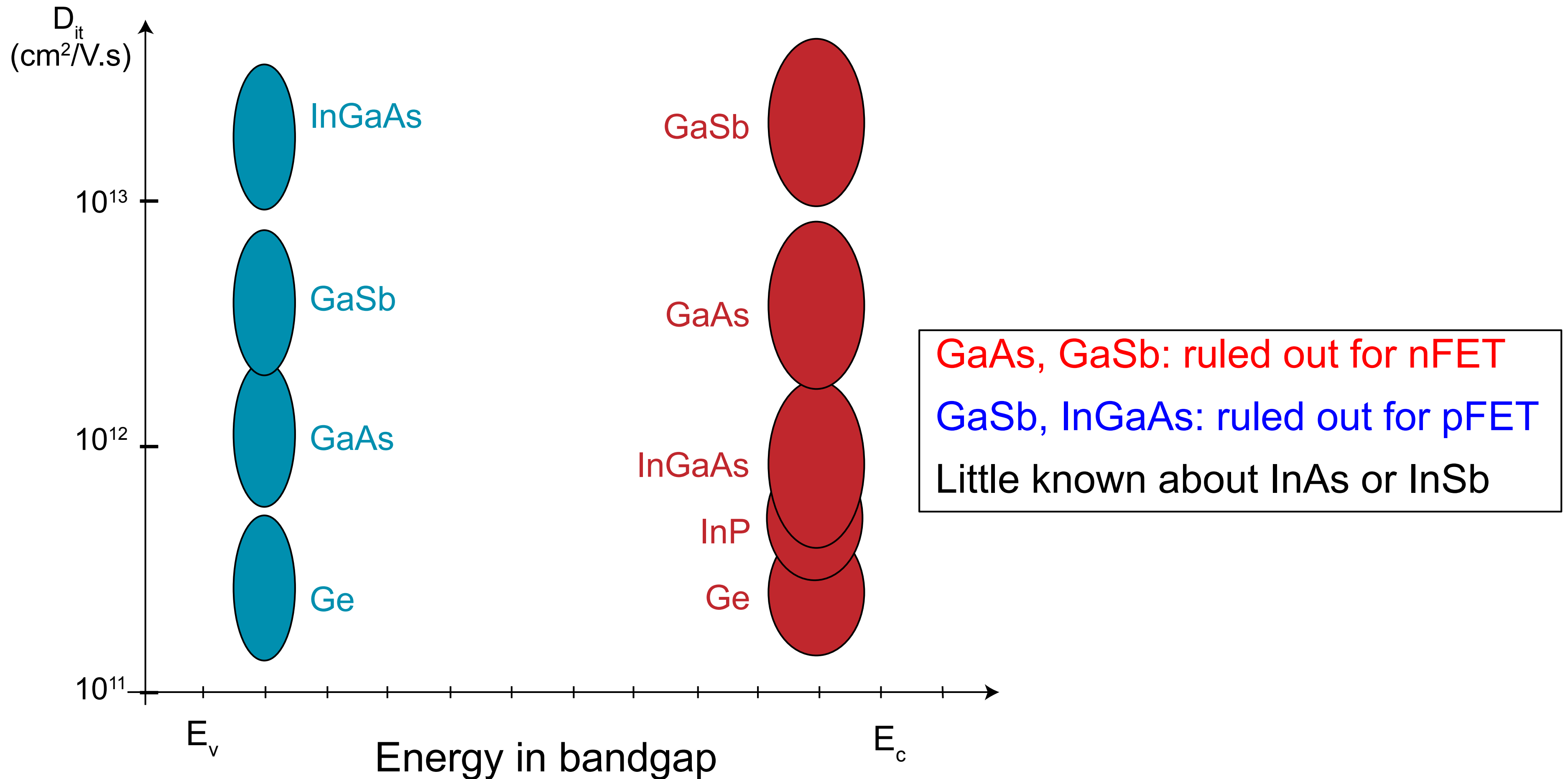


InGaAs: promising for nFET

InGaSb: promising for pFET

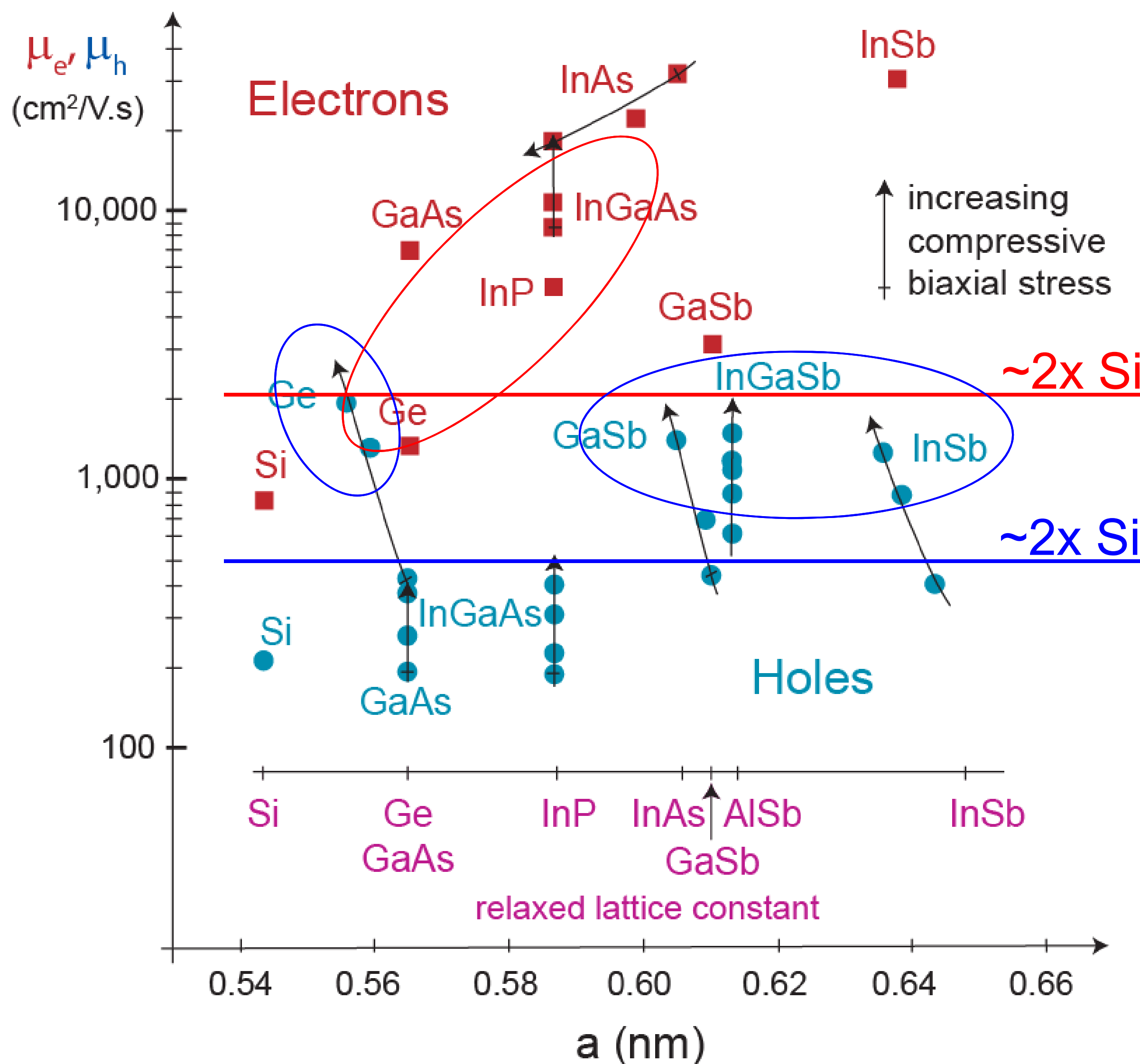
InGaAs: borderline for pFET

D_{it} close to band edges



Buried-channel structures still possible for narrow-bandgap materials but need to provide appropriate band discontinuity

Options for post-Si CMOS



InGaAs nFET
InP nFET
Ge nFET
InGaSb pFET
Ge pFET

Different lattice constants for n-channel and p-channel devices (except for Ge)

3. What have we learned from III-V HEMTs?

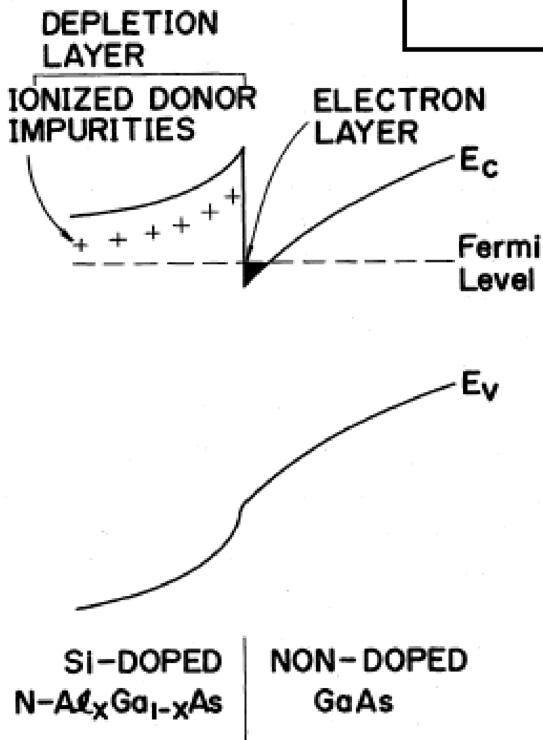
The High Electron Mobility Transistor is now >30 years old!

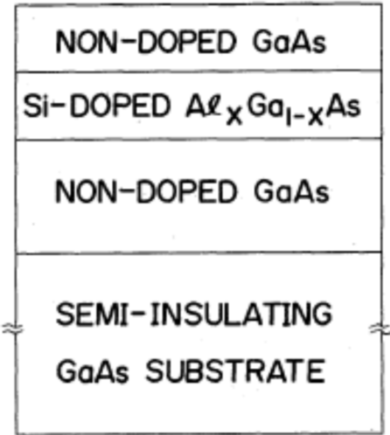
A New Field-Effect Transistor with Selectively Doped GaAs/n-$Al_xGa_{1-x}As$ Heterojunctions

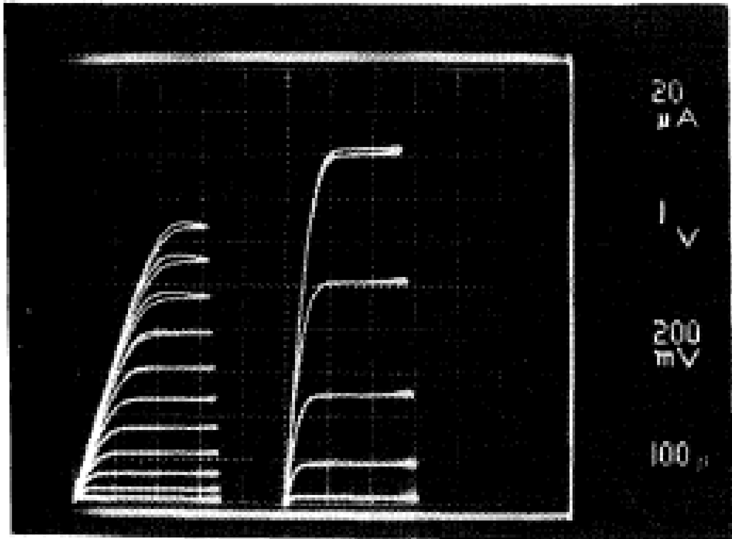
Takashi MIMURA, Satoshi HIYAMIZU, Toshio FUJII and Kazuo NANBU

Fujitsu Laboratories Ltd., 1015, Kamikodanaka, Nakahara-ku, Kawasaki 211

(Received March 24, 1980)





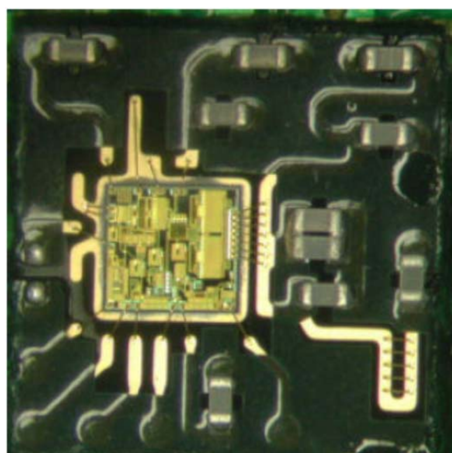


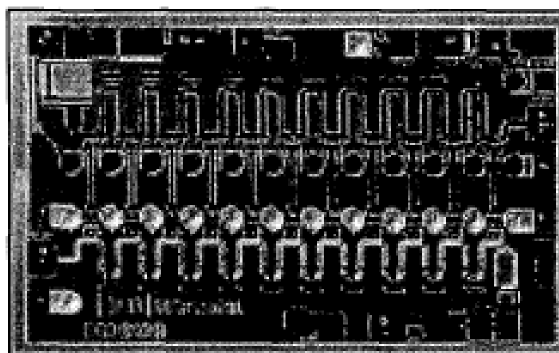
Mimura, JJAPL 1980

PHEMT ICs

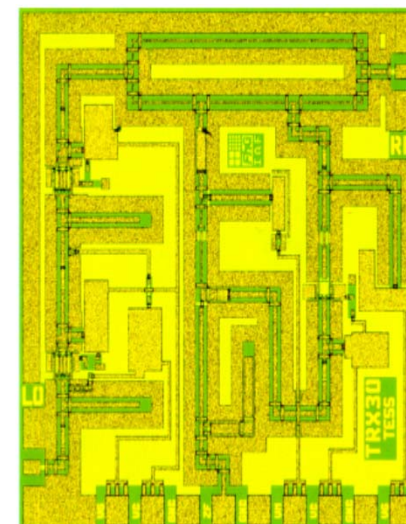
Saturday, February 26, 2011
TriQuint and Skyworks Power iPhone 5

UMTS-LTE PA module
Chow, MTT-S 2008

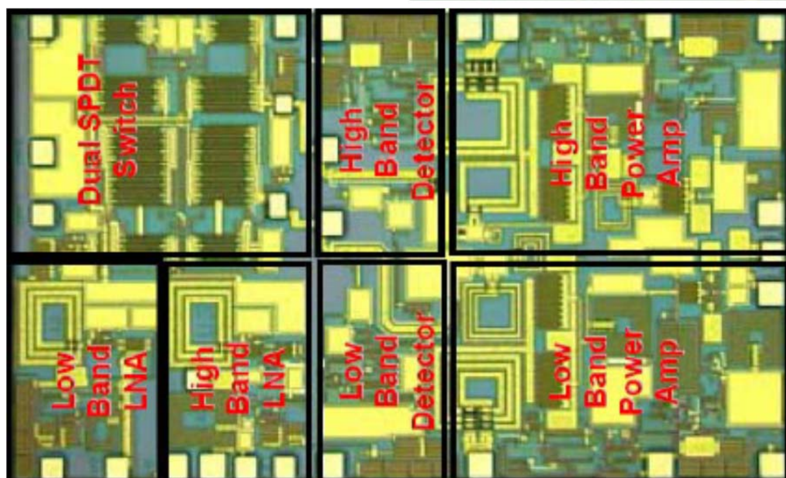




40 Gb/s modulator driver
Carroll, MTT-S 2002

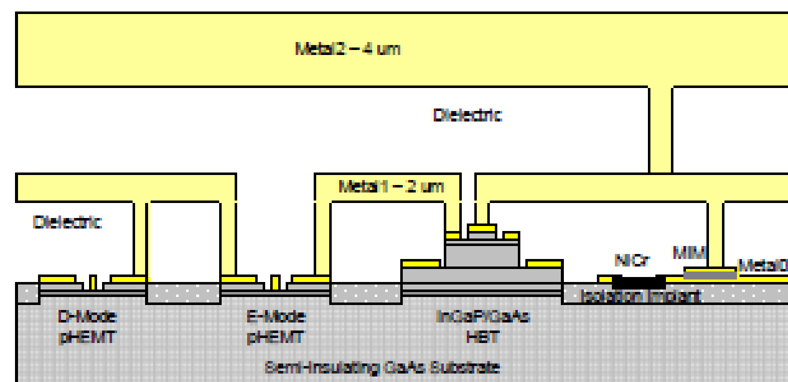


77 GHz transceiver
Tessmann, GaAs IC 1999



Single-chip WLAN MMIC, Morkner, RFIC 2007

Bipolar/E-D PHEMT process

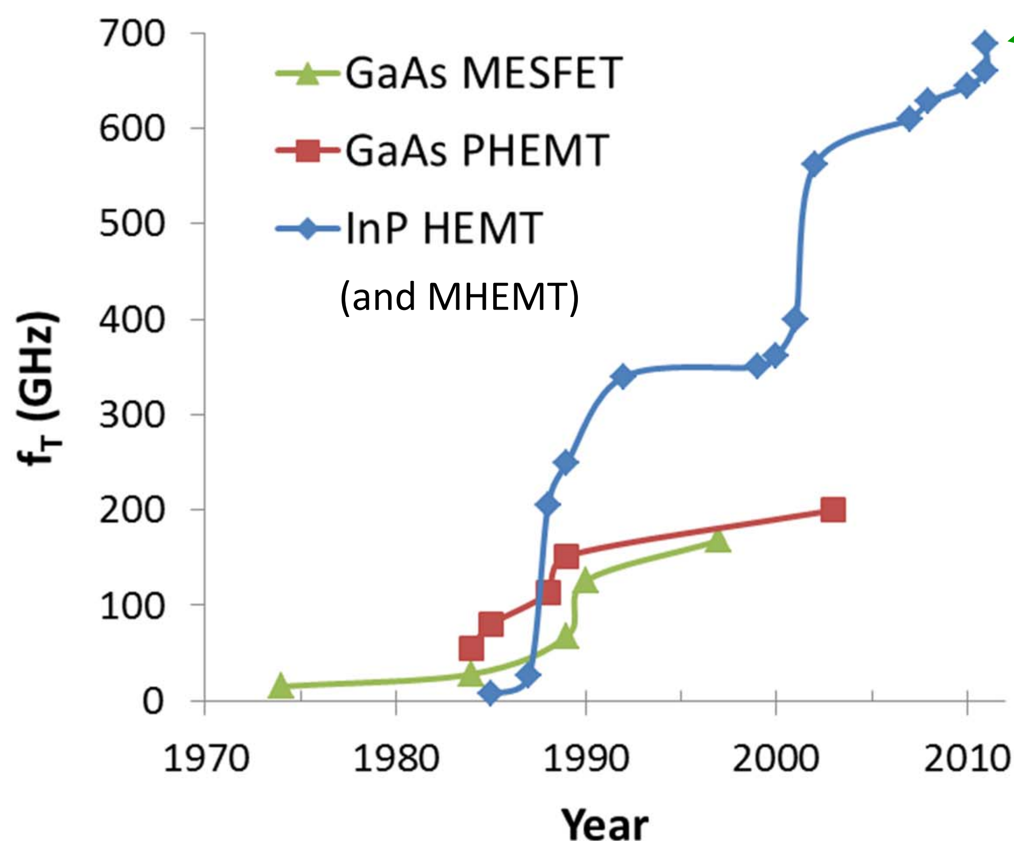


Henderson, Mantech 2007

PHEMT MMIC market=$1.2B in 2011

Near-THz III-V FETs

f_T in III-V FETs vs time:



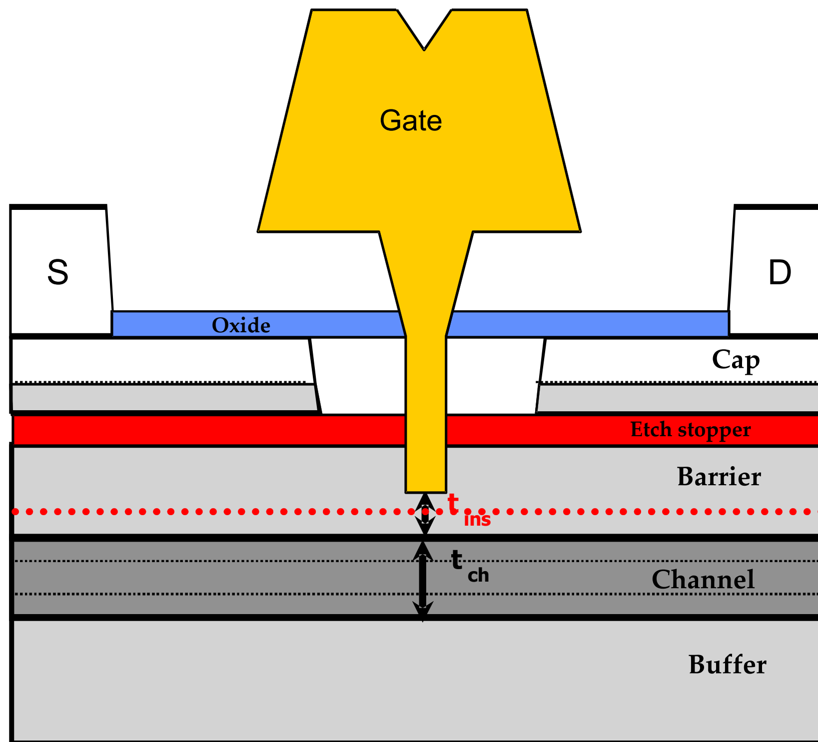
Current record:
f_T=688 GHz
f_{max}=800 GHz
Kim IEDM 2011
(Teledyne/MIT)

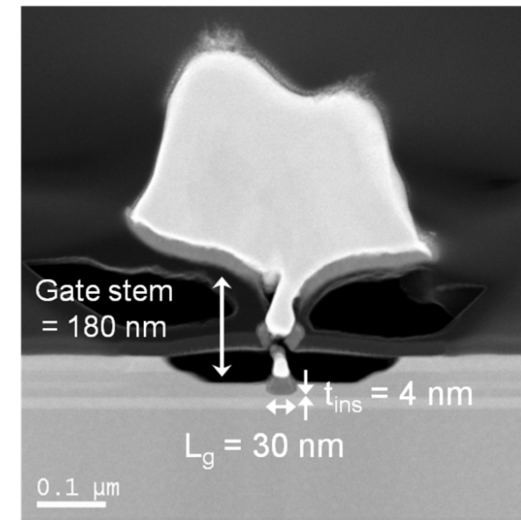
Current f_{max} record:
f_{max}=1.25 THz
Kim IEDM 2010
(Teledyne/MIT)

- For >20 years, record f_T obtained on InGaAs-channel HEMTs
- InGaAs-channel HEMTs offer record of balanced f_T and f_{max}

III-V HEMTs: excellent model system to explore logic suitability of III-Vs

State-of-the-art: InAs HEMTs



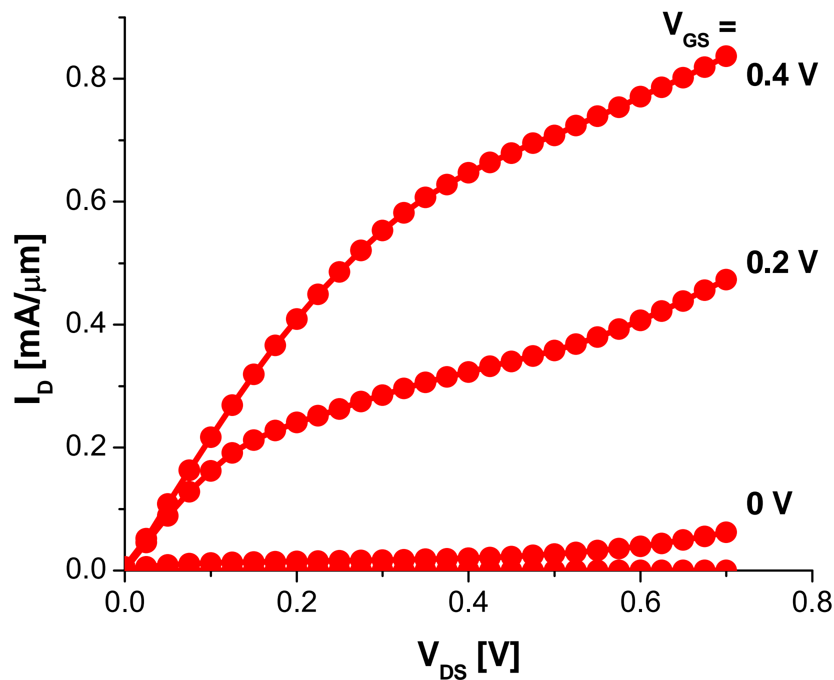


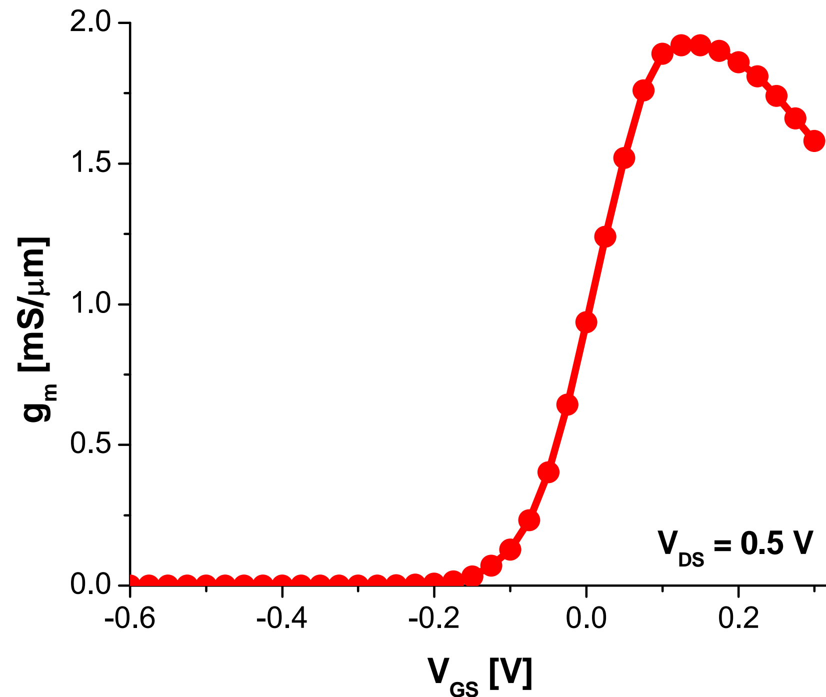
- QW channel (t_{ch}=10 nm):
  - InAs core (t_{InAs} = 5 nm)
  - InGaAs cladding
- $\mu_{n,Hall}$=13,200 cm^2/V-sec
- InAlAs barrier (t_{ins}=4 nm)
- Ti/Pt/Au Schottky gate
- L_g=30 nm

Kim, EDL 2010

L_g=30 nm InAs HEMT

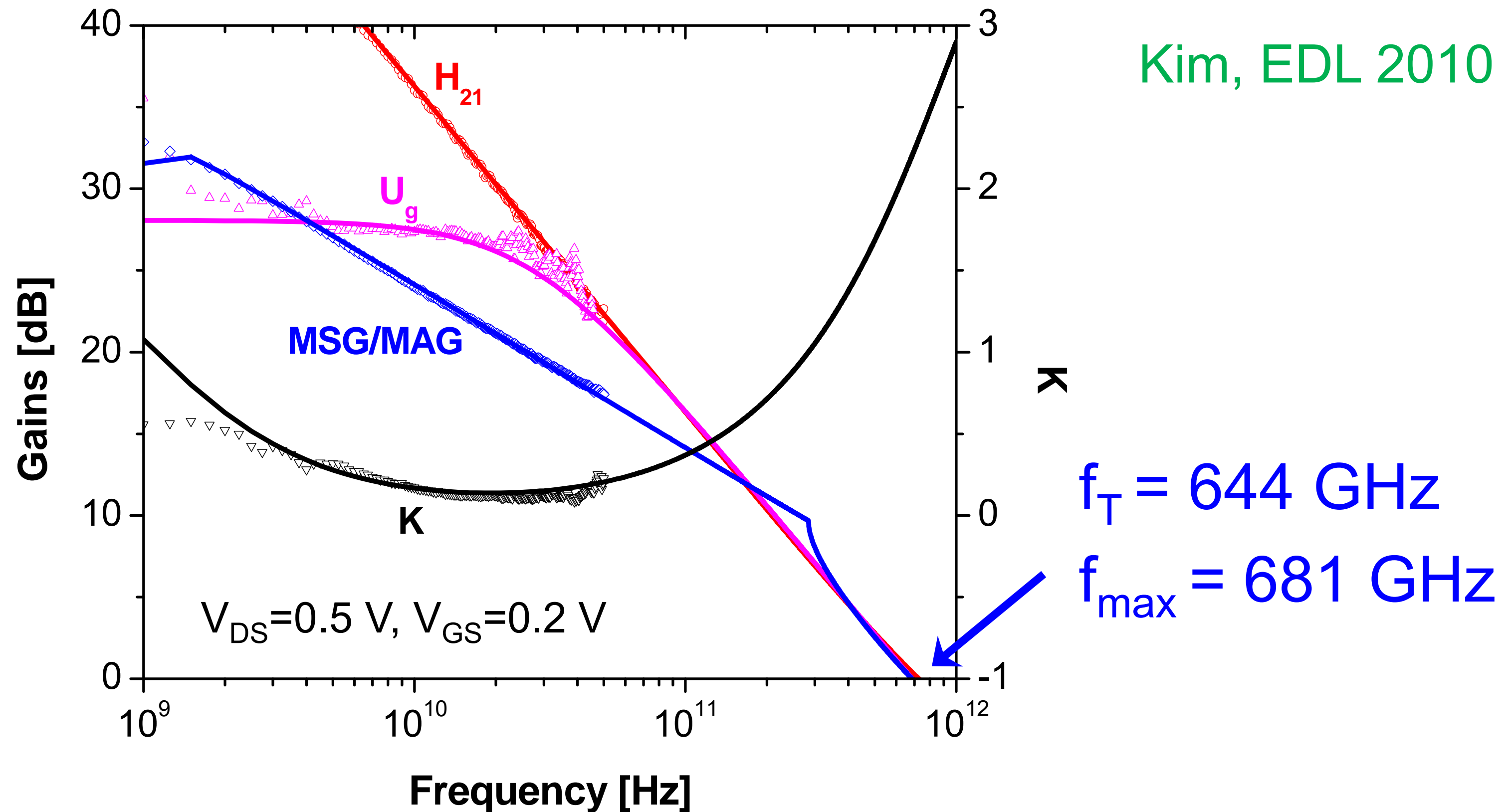
Kim, EDL 2010





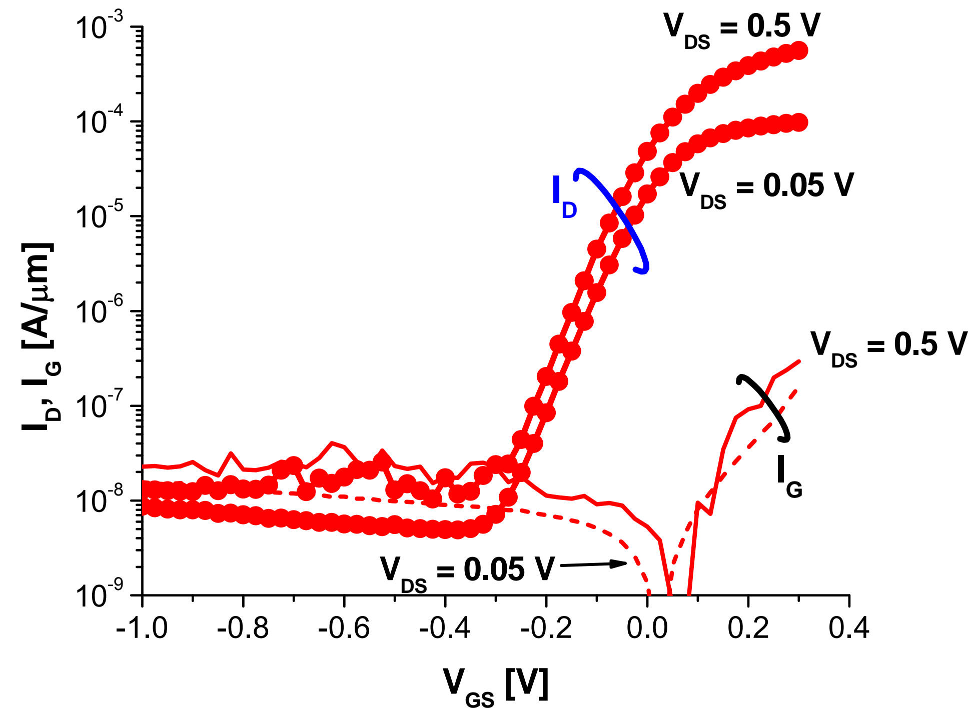
- Large current drive: I_{ON}>0.5 mA/μm at V_{DD}=0.5 V
- High transconductance: g_{mpk}= 1.9 mS/μm at V_{DD}=0.5 V
- V_T = -0.15 V, R_S=190 ohm.μm

L_g=30 nm InAs HEMT



- First transistor of any kind with both f_T and f_{max} > 640 GHz
- Current record is f_T, f_{max} > 688 GHz from Teledyne/MIT collaboration (Kim, IEDM 2011)

30 nm InAs HEMT – Logic characteristics

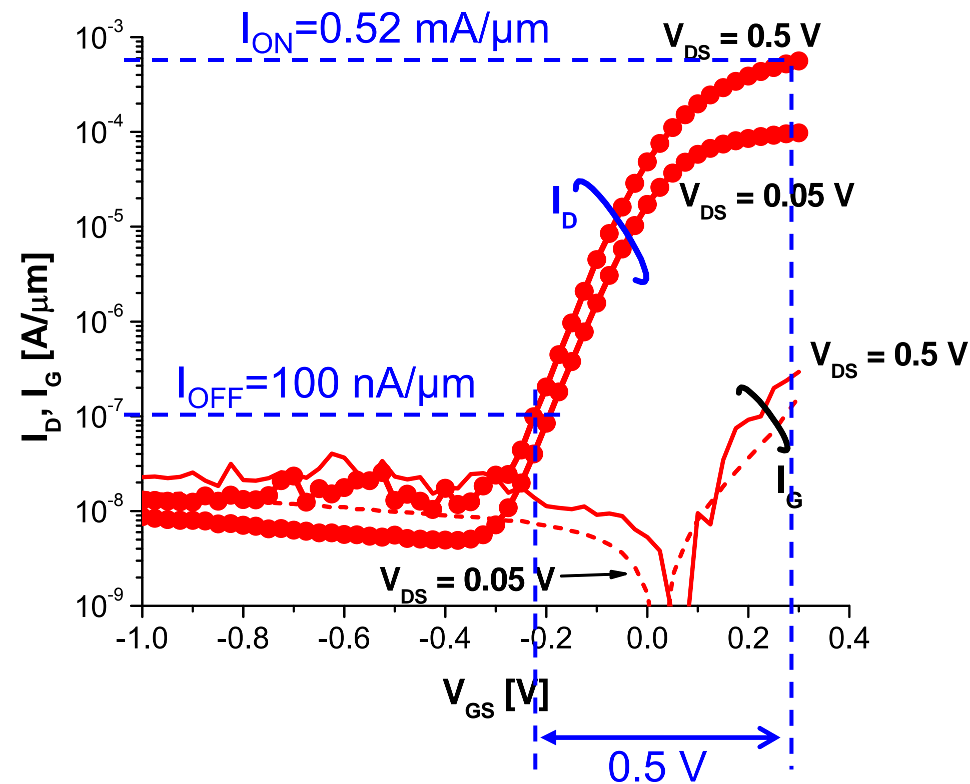


- S = 74 mV/dec, DIBL = 80 mV/V

Kim, EDL 2010

30 nm InAs HEMT – Logic characteristics

Kim, EDL 2010

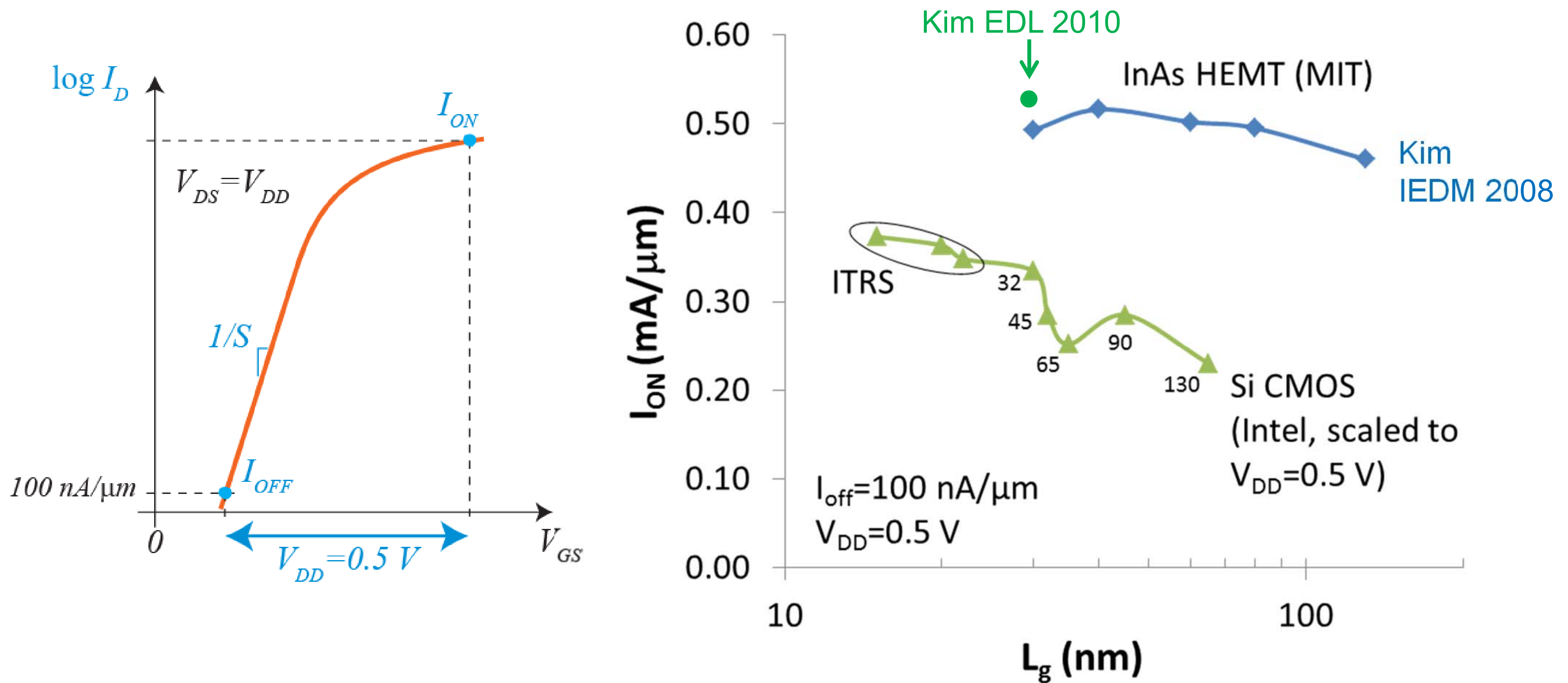


- S = 74 mV/dec, DIBL = 80 mV/V
- At I_{OFF}=100 nA/μm and V_{DD}=0.5 V, I_{ON}=0.52 mA/μm

InAs HEMTs: Benchmarking with Si

FOM that integrates short-channel effects and transport:

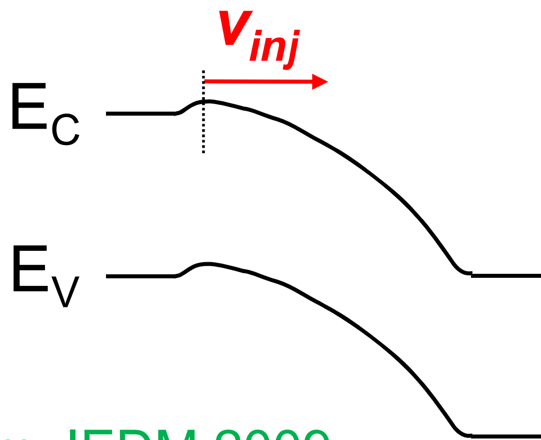
I_{ON} @ I_{OFF}=100 nA/μm, V_{DD}=0.5 V



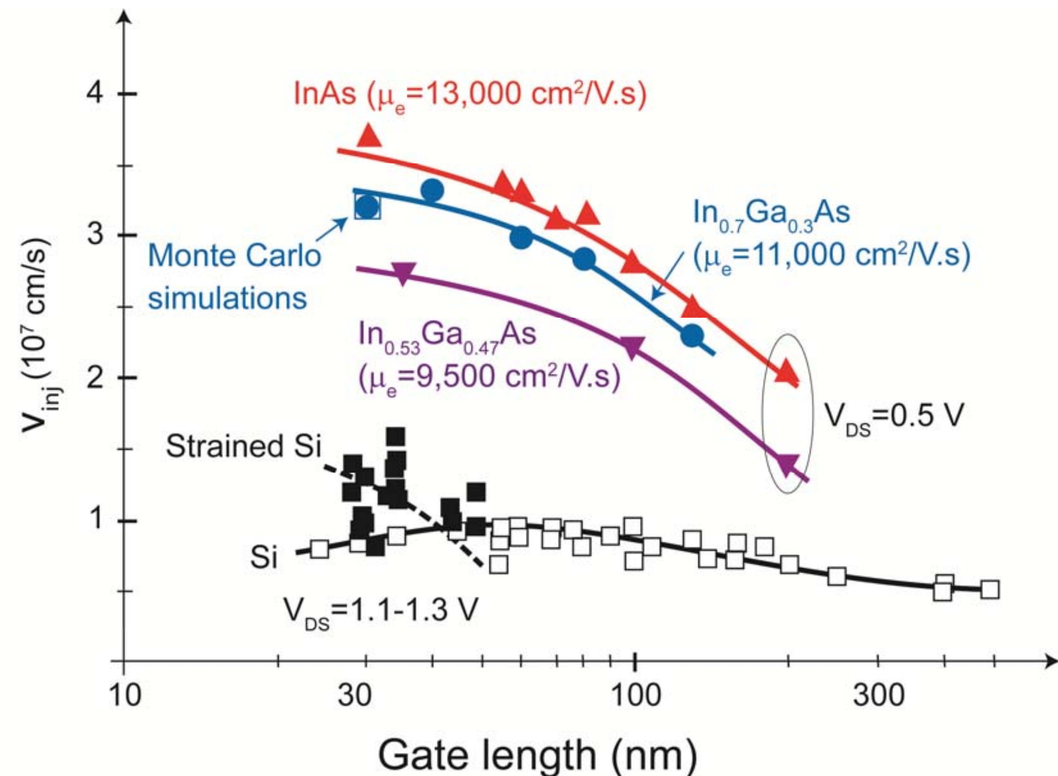
InAs HEMTs: higher I_{ON} for same I_{OFF} than Si. Why?

Why high I_{ON}?

1. Very high electron injection velocity at the virtual source



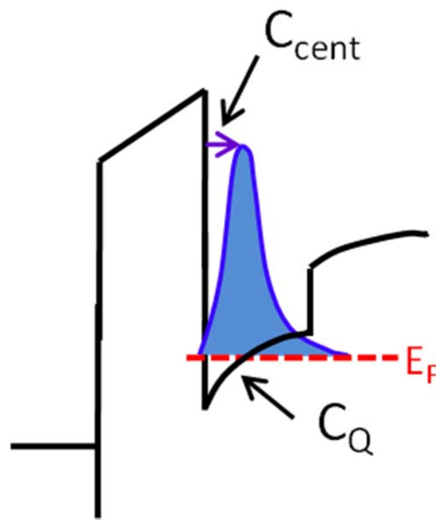
Kim, IEDM 2009
Liu, Springer 2010
Khakifirooz, TED 2008
del Alamo, Nature 2011



- v_{inj}(InGaAs) increases with InAs fraction in channel
- v_{inj}(InGaAs) > $2v_{inj}$(Si) at less than half V_{DD}
- ~100% ballistic transport at L_g~30 nm

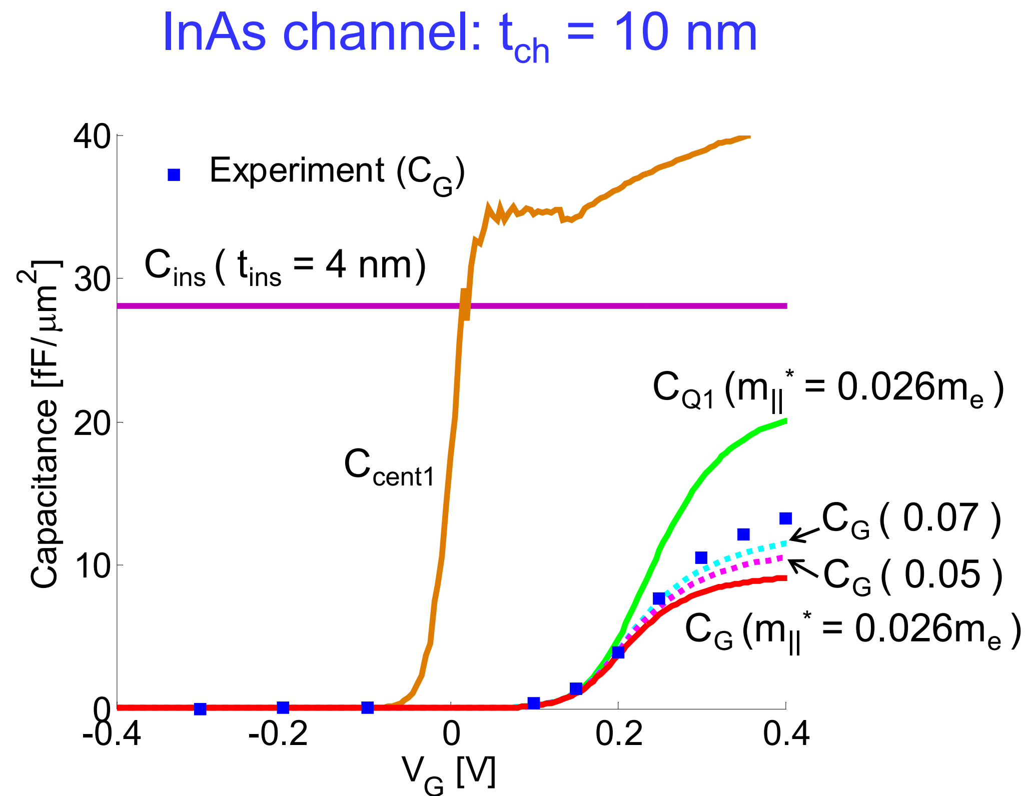
Why high I_{ON}?

2. Quantum capacitance less of a bottleneck than previously believed



Jin, IEDM 2009

InAs channel: t_{ch} = 10 nm

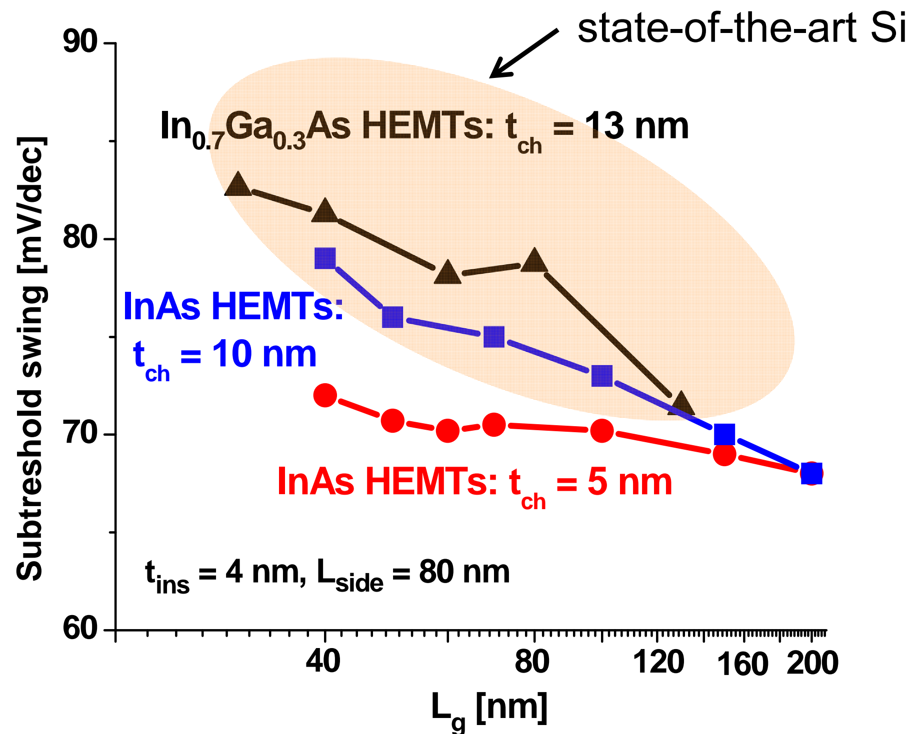


Biaxial strain + non-parabolicity + strong quantization:

$$m_{||}^* \uparrow \rightarrow C_G \uparrow \rightarrow n_s \uparrow \rightarrow I_{ON} \uparrow$$

Why high I_{ON}?

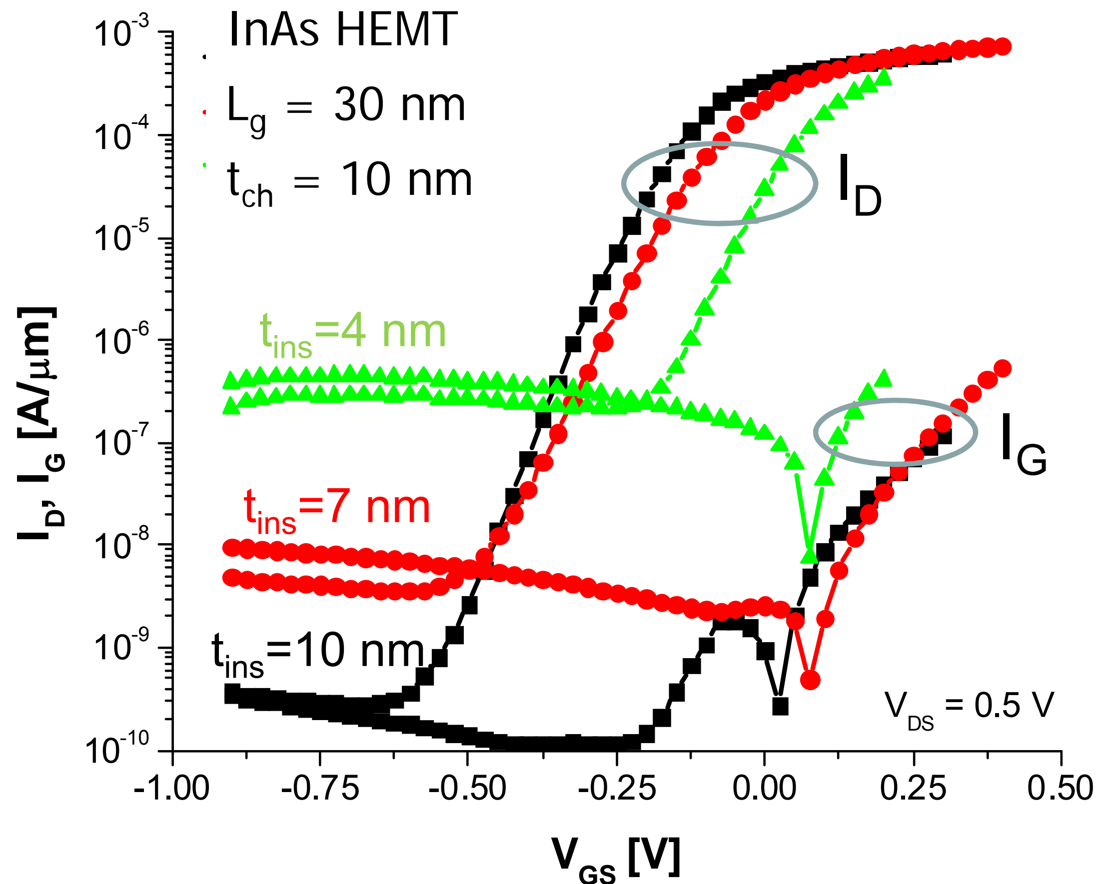
3. Sharp subthreshold swing due to quantum-well channel

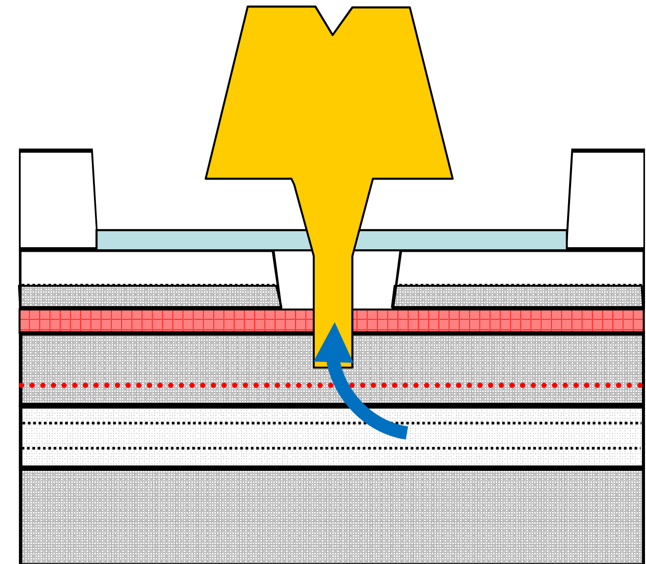


Kim, IPRM 2010

- Dramatic improvement in short-channel effects with thin channel
- Thin channel does not degrade v_{inj} at L_g~40 nm (Kim, IPRM 2011)

Limit to III-V HEMT Scaling: Gate Leakage Current





del Alamo. IPRM 2011

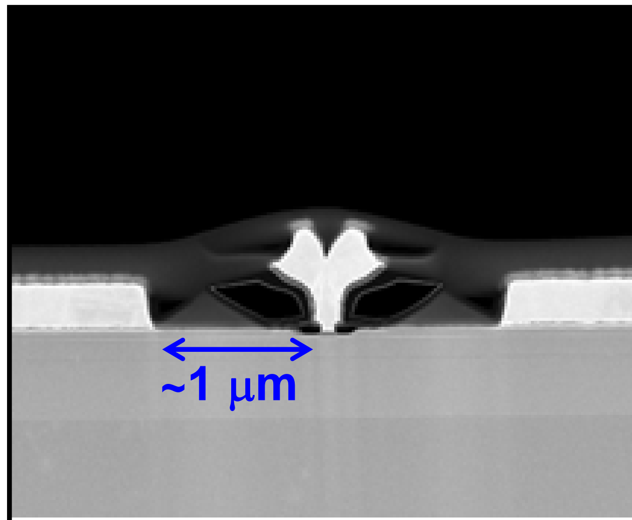
$t_{ins}\downarrow \rightarrow I_G\uparrow$

→ Further scaling requires high-K gate dielectric

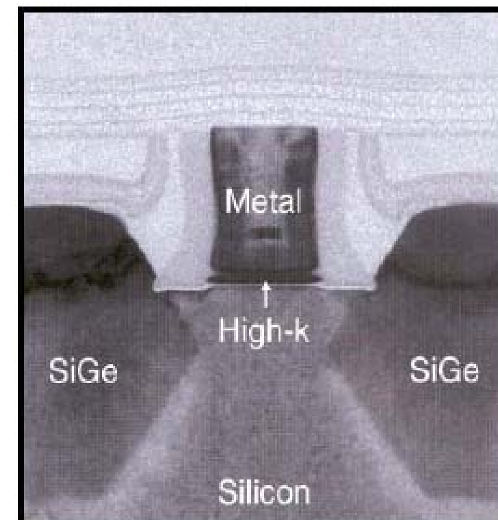
4. III-V CMOS: device design and challenges

Modern III-V HEMT vs. modern Si MOSFET:

III-V HEMT



Intel's 45 nm CMOS



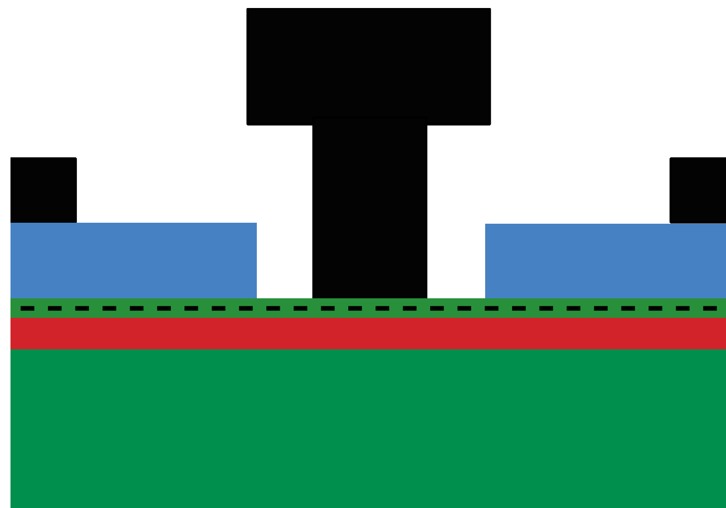
- What do we preserve?
- What do we change?

III-V CMOS: HEMT features worth preserving

- Quantum-well channel: key to scalability
- Undoped channel:
- InAs-rich channel:
- Buried-channel design:

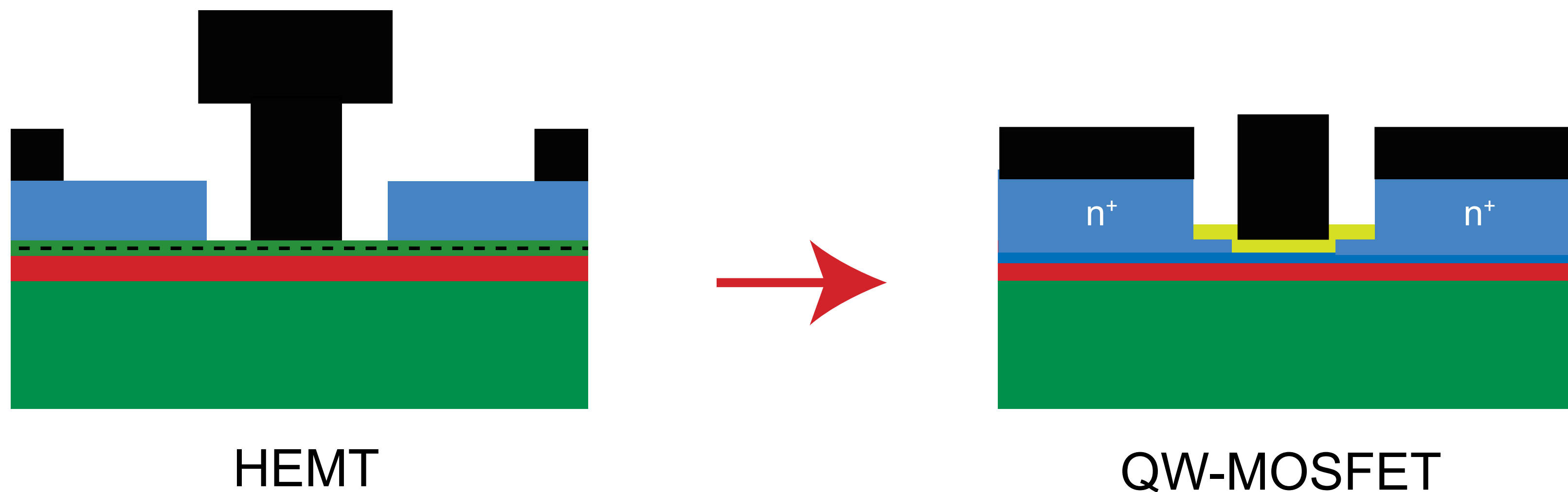
} for high mobility and velocity

- Raised source and drain regions: essential for scalability
- Undoped QW channel in extrinsic regions: key to low access resistance



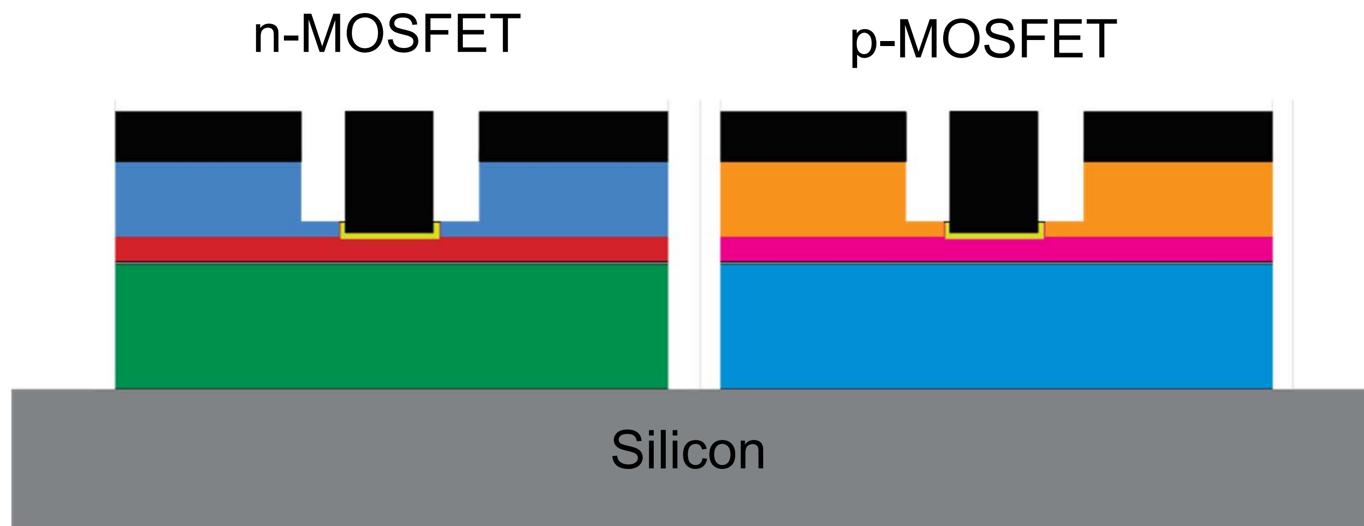
III-V CMOS:
HEMT features to change

- Schottky gate: need MOS gate with very thin high-K dielectric
- T-gate: need rectangular gate
- Barrier under contacts: need to eliminate
- Alloyed ohmic contacts: change to refractory ohmic contacts
- Source and drain contacts: need self-aligned with gate
- Footprint: need to reduce by 1000x!



III-V CMOS:
other critical issues

- p-channel MOSFET: with performance >1/3 that of n-MOSFET
- Co-integration of n-FET and p-FET on Si: compact, planar surface
- Sub-10 nm MOSFET architectures



What can we expect from ~10 nm III-V NMOS at 0.5 V?

Focus on I_{ON} for fixed I_{OFF} as FOM.

Simple model:

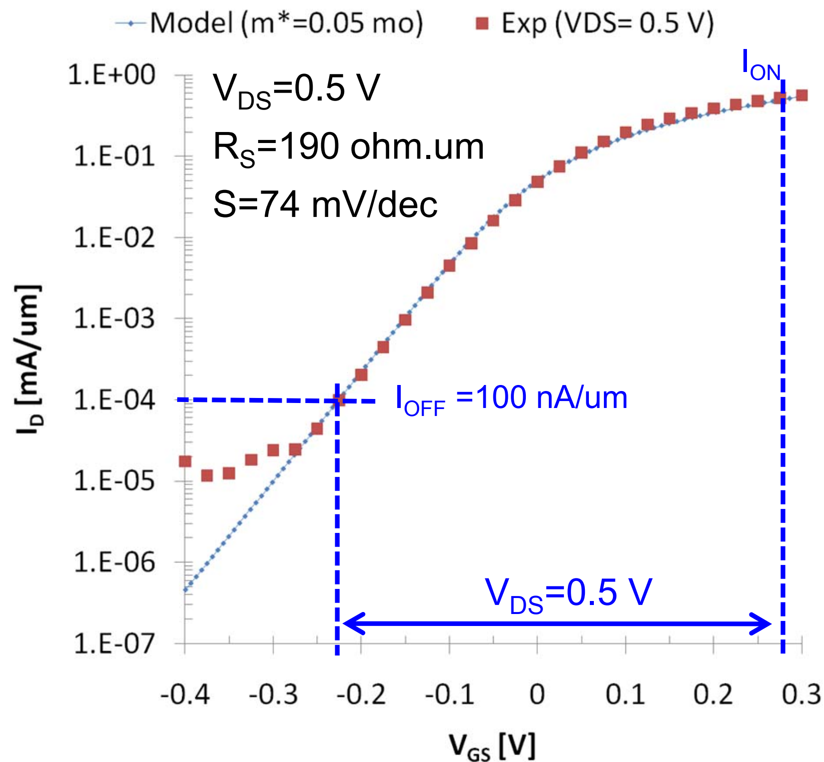
- Q-V characteristics from Poisson-Schrodinger simulations (from subthreshold to strong inversion)
- 2D ballistic velocity model (1 subband):

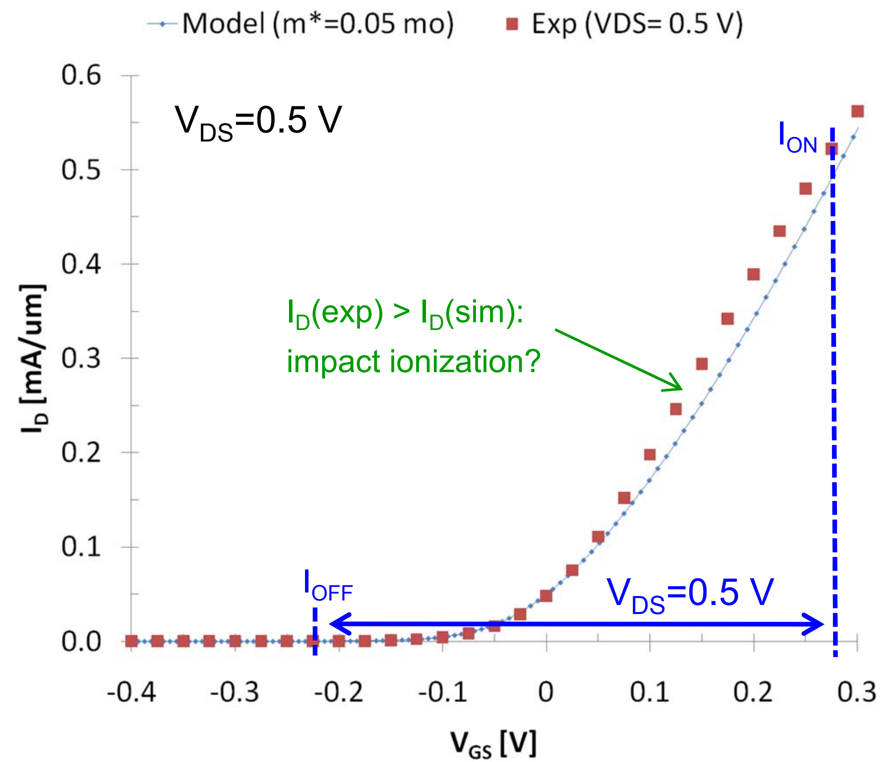
$$v_{inj} = \sqrt{\frac{2kT}{\pi m^*}} \frac{\mathcal{F}_{1/2}\left(\frac{E_F - E_1}{kT}\right)}{\mathcal{F}_0\left(\frac{E_F - E_1}{kT}\right)}$$

Lundstrom, TED 2002

- Add channel capacitance to match experimental S
- Add ohmic drop on experimental R_S
- No adjustable parameters beyond $m^*=0.05\ m_o$
- Did not attempt to match V_T

Model validation: I-V characteristics of 30 nm InAs HEMT

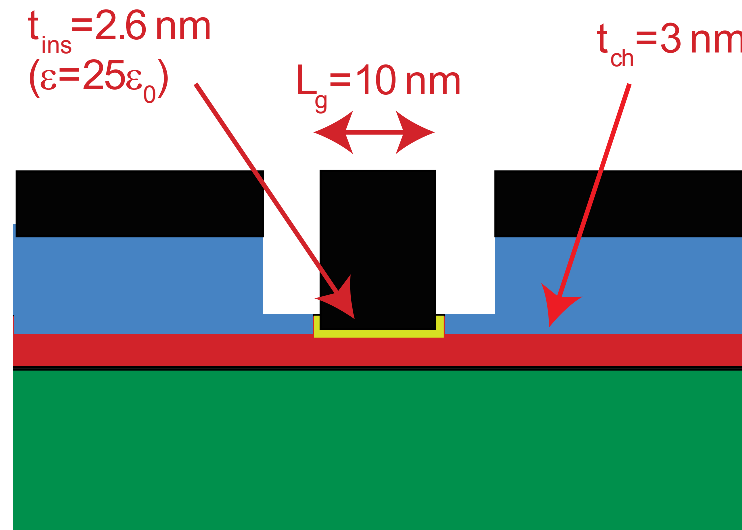




- Excellent agreement through nearly five orders of magnitude of I_D
- Residual disagreement due to impact ionization?

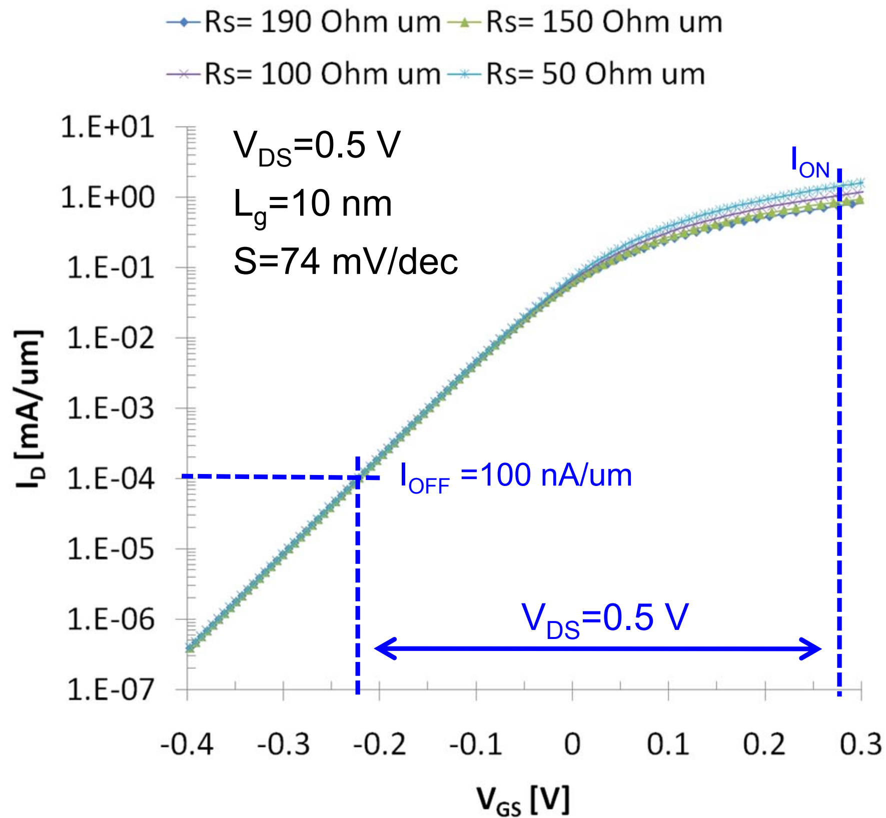
Projection to ~10 nm InAs NMOS at 0.5 V

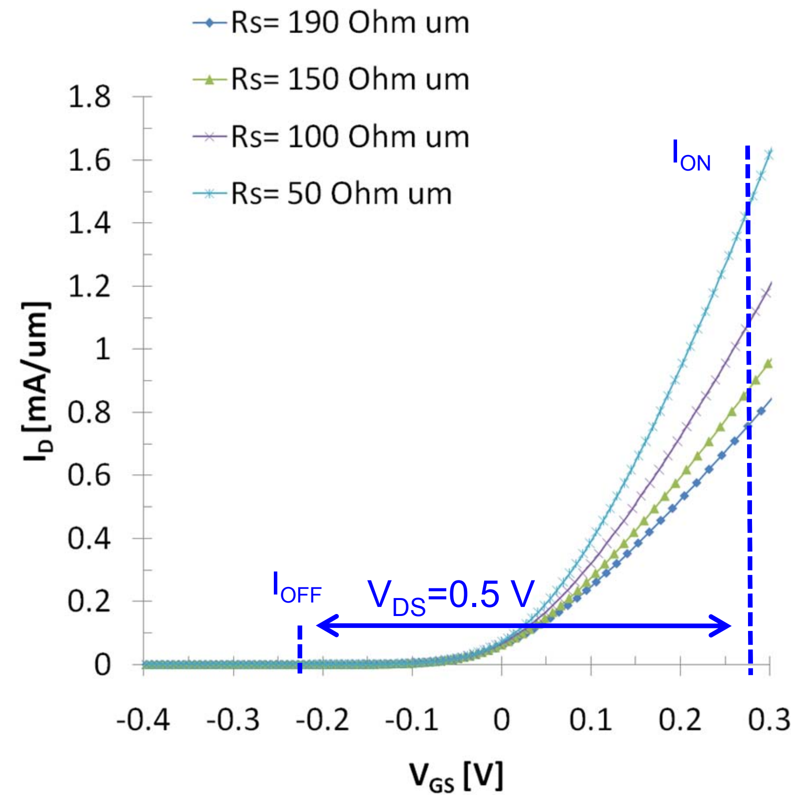
Scale experimental 30 nm InAs HEMT by about 3x:



- Q-V characteristics from Poisson-Schrodinger simulator
- Assume same short-channel effects: S=74 mV/dec
- Examine impact of R_S and D_{it}

Role of R_S



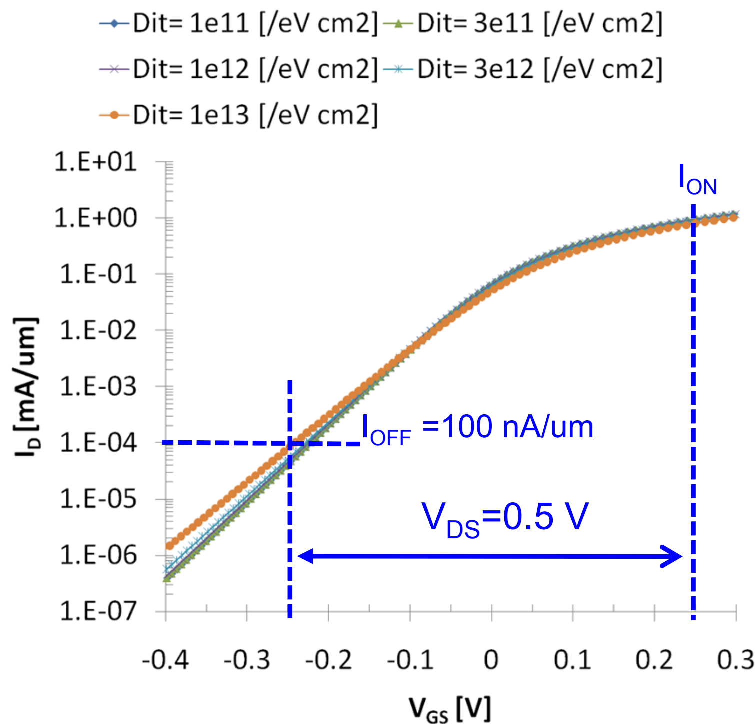


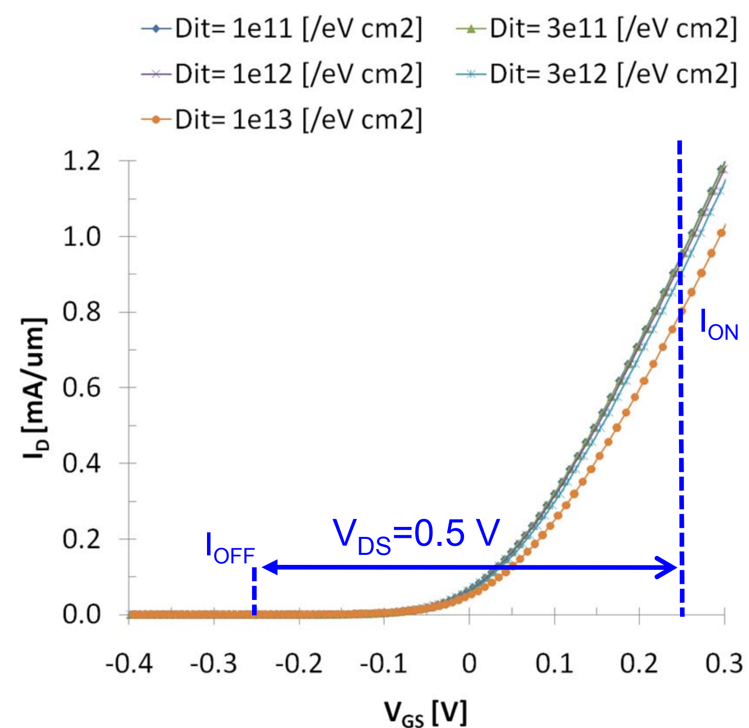
- R_S depresses I_{ON} without changing I_{OFF}
- To obtain I_{ON}>1 mA/μm, need R_S<100 Ω.μm

Role of D_{it}

Simple case: constant D_{it} throughout structure

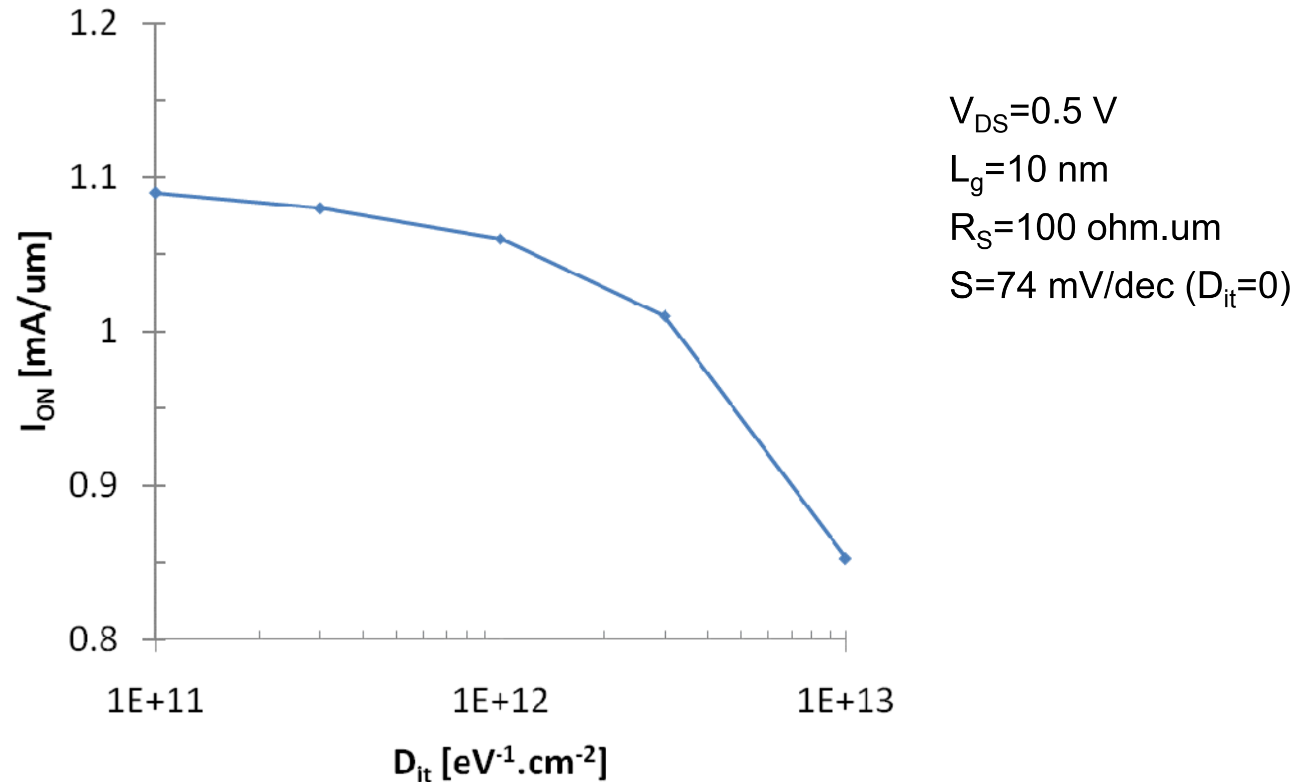
For R_S=100 ohm.um and S=74 mV/dec (for D_{it}=0):





- D_{it} in bandgap increase S → I_{ON}↓
- D_{it} inside conduction band further decrease I_{ON}

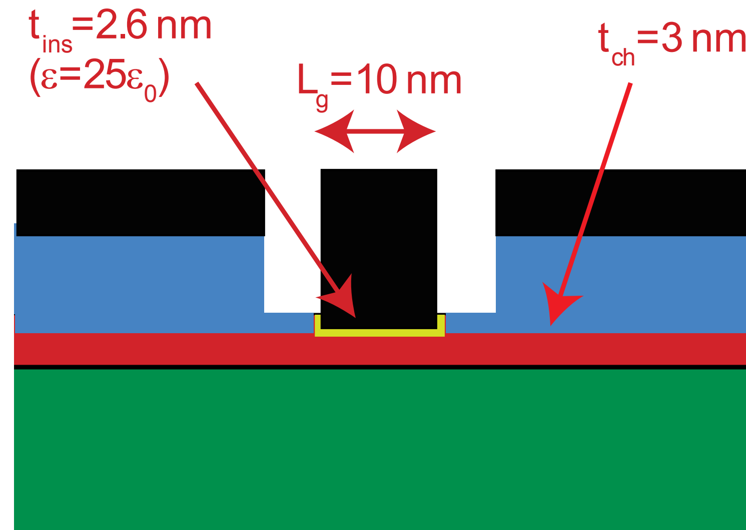
Role of D_{it}



- To obtain I_{ON}>1 mA/µm, need $D_{it}<3x10^{12}$ $eV^{-1}.cm^{-2}$
- Relative insensitivity of I_{ON} to D_{it} due to high C_{ins}:

$$C_{ins}=85\ fF/\mu m^2 \leftrightarrow D_{it}=5.3x10^{13}\ eV^{-1}.cm^{-2}$$

Assumptions/concerns



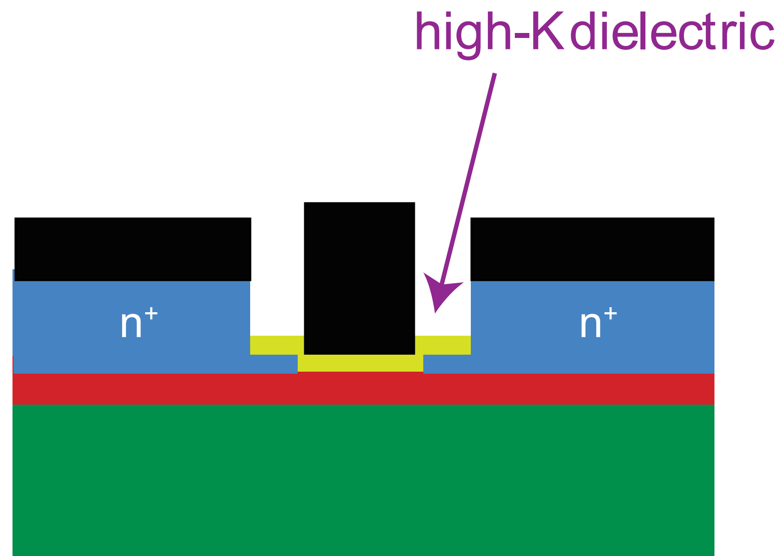
- Aggressive vertical scaling possible: EOT=0.41 nm

  [EOT ≡ equivalent oxide thickness]
- Rigid 3X shrink preserves short-channel effects
- L_{side} can be shrank without degrading SCE
- R_S<100 Ω.μm feasible at required footprint
- Ballistic transport even with high-K dielectric + thin channel

Critical issue #1: the gate stack

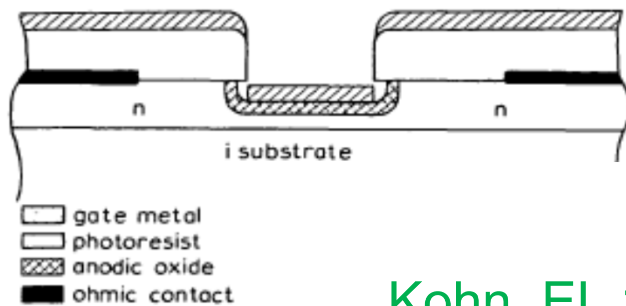
Challenge: metal/high-K oxide gate stack

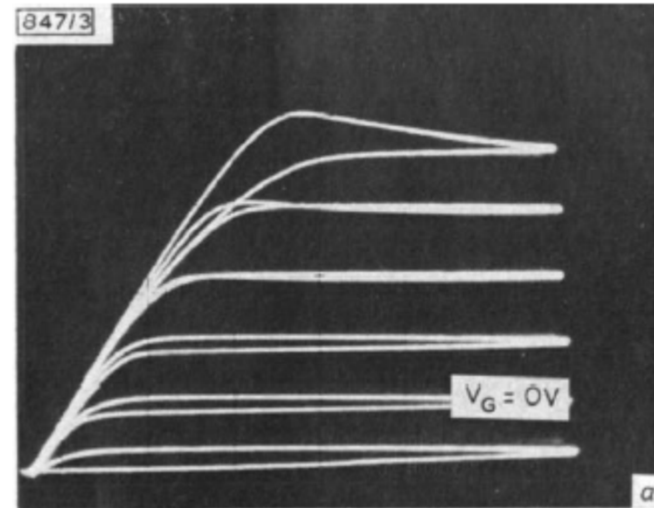
- Fabricated through *ex-situ* process
- Very thin barrier (EOT<1 nm)
- Low gate leakage (I_G<1 A/cm^2 at V_{GS}=0.5 V)
- Low D_{it} (<3x10^{12} eV^{-1}.cm^{-2} in top ~0.3 eV of bandgap and inside CB)
- Reliable



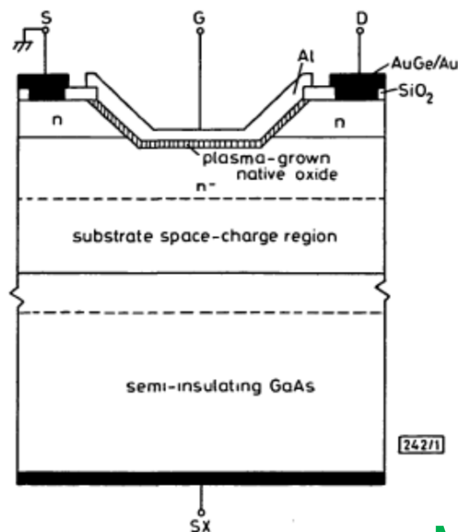
Problem: Fermi level pinning at oxide/III-V interfaces

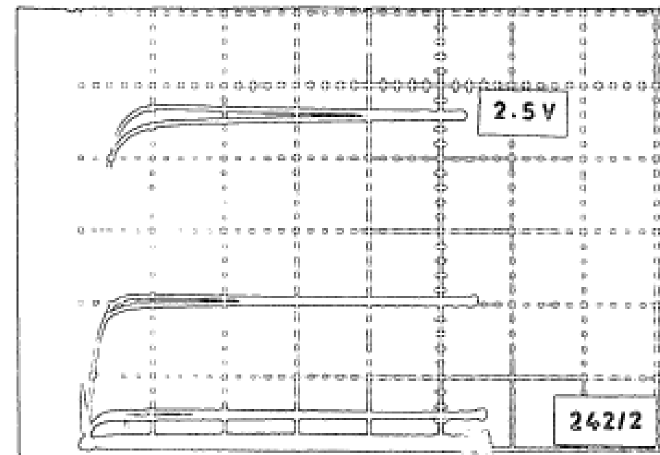
III-V MOSFET: a >40 year pursuit!





Kohn, EL 1977



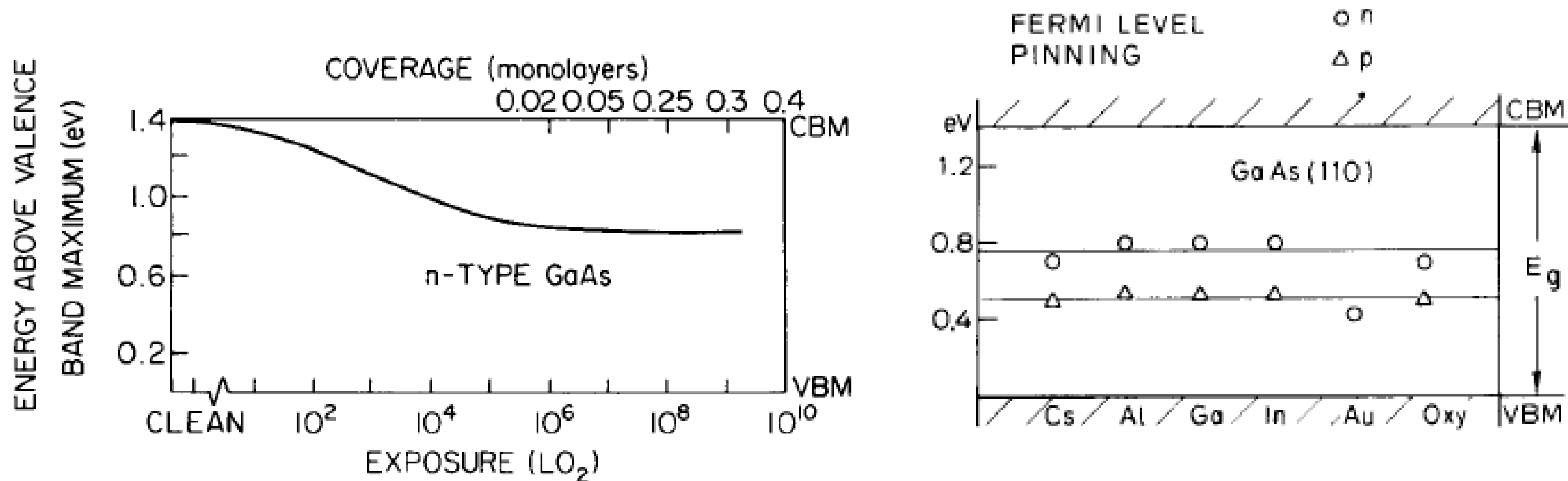


Mimura, EL 1978

Problem: Fermi level pinning at oxide/III-V interfaces

Fermi level pinning due to interfacial defects

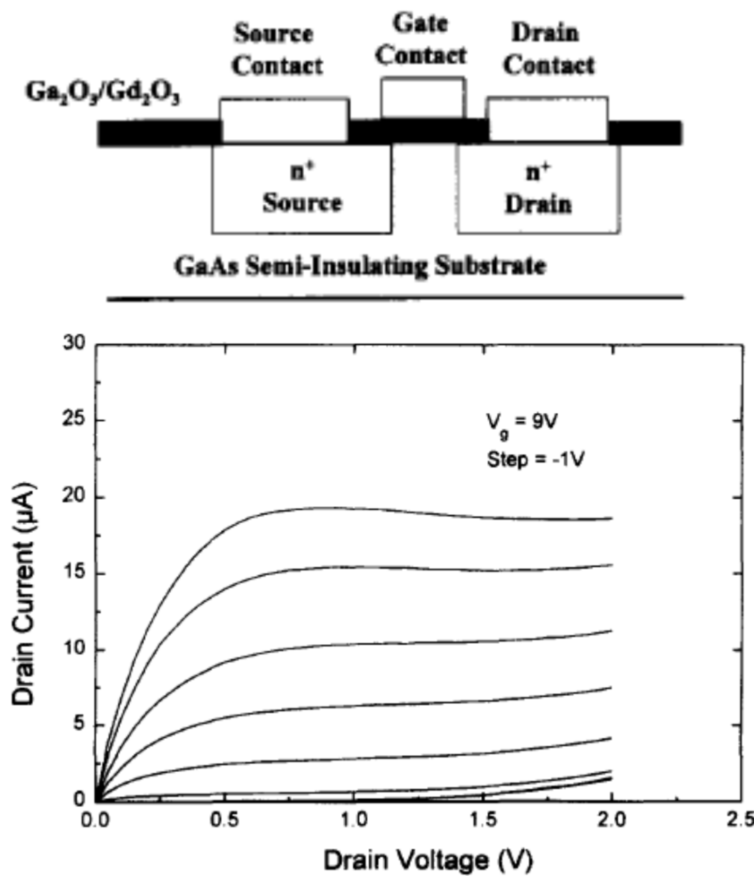
- Even 1% of a monolayer of O at GaAs surface pins E_F
- E_F pinning produced by any foreign element at GaAs surface
- E_F pinning position largely independent of surface adatom



Spicer, JVST 1979

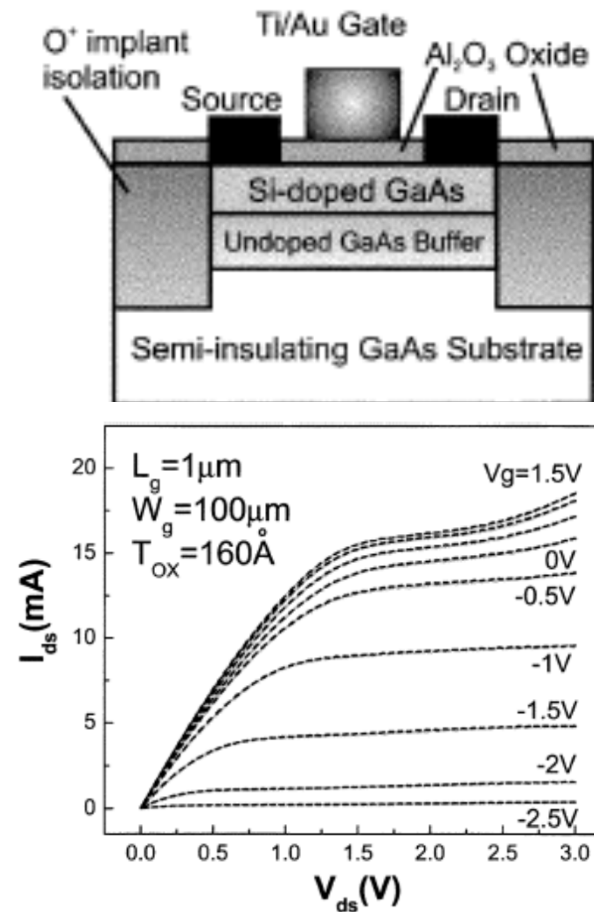
Recent breakthrough: oxide/III-V interfaces with unpinned Fermi level!

In-situ UHV Ga_2O_3-Gd_2O_3 on GaAs



Ren, SSE 1997

Ex-situ ALD Al_2O_3 on InGaAs

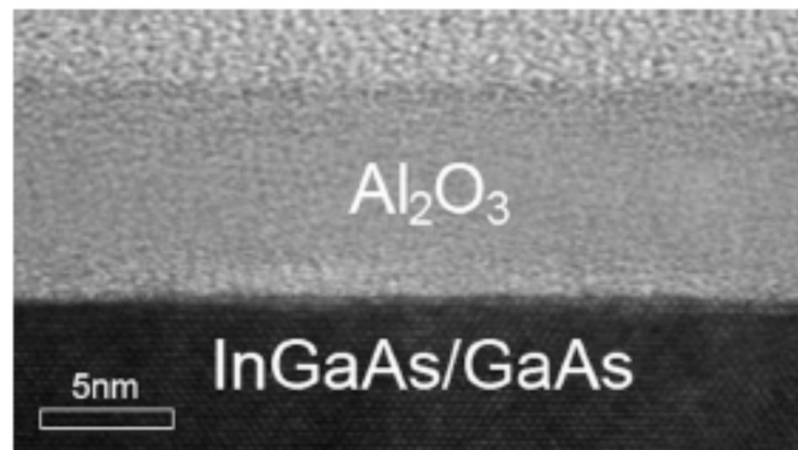


Ye, EDL 2003

"Self-cleaning" during ALD

ALD largely eliminates surface oxides responsible for Fermi level pinning:

- Occurs during first exposure of III-V surface to ALD metal source
- Surface robust to later exposure to ALD oxidant
- First observed with Al_2O_3, then with other high-K dielectrics
- First seen in GaAs, then in other III-Vs



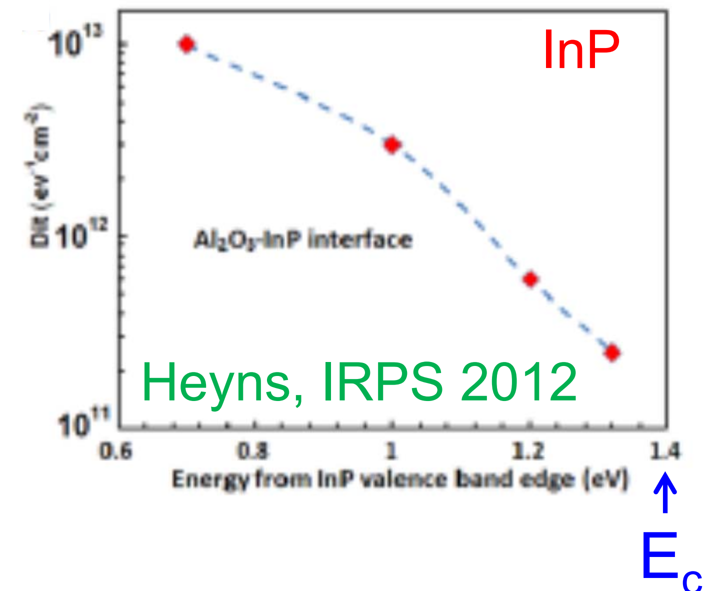
Huang, APL 2005

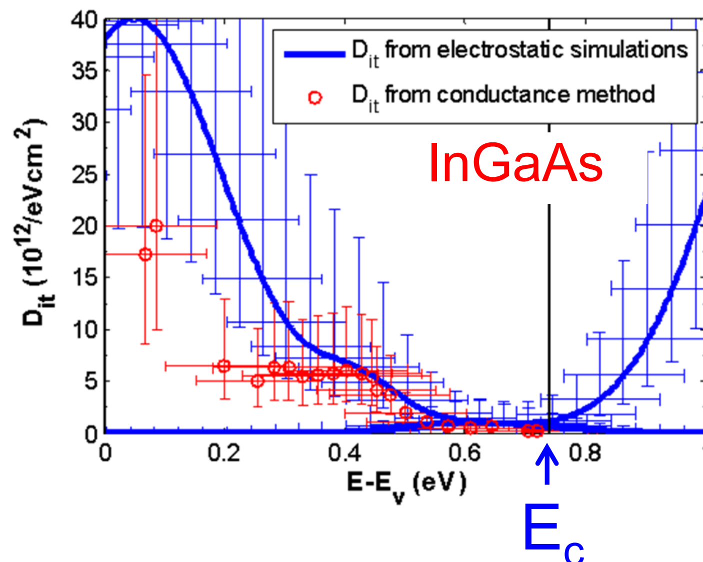
Interface state density in high-K/III-V by ALD

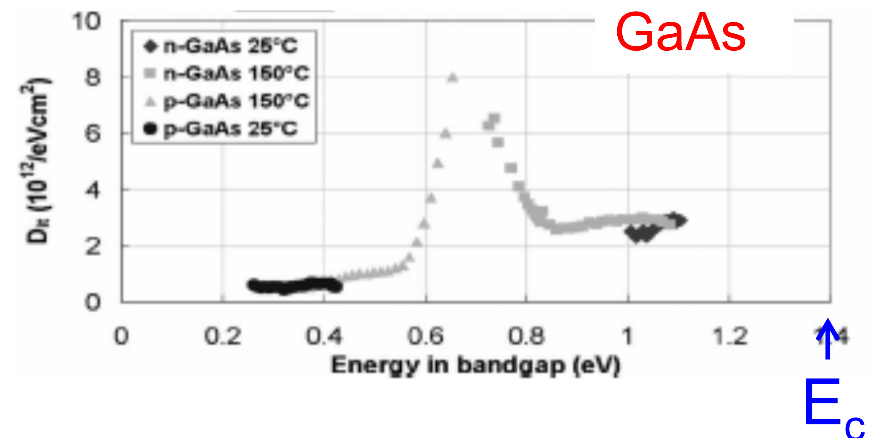
D_{it} hard to characterize → reports vary widely

General consensus for D_{it}:

- GaAs: high at midgap, medium close to E_c and E_v, large peak around midgap
- InGaAs: high close to E_v, low close to E_c
- InP: high close to E_v, very low close to E_c



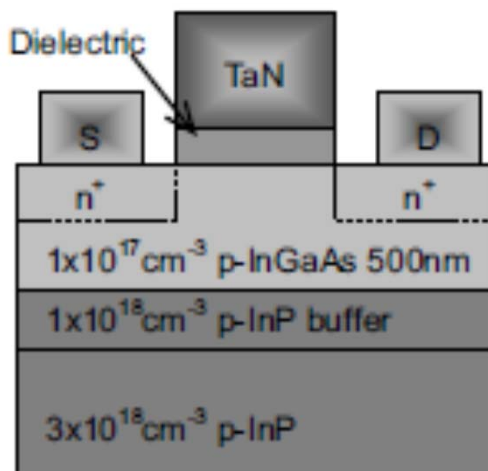


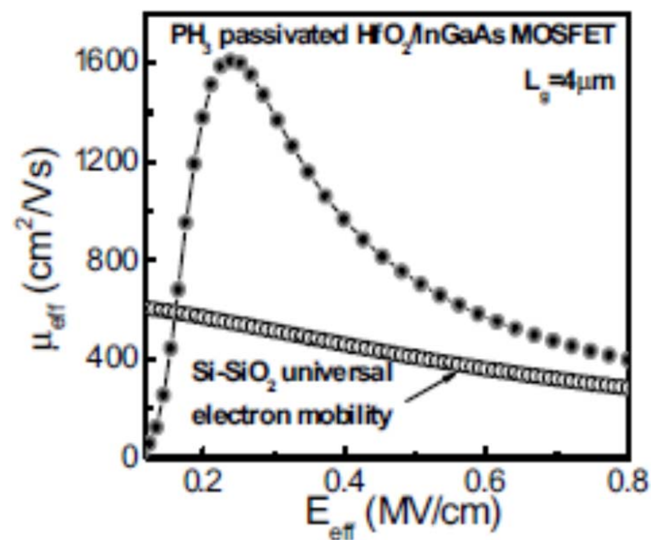


Problem: low mobility in high-K/InGaAs structure

In high-K/InGaAs *surface-channel structure*:

- Low mobility (μ_e<2,000 cm^2/V.s vs. μ_e~10,000 cm^2/V.s in HEMT)
- $t_{ox} \downarrow \rightarrow \mu_e \downarrow$
- Mostly due to interface roughness scattering





Lin, IEDM 2008

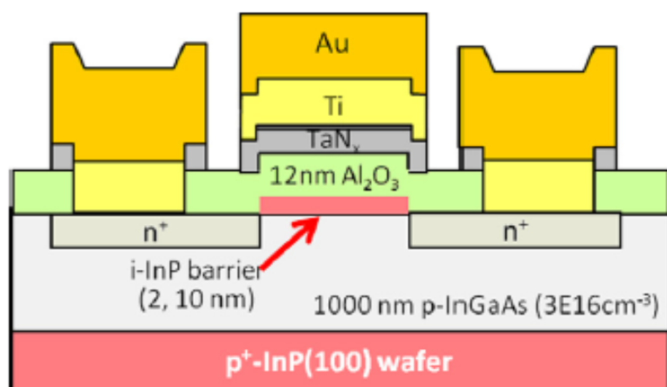
Solution: *buried-channel structure*

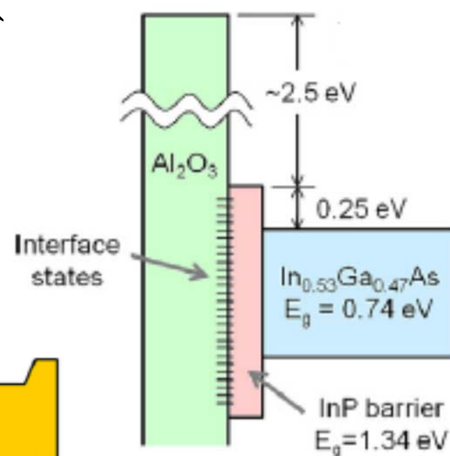
Introduce thin wide bandgap semiconductor between dielectric and channel:

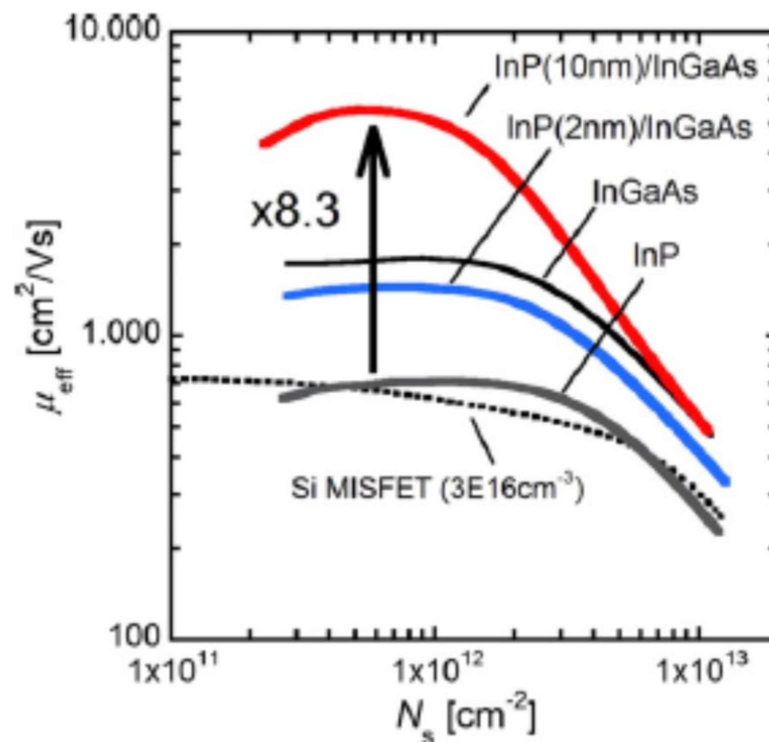
- For InGaAs, InP best choice (lattice matched, low D_{it} close to E_c)
- Key trade-off: scalability vs. transport:

$t_{barr} \downarrow \rightarrow \mu_e \downarrow$

$\rightarrow s \uparrow$

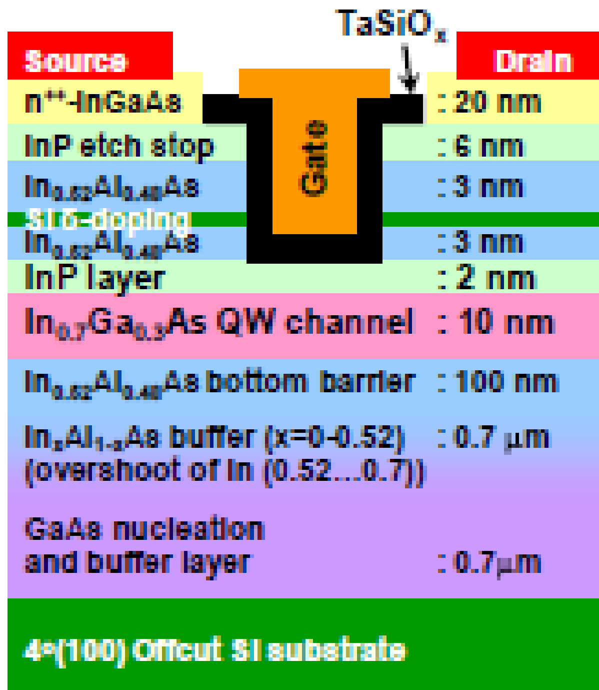




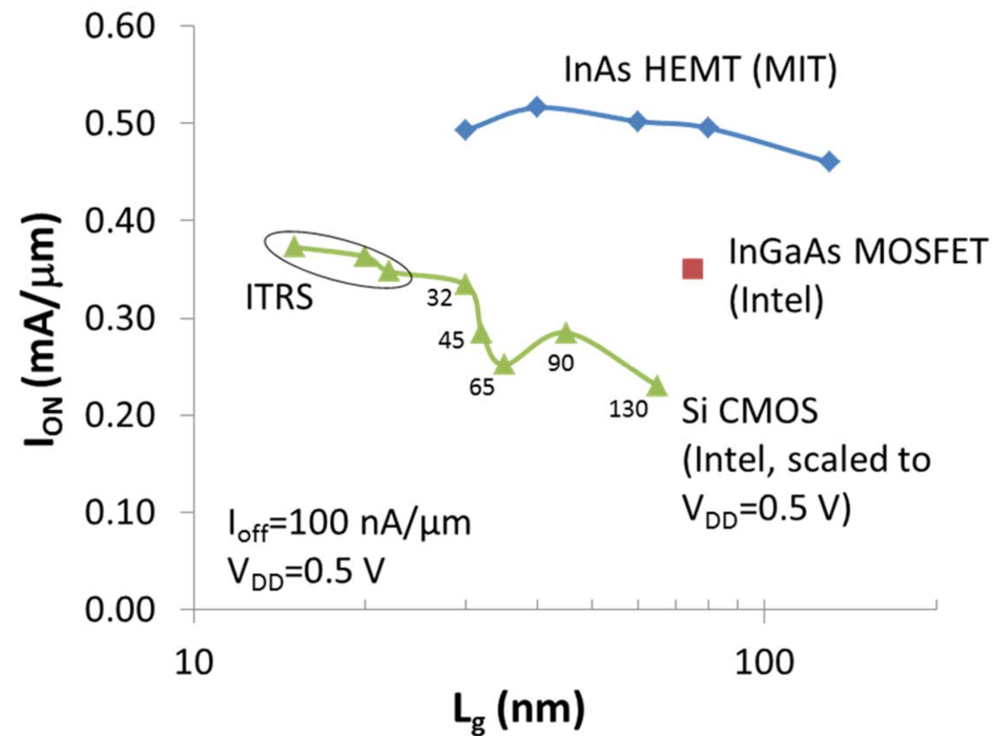


Urabe, ME 2011

The high-water mark: Intel's InGaAs Quantum-Well MOSFET



Radosavljevic, IEDM 2009

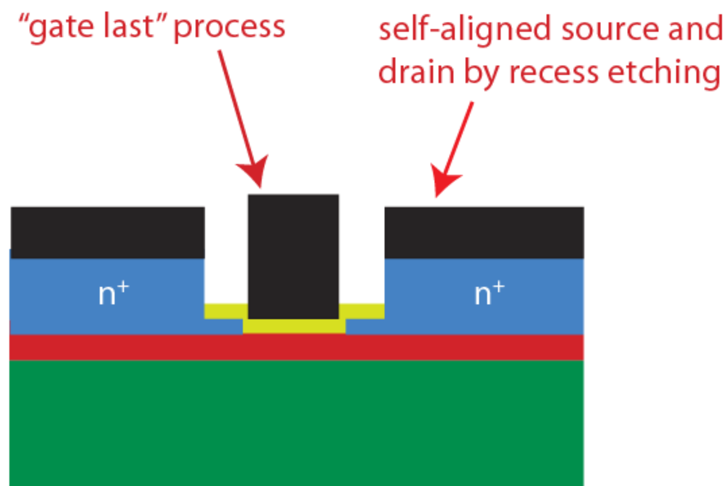


- Direct MBE on Si substrate (1.5 µm buffer thickness)
- InGaAs buried-channel MOSFET (under 2 nm InP barrier)
- 4 nm $TaSiO_x$ gate dielectric by ALD, L_g=75 nm
- First III-V QW-MOSFET with better performance than Si

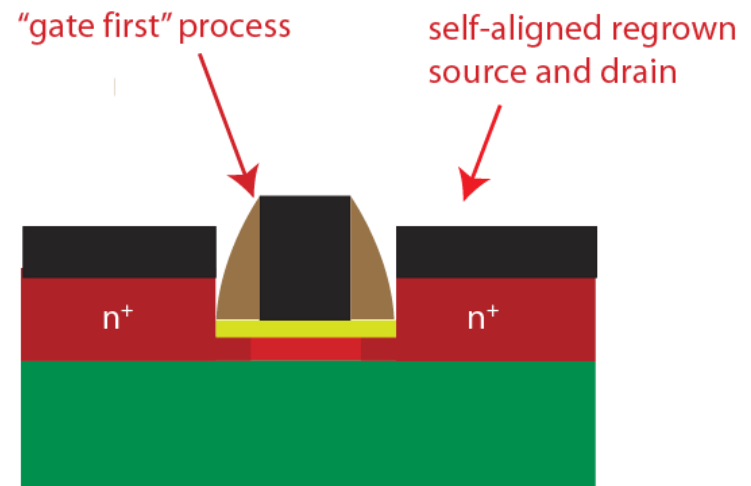
Critical issue #2: the ohmic contacts

Challenge: nanometer-scale ohmic contacts with low R_s

- Low contact resistance (R_s<100 Ω.μm)
- Raised above channel
- Self-aligned to gate (L_{side}<10 nm)

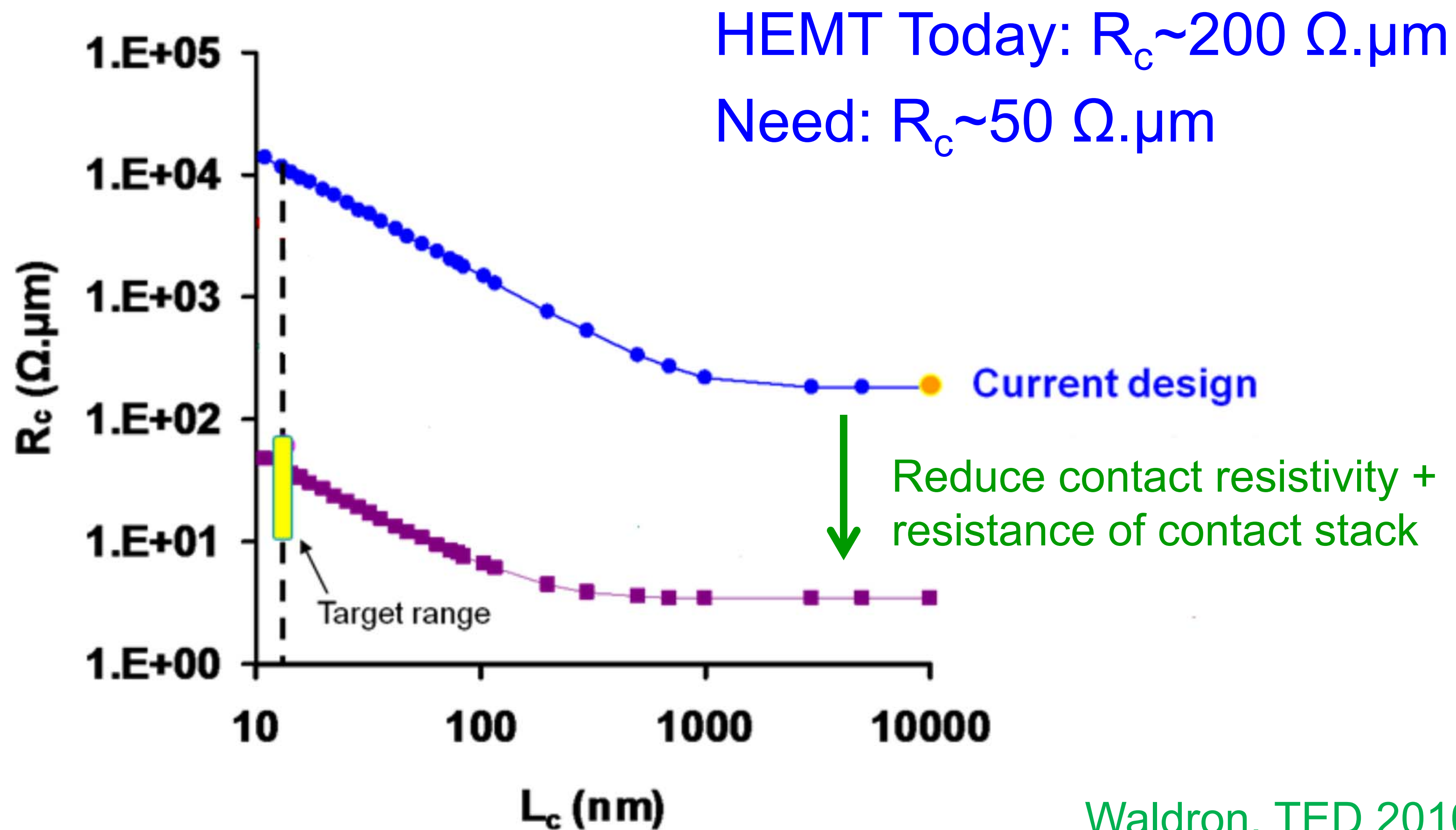


Recessed gate



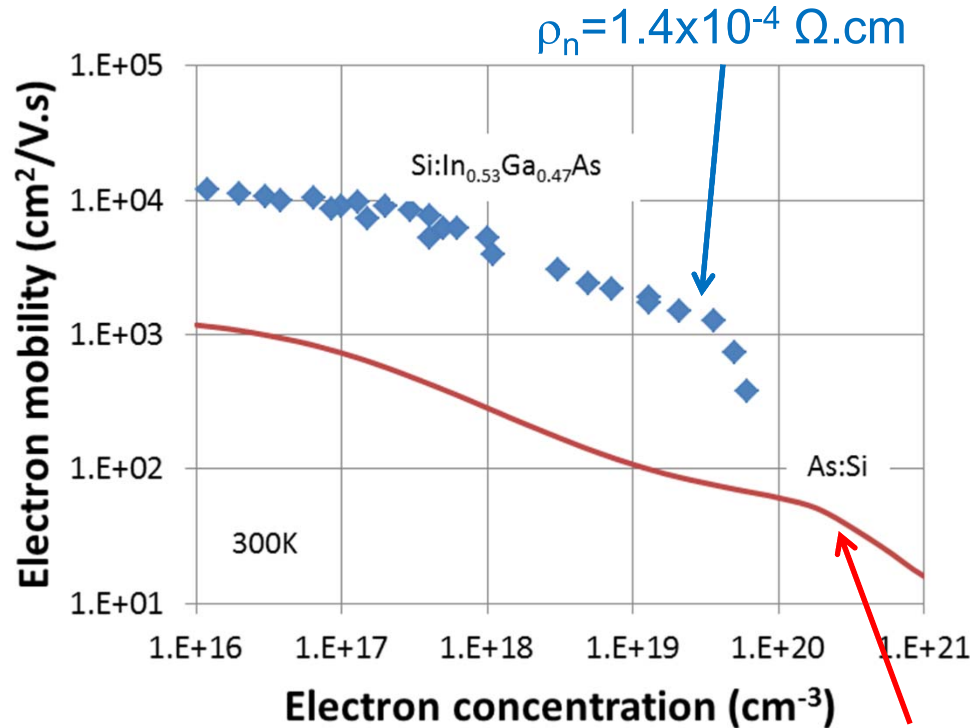
Regrown source and drain

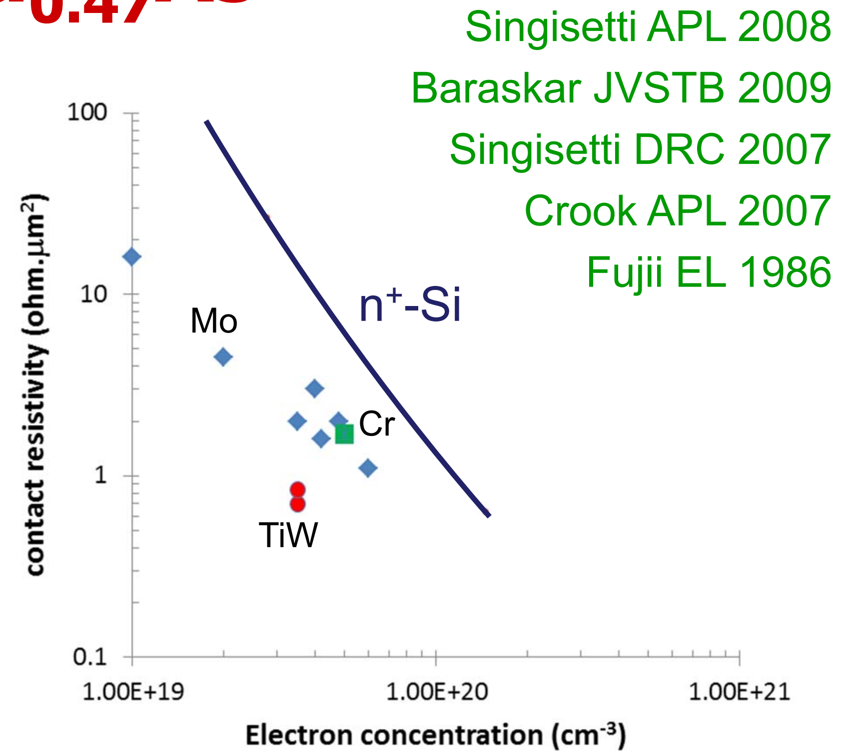
Key problem: ohmic contact scaling



Current contacts to III-V FETs are >100X off in required contact resistance

Resistivity and contact resistance of n^+-$In_{0.53}Ga_{0.47}As$





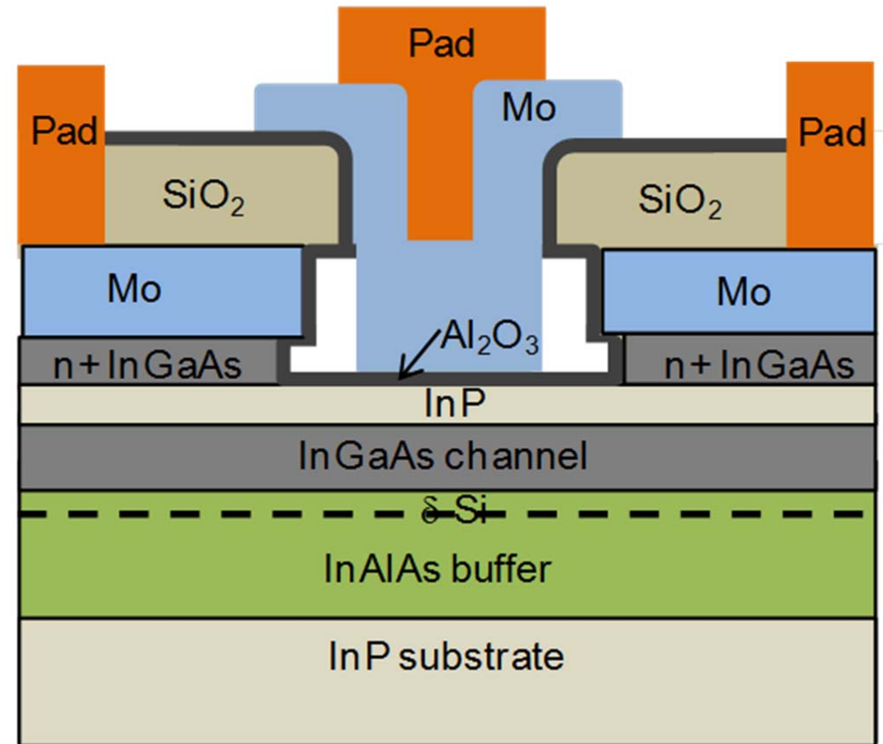
- n^+-$In_{0.53}Ga_{0.47}As$ *vs.* n^+-Si:
  - μ_e: ~10X across doping range → minimum ρ_n comparable
  - ρ_c comparable for various metals
- Fundamentally, contacts to InGaAs should be as good as to Si

Recessed-gate self-aligned InGaAs QW-MOSFET

Key features:

- Buried channel design
- Inverted-delta doping
- Refractory ohmic contacts
- Ohmic contacts self-aligned to gate
- Gate-last process
- Lift-off free front-end process
- Extensive RIE

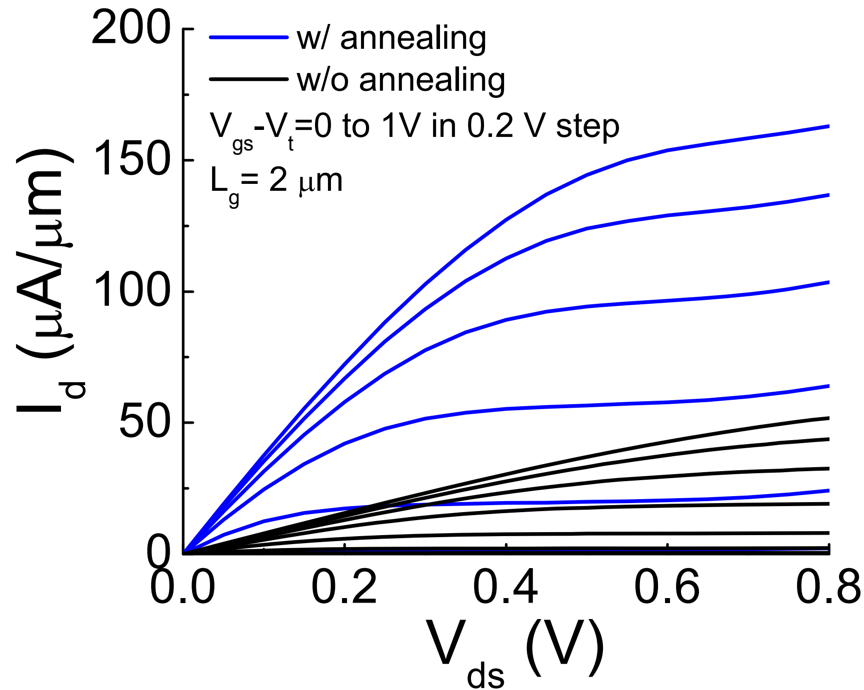
Lin, APEX 2012

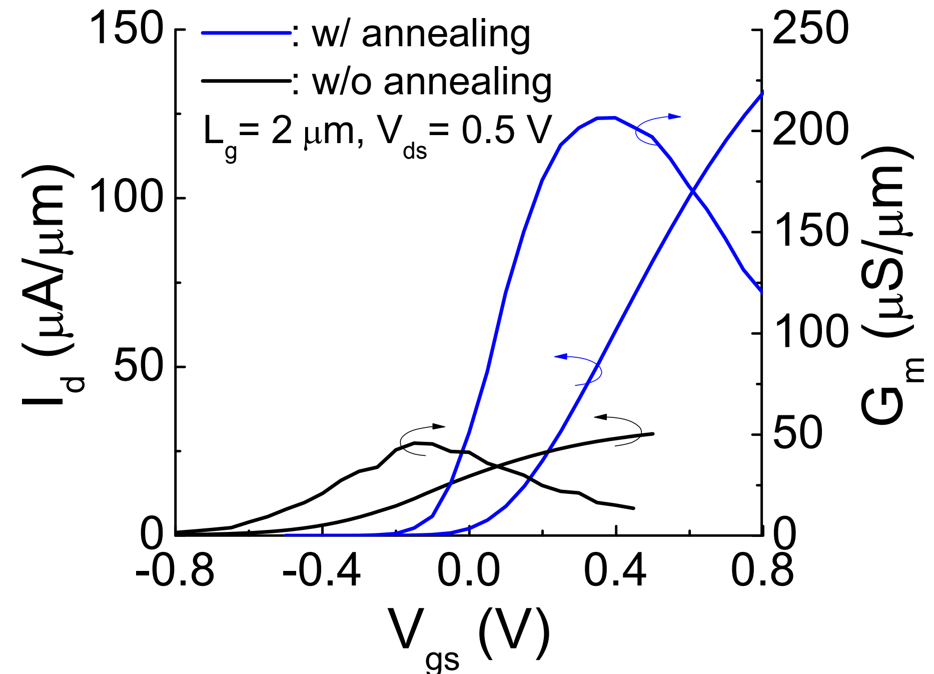


Process leverages self-aligned InGaAs HEMT for mmw applications

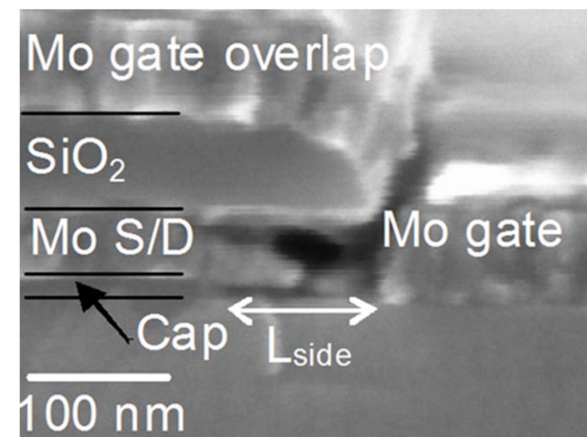
(Waldron, TED 2010; Kim, IEDM 2010)

Output and transfer characteristics: evidence of RIE damage and solution

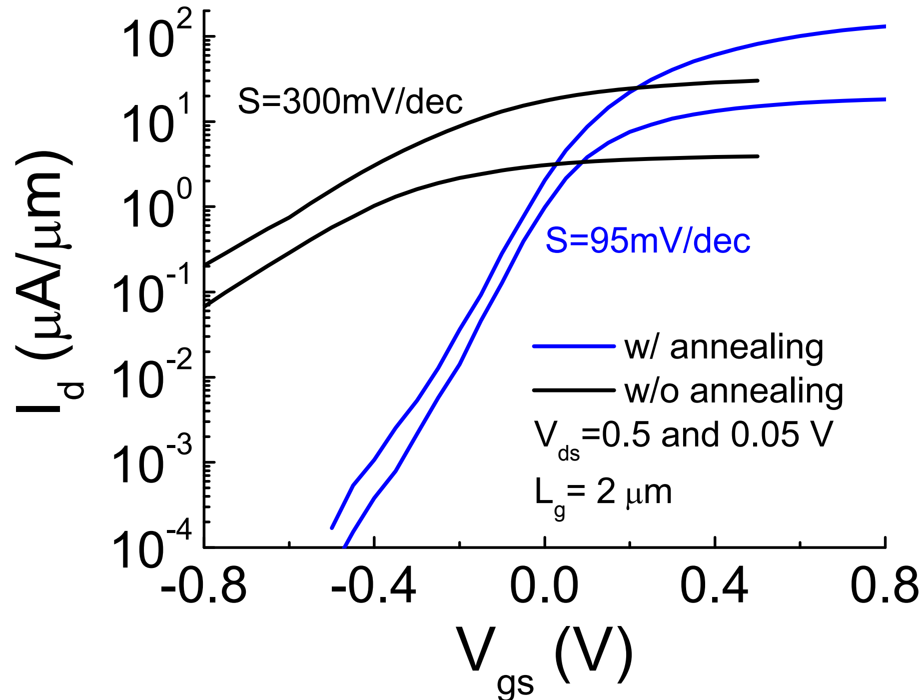


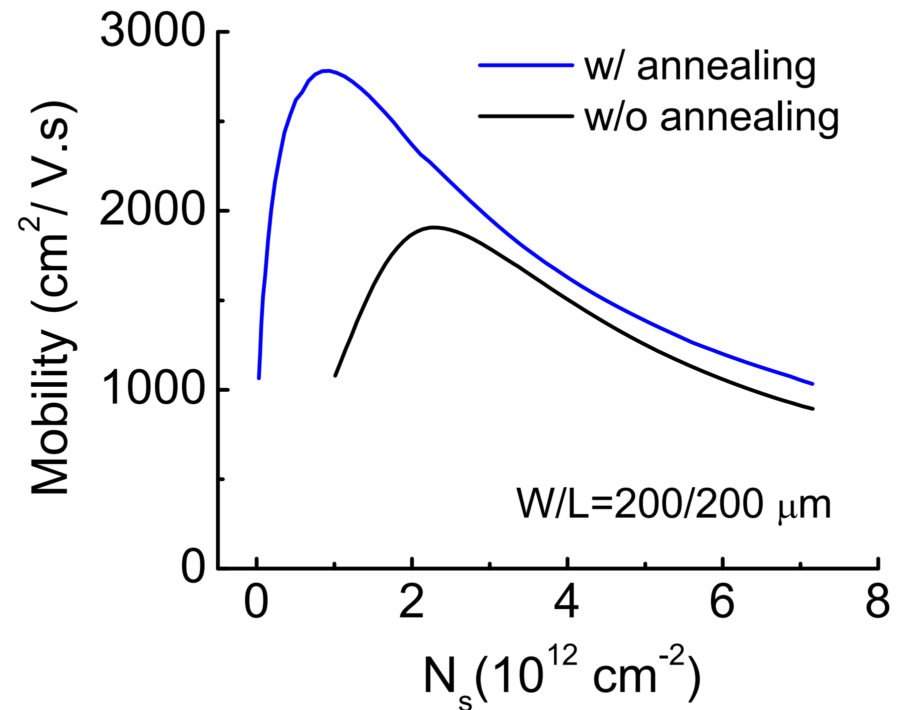


- L_g=2 μm, L_{side}= 100 nm
- RIE leads to extensive device damage
- Damage annealed at 340°C for 15 min
- g_m=205 μS/μm at V_{DS}=0.5 V for L_g=2 μm
- V_T=0.05 V



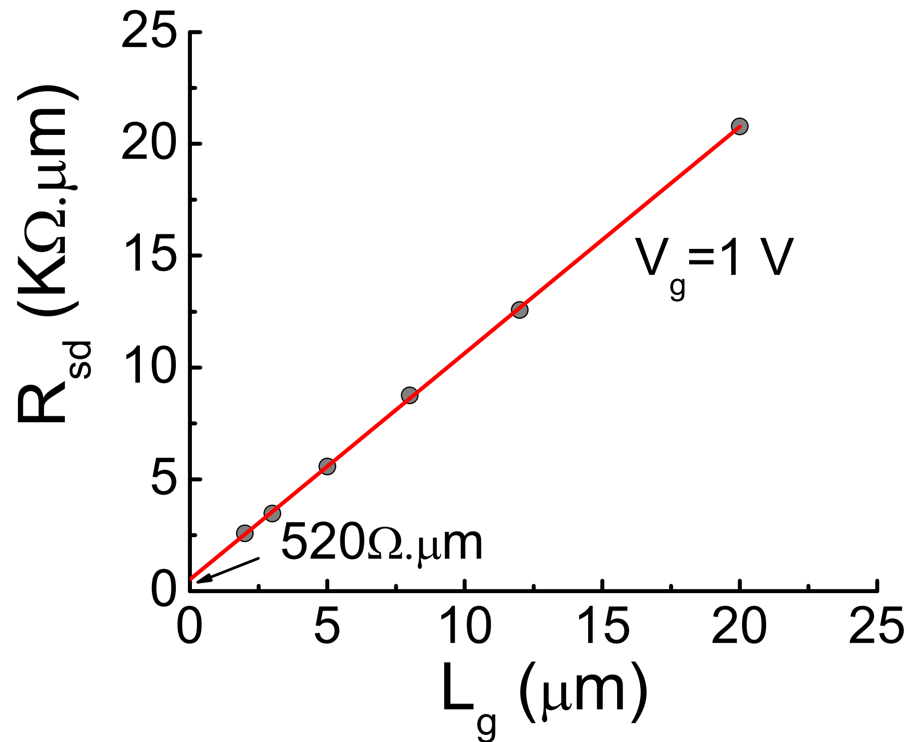
Subthreshold and mobility characteristics

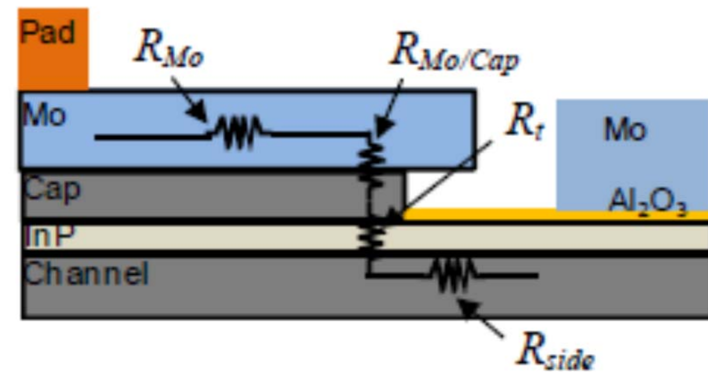




- S=95 mV/dec
- $I_{on}/I_{off}=10^6$
- μ_{peak}=2800 cm^2/V.s

Source and drain resistance





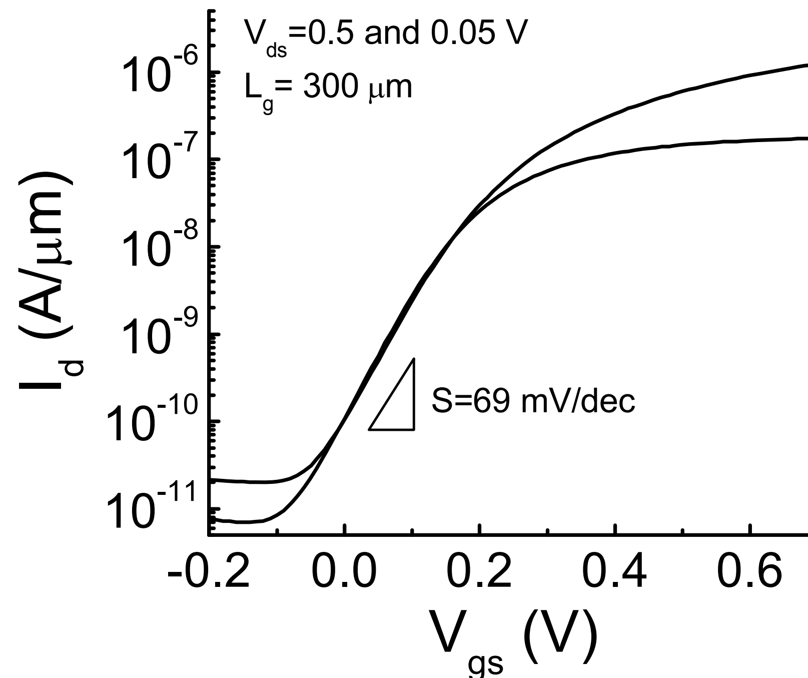
R_{Mo}= 120 Ω.µm, $R_{Mo/Cap}$+R_t = 50 Ω.µm

R_{side}= 100 Ω.µm

- R_s=260 Ω.µm (our best result in HEMT ~140 Ω.µm)
- Major component is lateral Mo resistance (R_{sh}=25 Ω/□)
- Vertical tunneling resistance greatly reduced wrt HEMT (50 Ω.µm vs. >100 Ω.µm)

Latest results: Dielectric scaling to EOT<1 nm

InP (1 nm) + Al_2O_3 (0.4 nm) + HfO_2 (2 nm) → EOT~0.9 nm



Lin, IEDM 2012

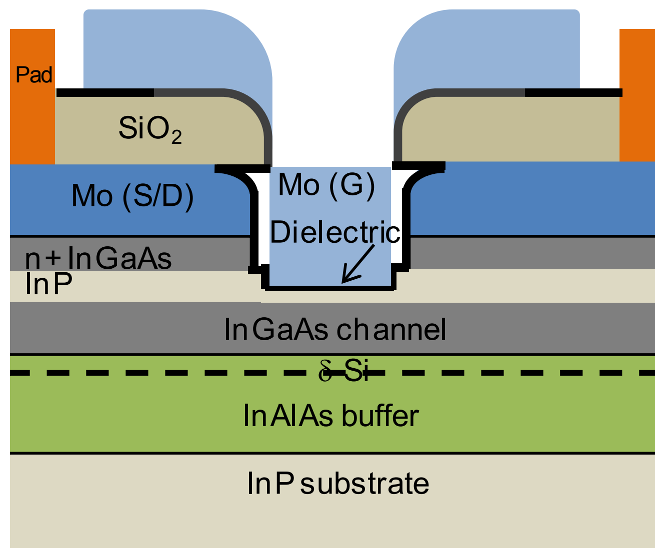
- Long-channel $In_{0.53}Ga_{0.47}As$ FET
- InP scaled to 1 nm by Ar-based dry etching
- S=69 mV/dec
- Close to lowest S reported in any III-V MOSFET: 66 mV/dec (EOT=1.2 nm) [Radosavljevic, IEDM 2011]

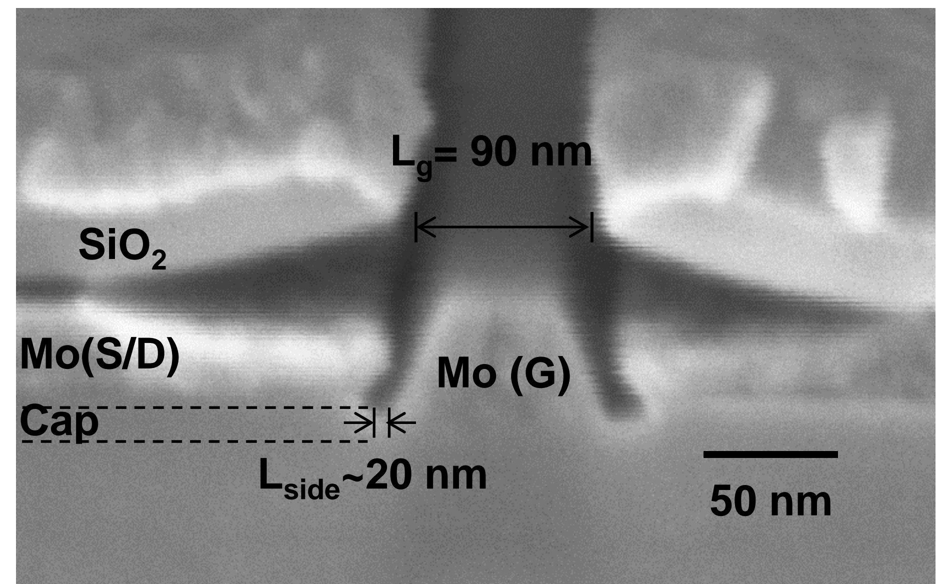
Latest results: L_g=60 nm QW-MOSFET

Many improvements:

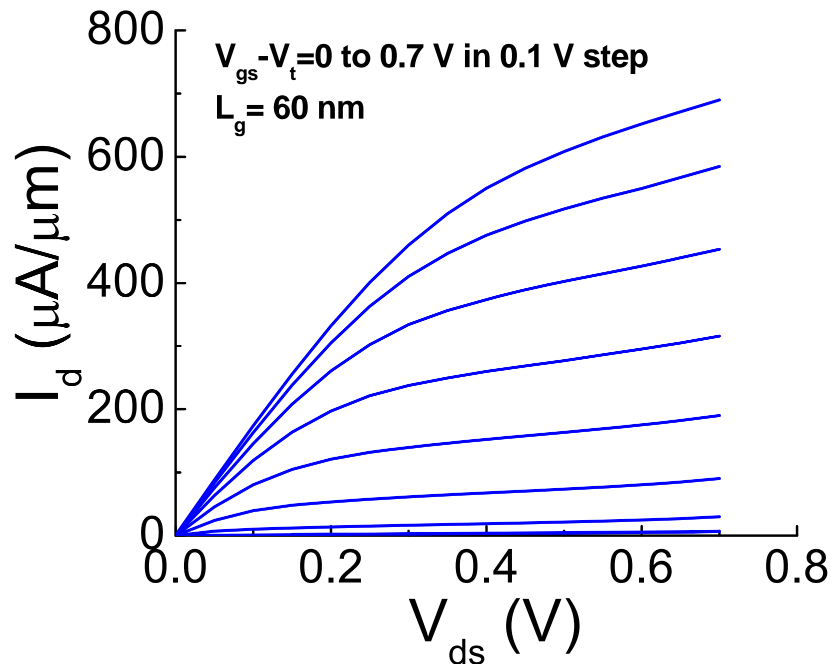
Lin, IEDM 2012

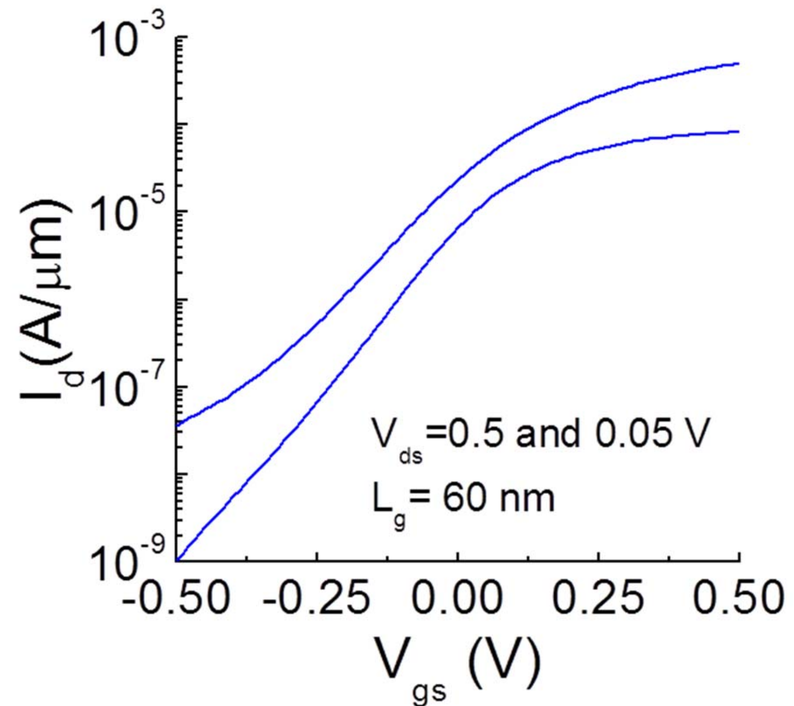
- L_g=60 nm
- Improved gate recess process
- Tight S/D spacing (L_{side} < 20 nm)
- Scaled barrier (InP) and dielectric (high-K) thickness





Transfer and output characteristics

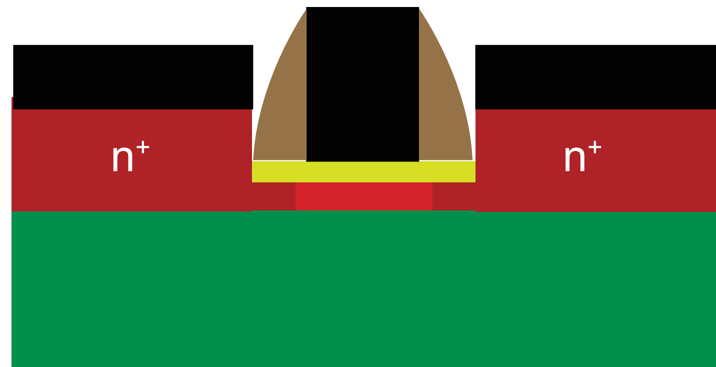




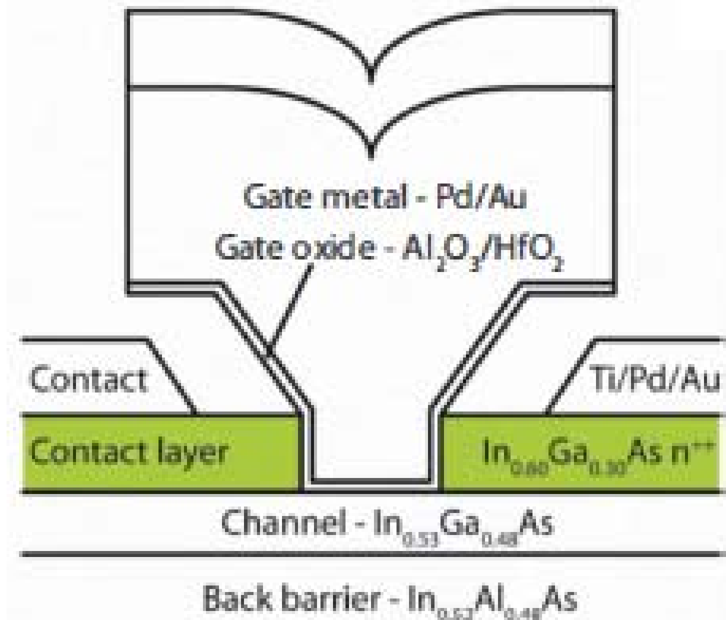
- S=145 mV/dec at 0.5 V
- I_{on} = 120 mA/μm measured at V_{dd}= 0.5 V and I_{off}= 100 nA/μm
- Peak g_m = 1250 μS/μm
- I_g < $5x10^{-10}$ A/μm at maximum gate overdrive
- R_{on} = 570 Ω.μm (at V_{gs}-V_t=0.7 V)

Lin, IEDM 2012

Regrown source and drain self-aligned InGaAs QW-MOSFET



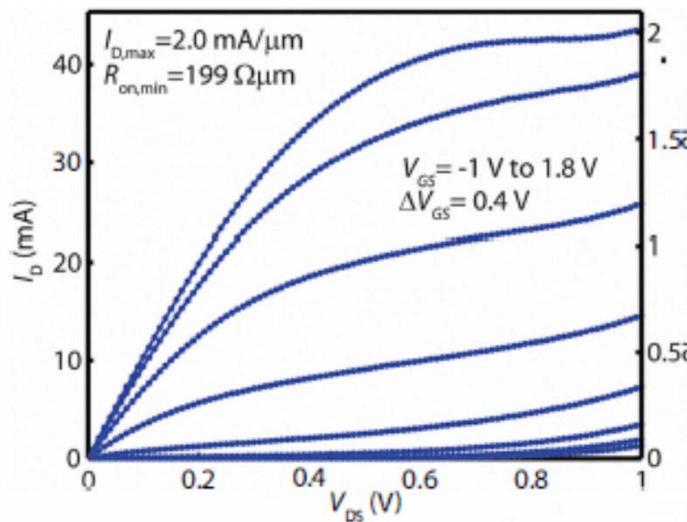
Egard, IEDM 2011

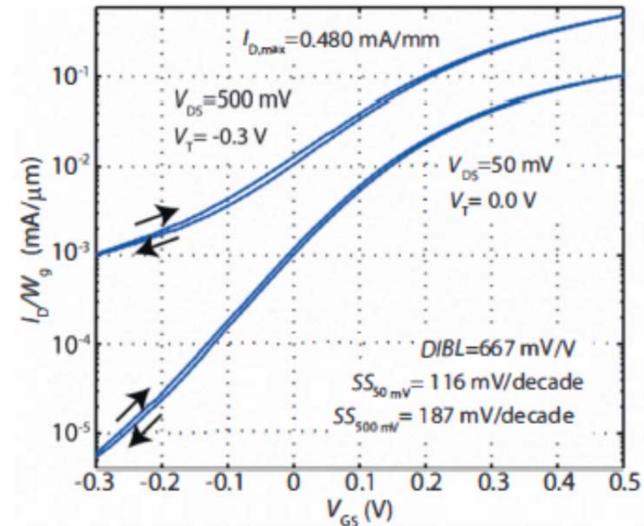


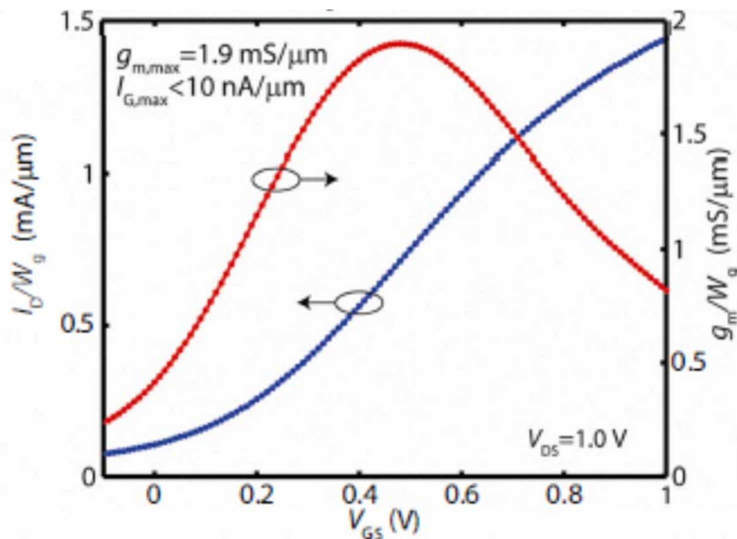
Key features:

- n^+-InGaAs raised source and drain regions grown by MOCVD
- Self-aligned to gate
- Surface quantum-well channel
- Gate oxide: Al_2O_3 (0.5 nm) + HfO_2 (6.5 nm); EOT=1.3 nm

Characteristics of L_g=55 nm MOSFET







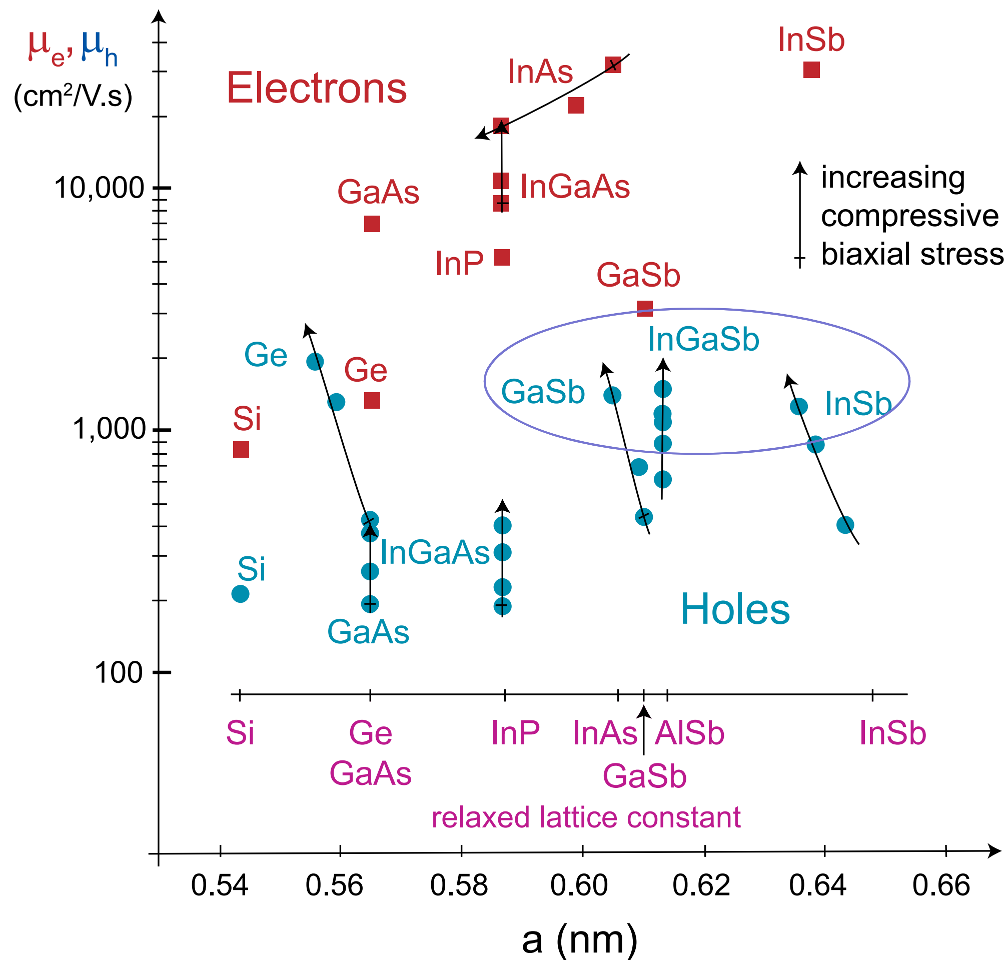
- g_m=1900 µS/µm
- S=187 mV/dec
- R_S=88 Ω.µm

Egard, IEDM 2011

Critical issue #3: the p-channel device

Challenge: high-performance p-type III-V MOSFETs

- Antimonide channel
- Incorporating strong compressive strain



del Alamo, Nature 2011

III-V pFETs: the benefits of strain

Uniaxial-strain piezoresistance coefficients in p-type Quantum Wells

Thompson, IEDM 2006

Weber, IEDM 2007

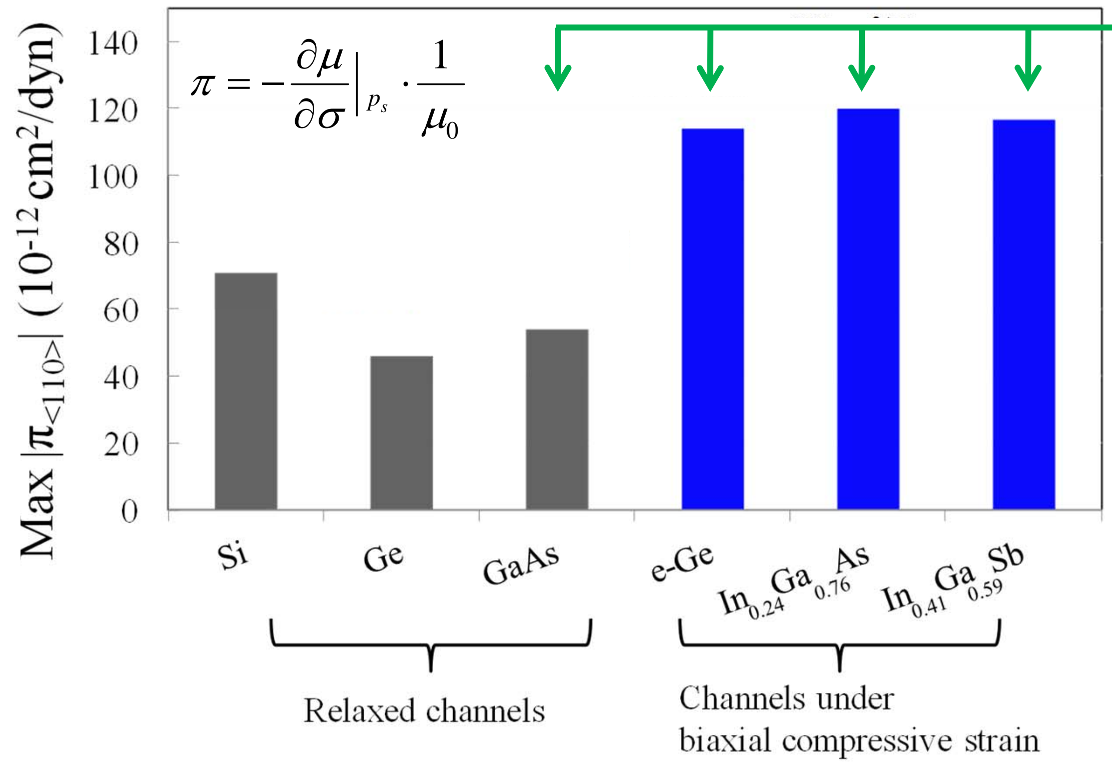
MIT work

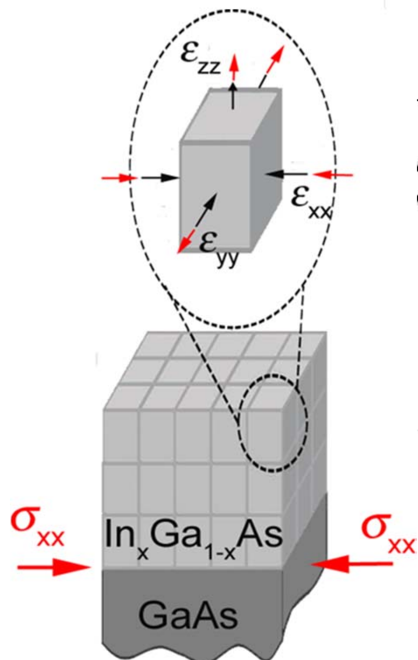
Xia, APL 2011

Xia, TED 2011

Xia, ISCS 2011

Gomez, EDL 2010

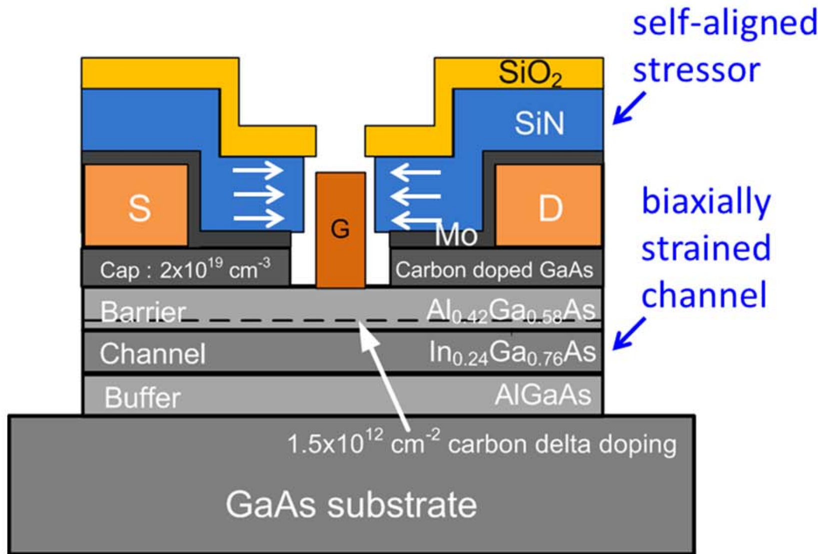


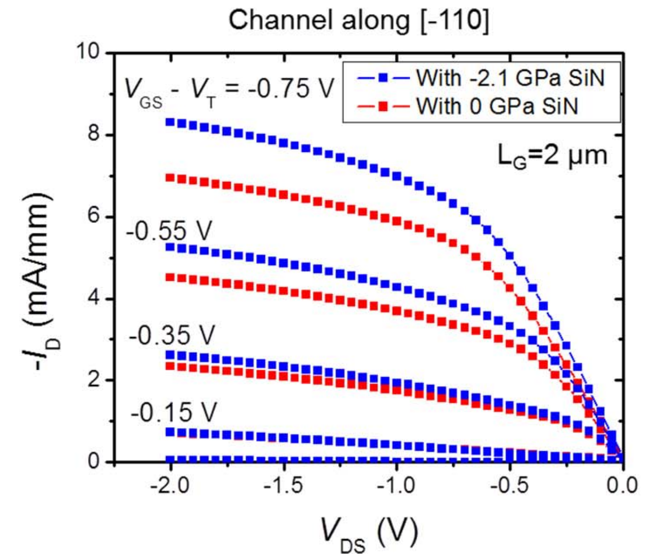


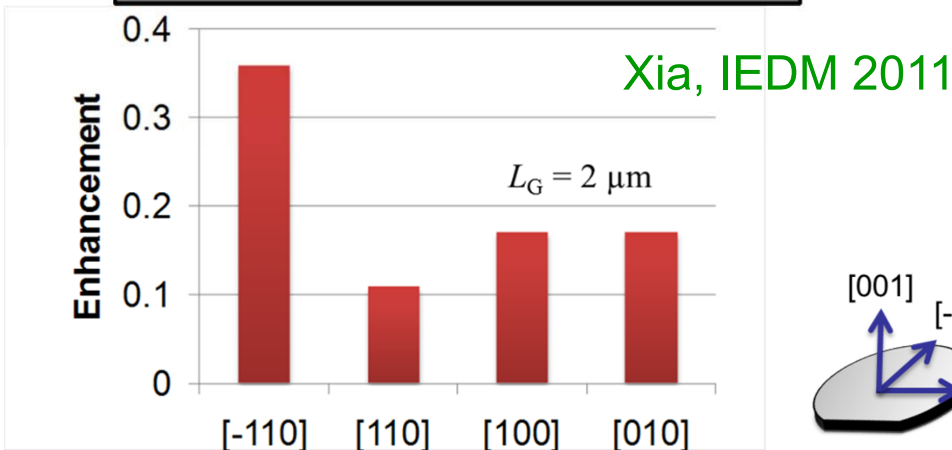
Compressive *biaxial* strain + *uniaxial* strain

→ μ↑↑

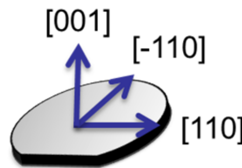
P-type InGaAs QW-FET with process-induced uniaxial strain + epitaxially-grown biaxial strain

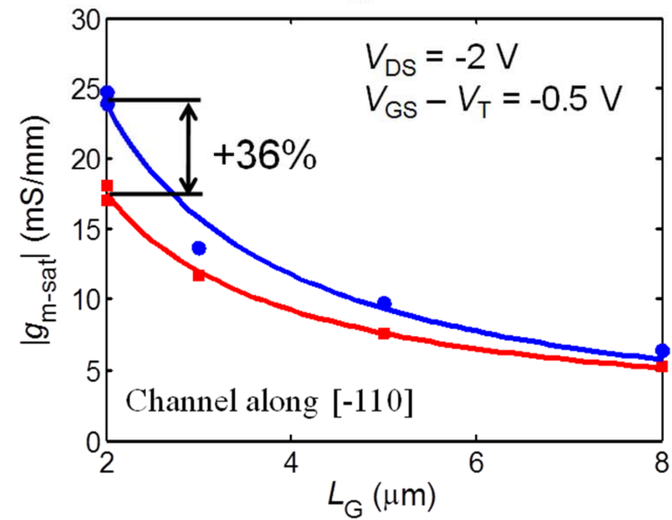






Xia, IEDM 2011



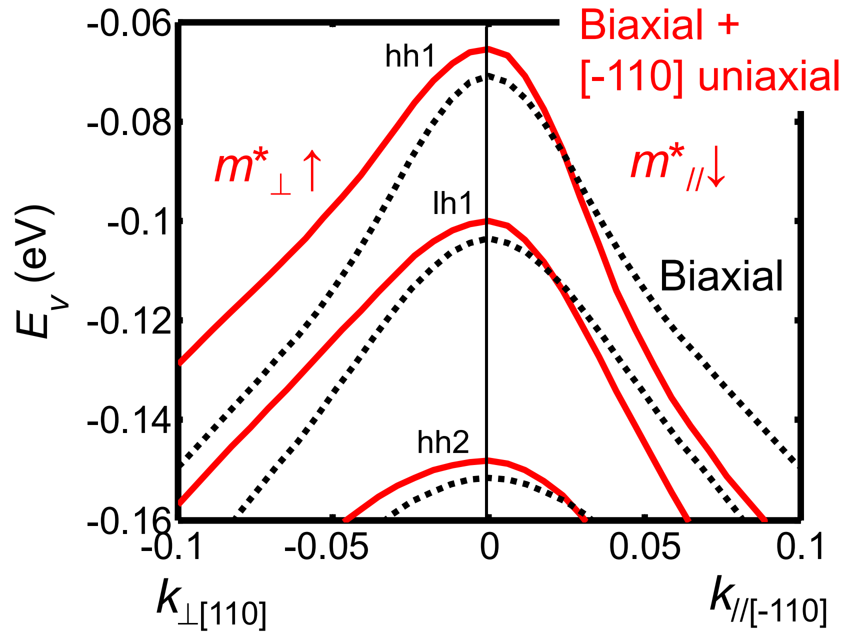


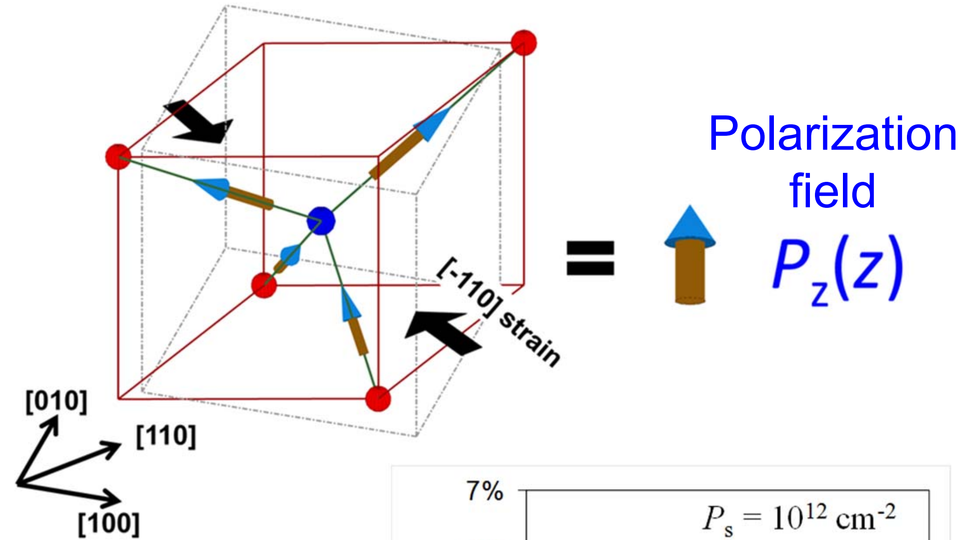
Anisotropic g_m enhancement

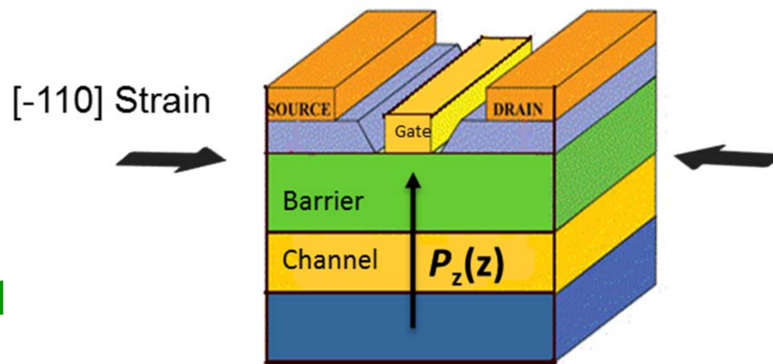
g_m enhancement scales correctly

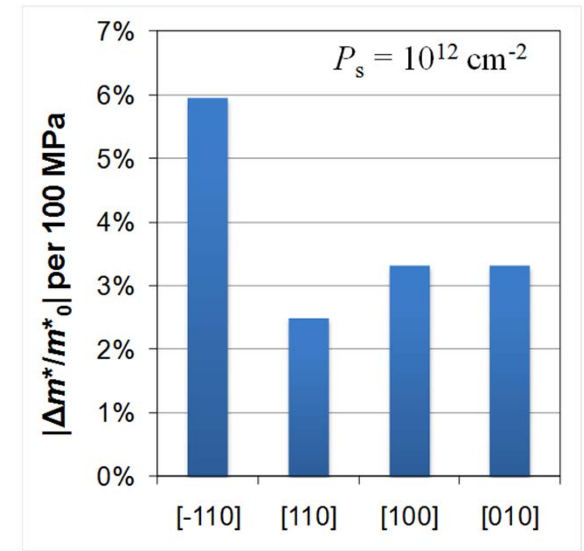
Strain-induced Δg_m anisotropy

Result of band deformation + piezoelectric effect









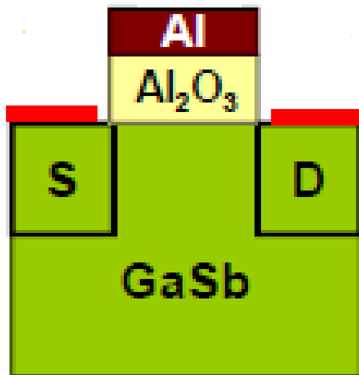
Xia, IEDM 2011

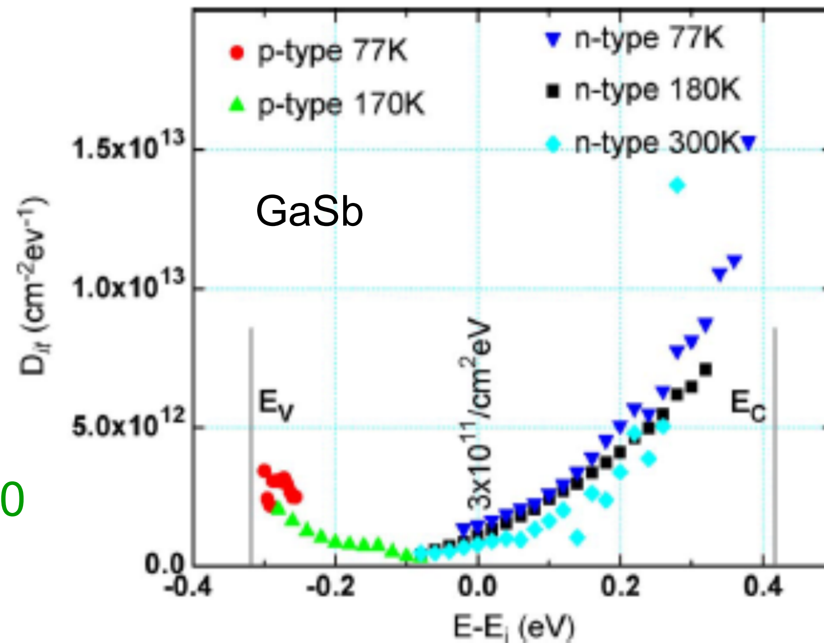
P_z affects quantization in valence band → m* anisotropy

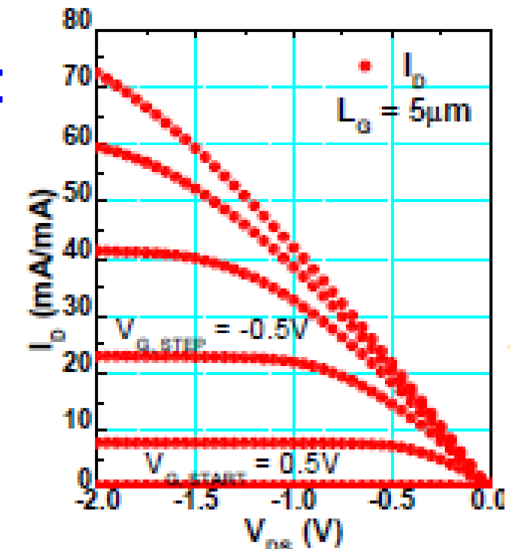
InGaSb surface-channel MOSFET

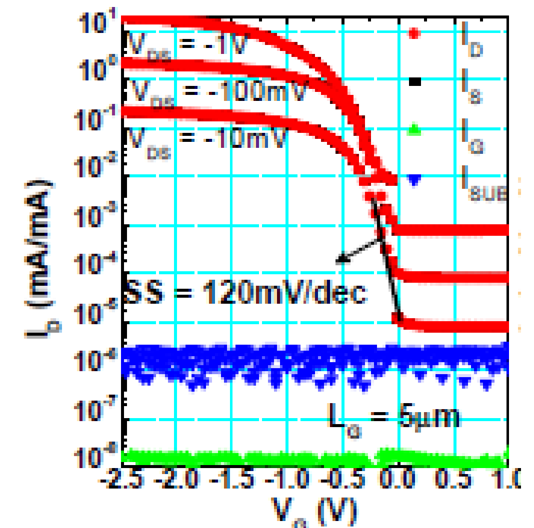
InGaSb surface channel device problematic:

high D_{it} close to valence band edge









Nainani, IEDM 2010

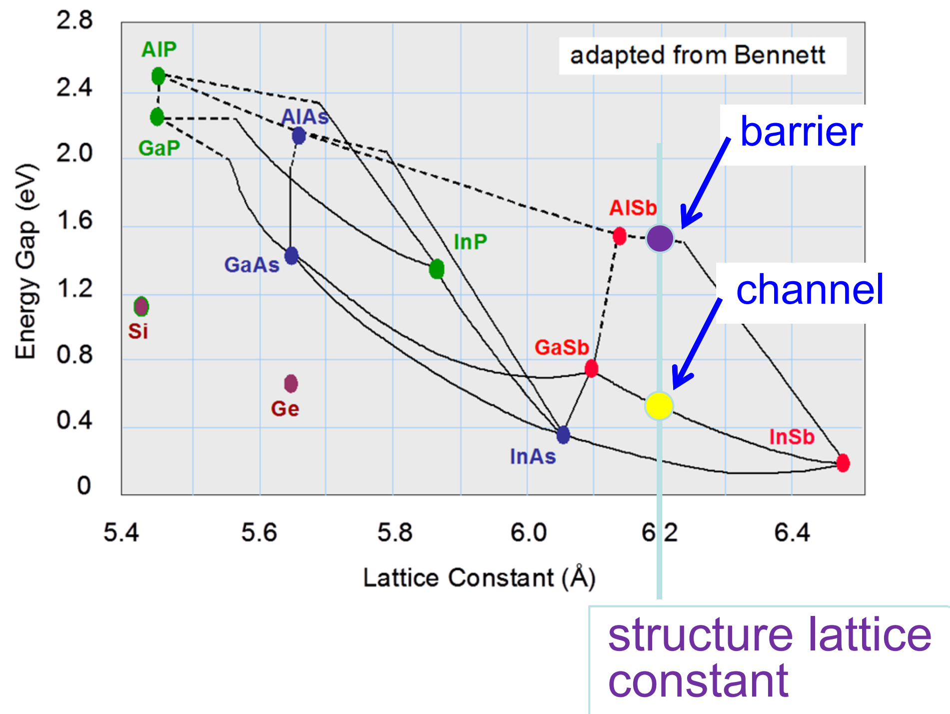
Nainani, TED 2011

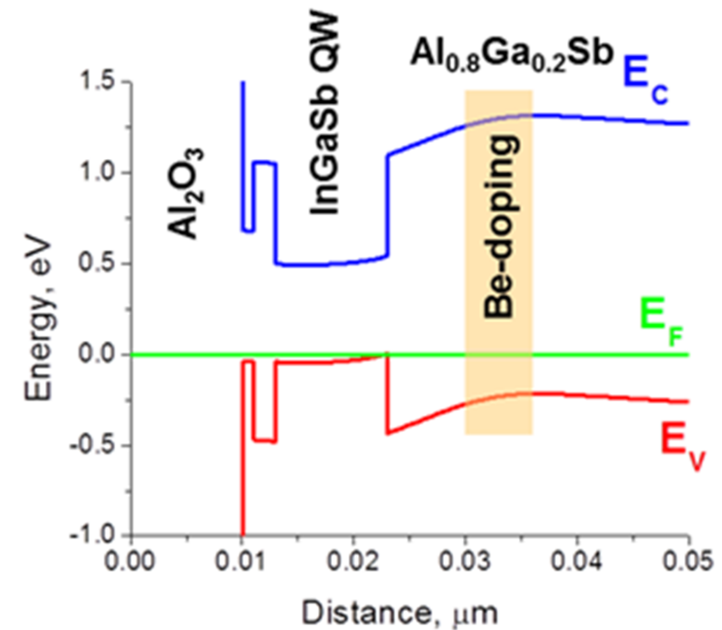
- Al_2O_3 (10 nm) / $In_{0.35}Ga_{0.65}Sb$ (7 nm) MOSFET
- S=120 mV/dec in L_g=5 µm device

InGaSb buried-channel MOSFET

Need Al containing barrier (*i.e.* AlInSb)

→ Also need cap: GaSb or InAs



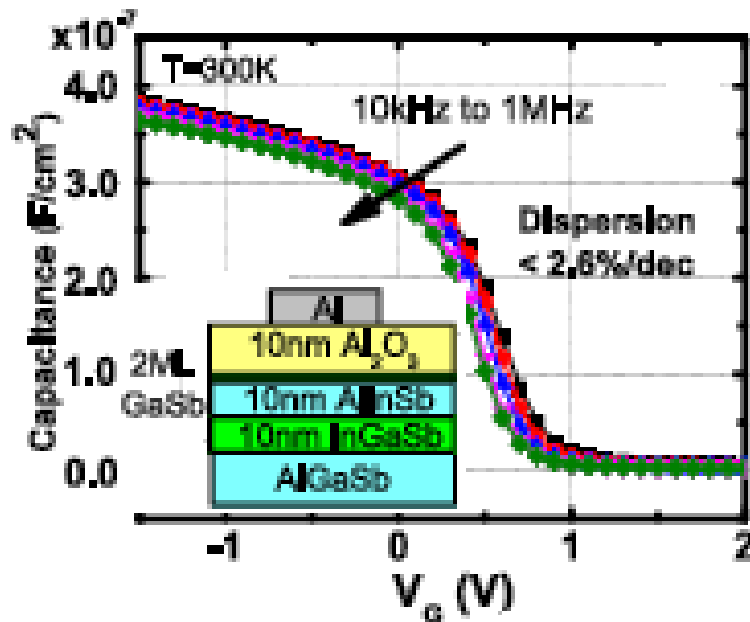


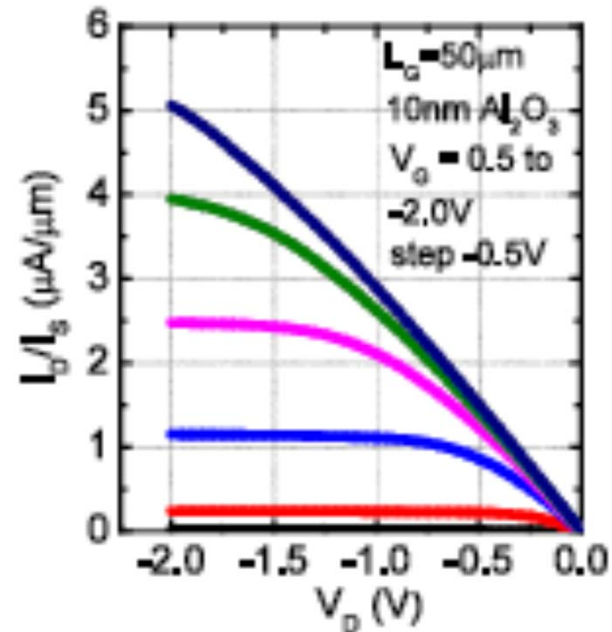
Madisetti, DRC 2012

Scalibility problems for buried-channel InGaSb MOSFETs

InGaSb buried-channel MOSFET

Al_2O_3/GaSb/AlInSb/InGaSb buried-channel MOSFET:





No subthreshold swing data given

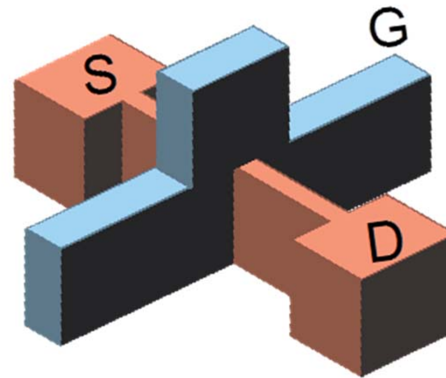
Yuan, VLSI Tech 2012

Critical issue #4: non-planar MOSFET designs

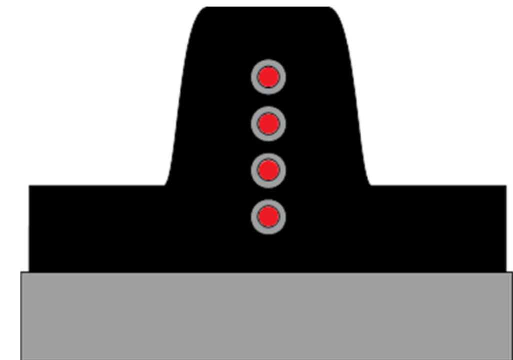
Challenge: small subthreshold swing on a small-footprint

- Planar designs might not provide enough "electrostatic integrity"
- Need higher carrier confinement through restricted dimensionality designs

QW-MOSFET



FinFET

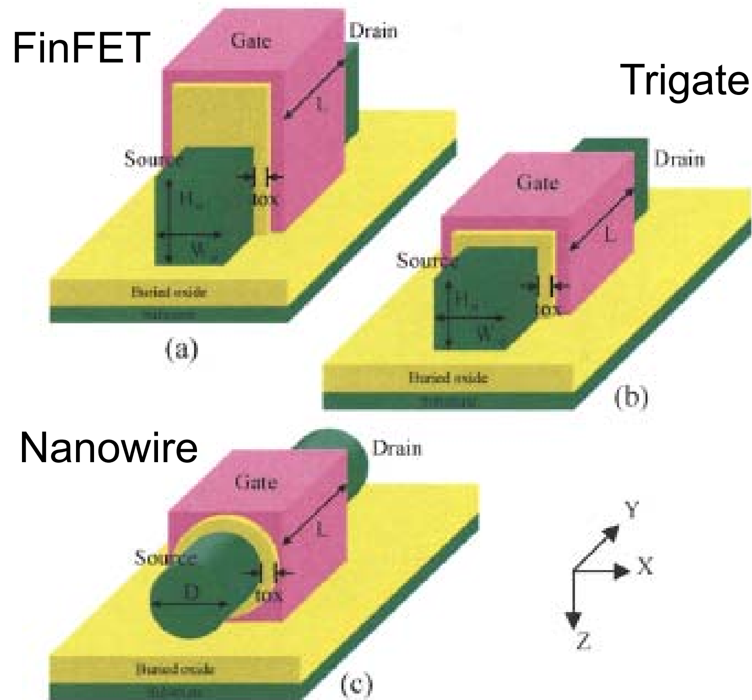


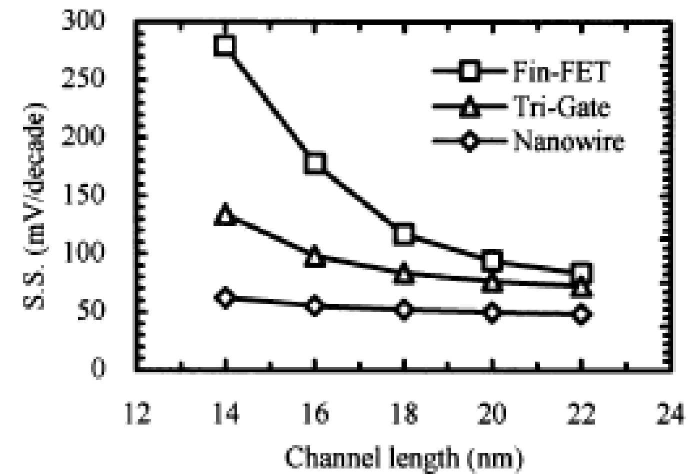
Gate-all-around nanowire FET

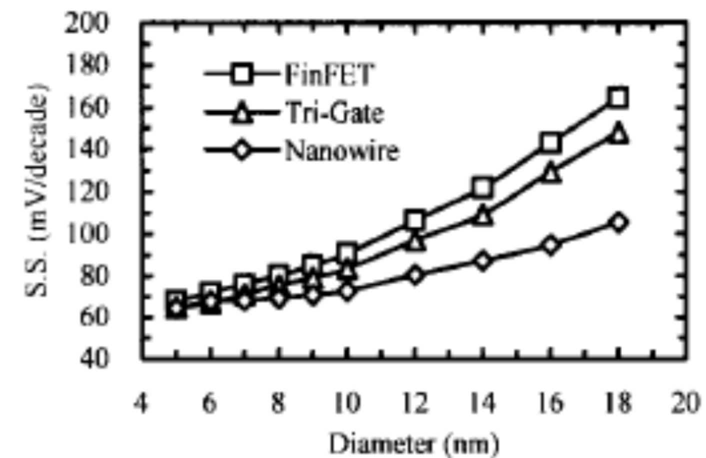
Increased electrostatic control through multiple gates

As number of gates increases, electrostatic control of gate over channel improves → S ↓

- Improved L_g scaling
- Cross section ↓ → S ↓

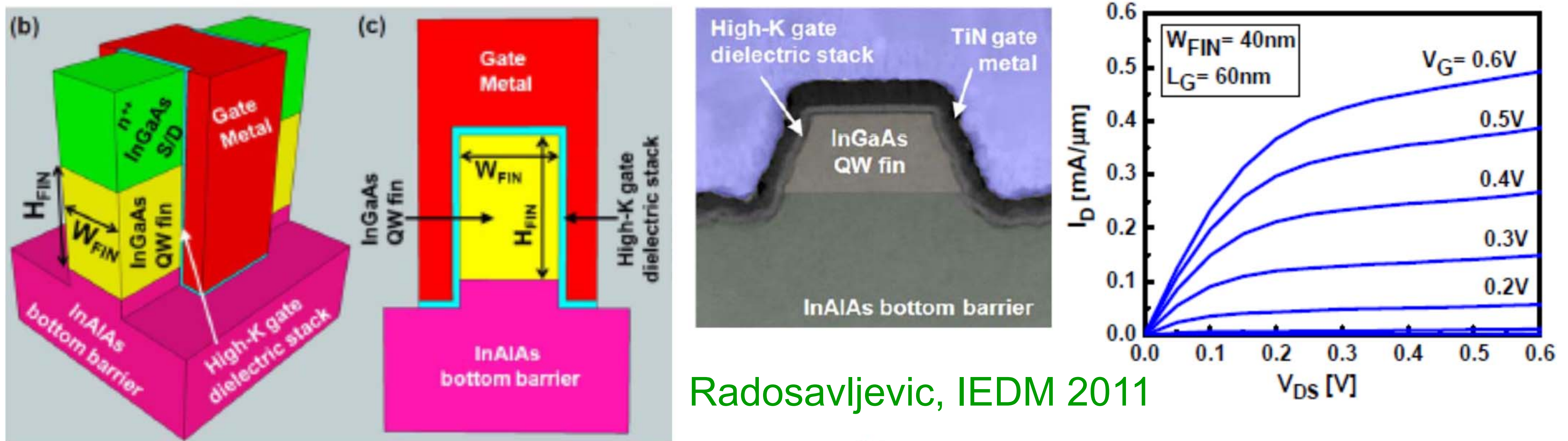




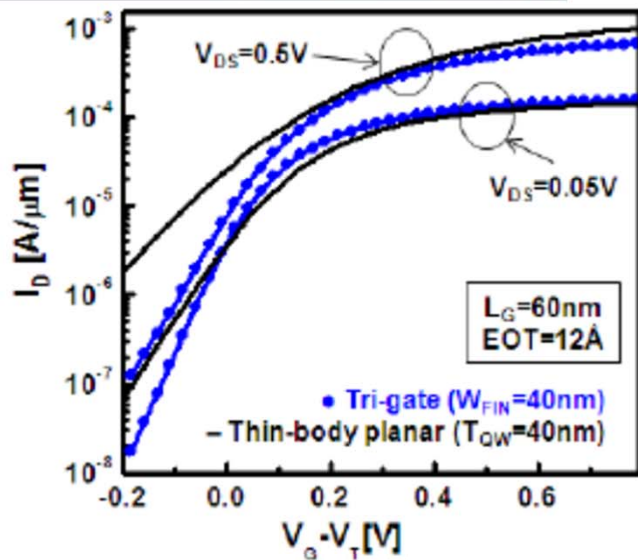


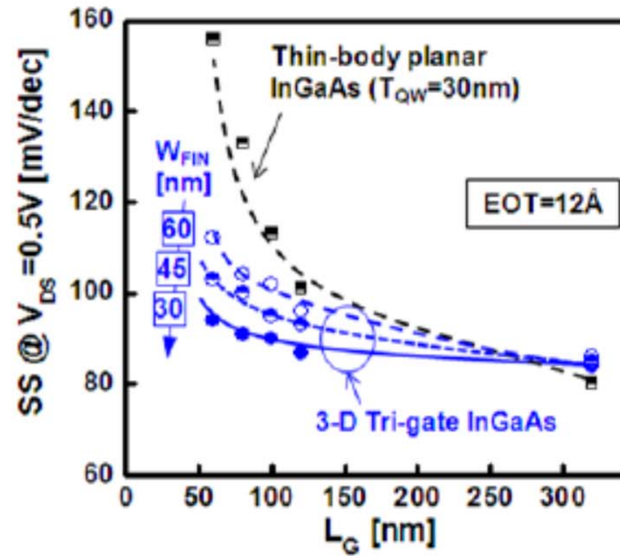
Chen, ICSICT 2008

InGaAs Trigate MOSFET



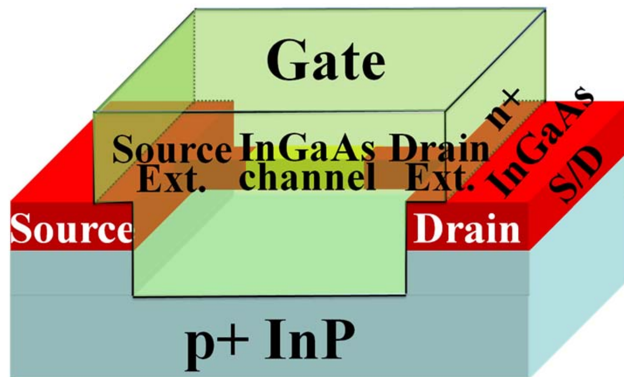
Radosavljevic, IEDM 2011

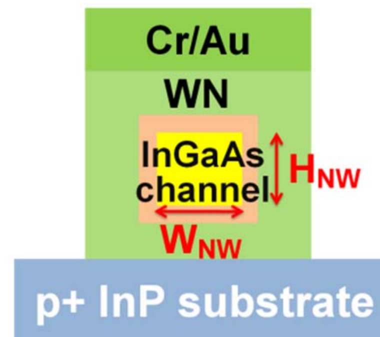


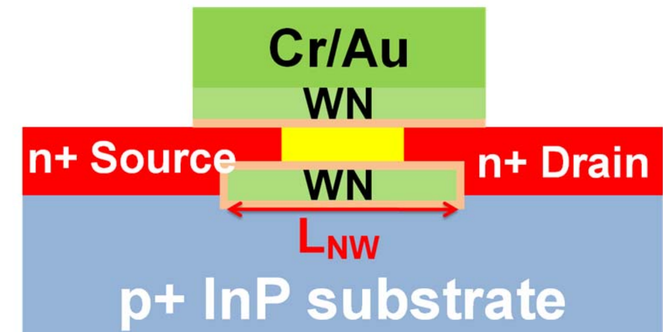


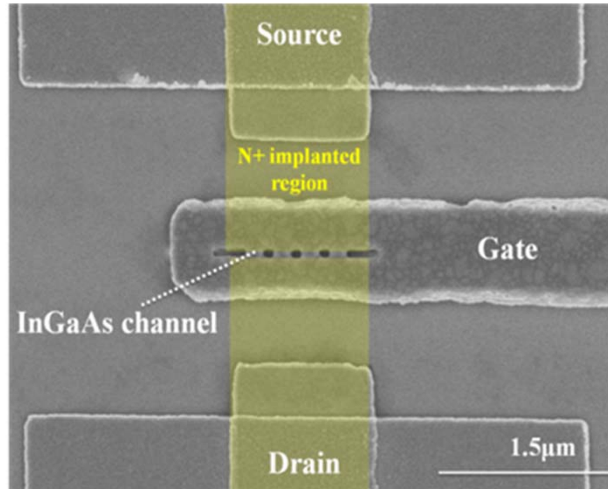
Far improved S vs. planar quantum-well MOSFET

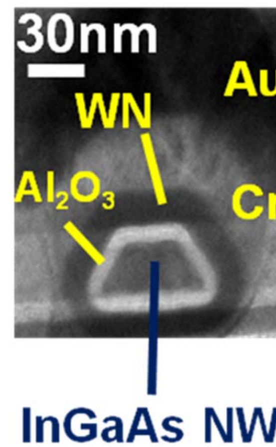
InGaAs Gate-All-Around Nanowire MOSFET









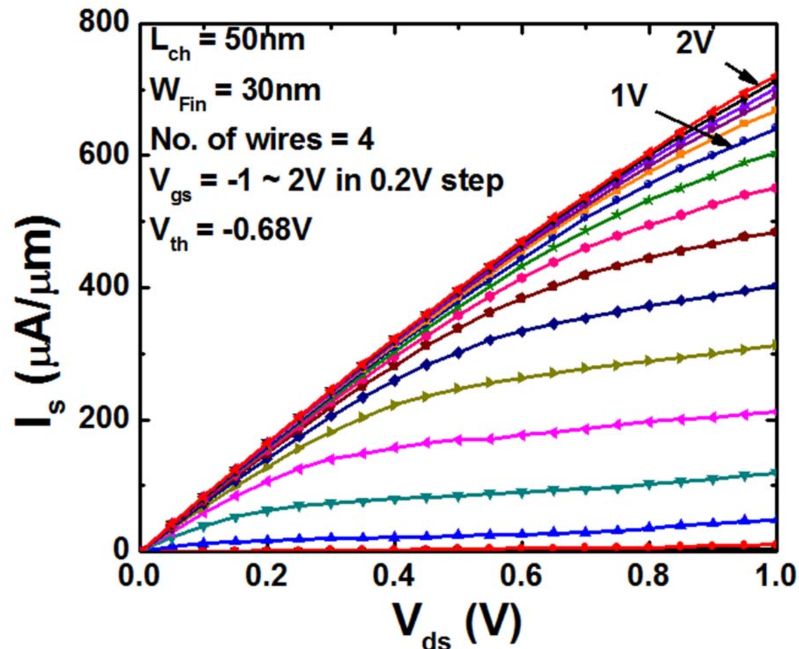


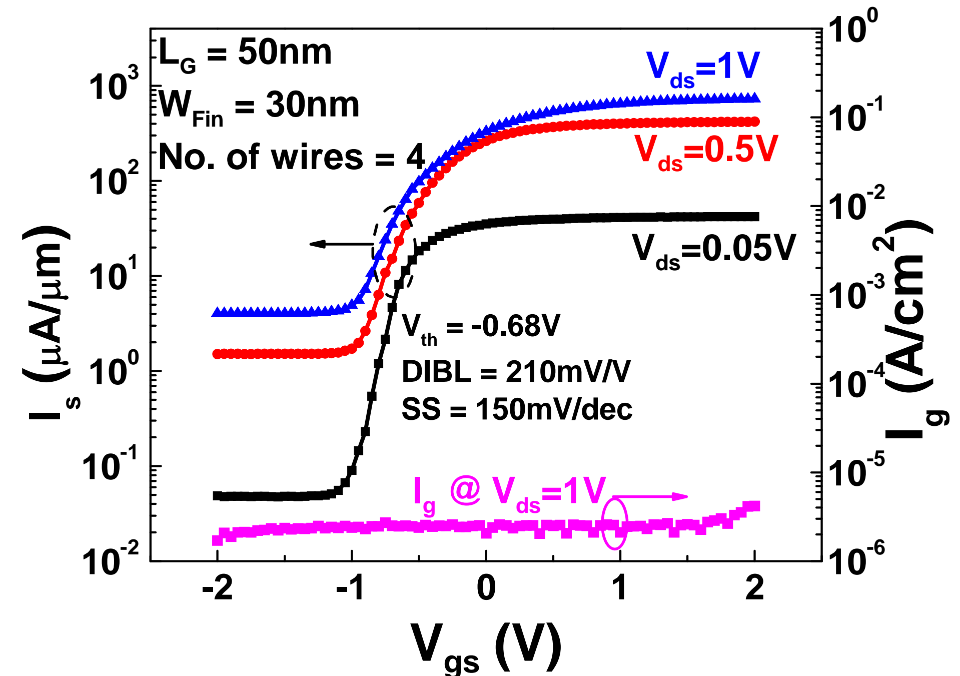
- L_{ch}= 50-120 nm
- W_{Fin}=30, 50 nm
- H_{Fin} = 30 nm
- L_{NW} = 150-200 nm
- t_{ox} = 10 nm Al_2O_3
- # wires = 1, 4, 9, 19

Gu, IEDM 2011
Gu, APL 2011

Surface-channel design

InGaAs Gate-All-Around Nanowire MOSFET





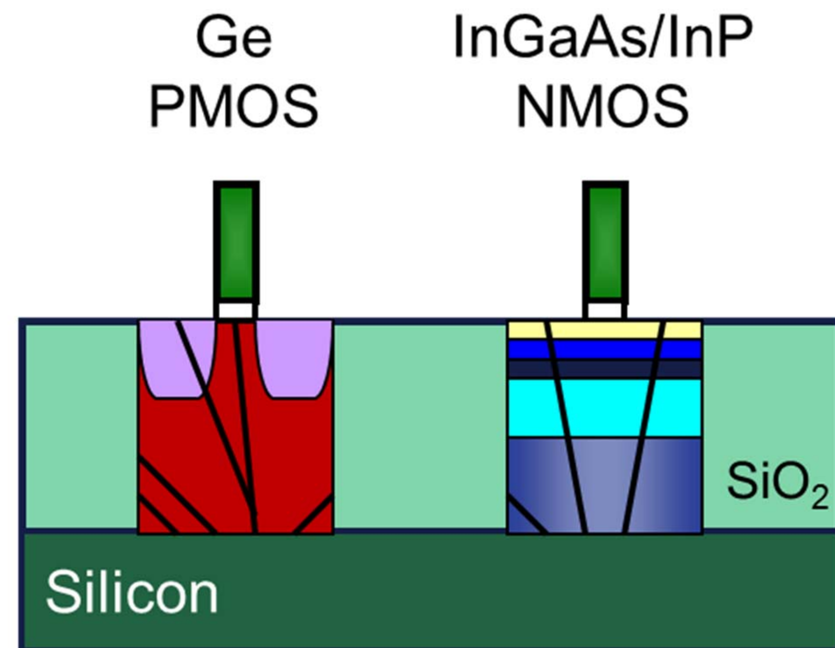
- I_{on} =720 μA/μm (86 μA/wire)
- g_m =510 μS/μm (61 μS/wire) at V_{GS}-V_T=2 V
- S=150 mV/dec (EOT≈4.5 nm), I_g <10^{-7} A/cm^2
- Low field μ~900 cm^2/V.s (200 cm^2/V.s in Si GAA NW from Samsung)

Gu, EDL 2012

Critical issue #5: co-integration of nFETs and pFETs

The challenge: cost-effective co-integration of nFETs and pFETs on Si substrate

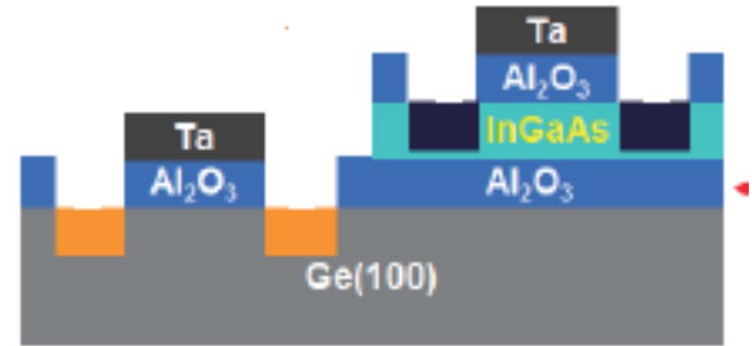
- Different channel materials
- Different lattice constants
- Planar surface
- Thin buffer layer
- Compact
- Low defectivity

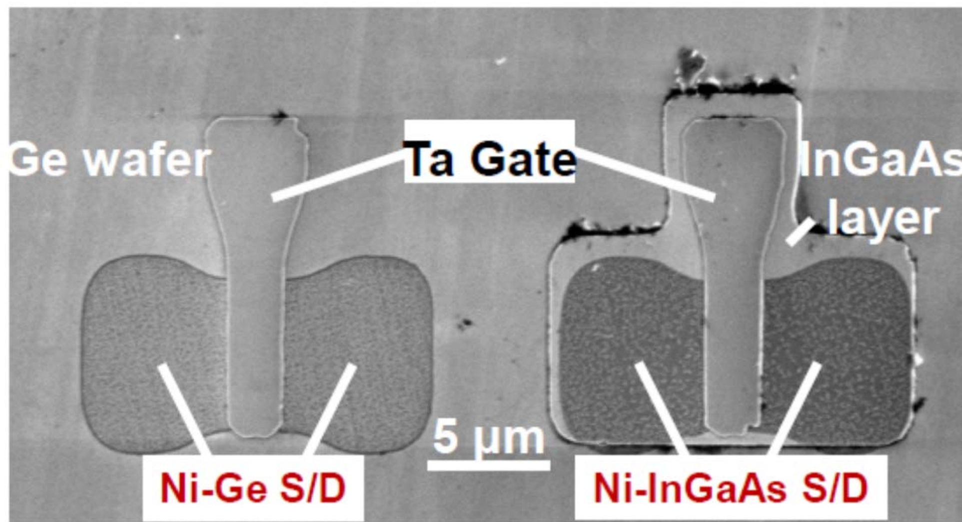


Fiorenza ECS 2010

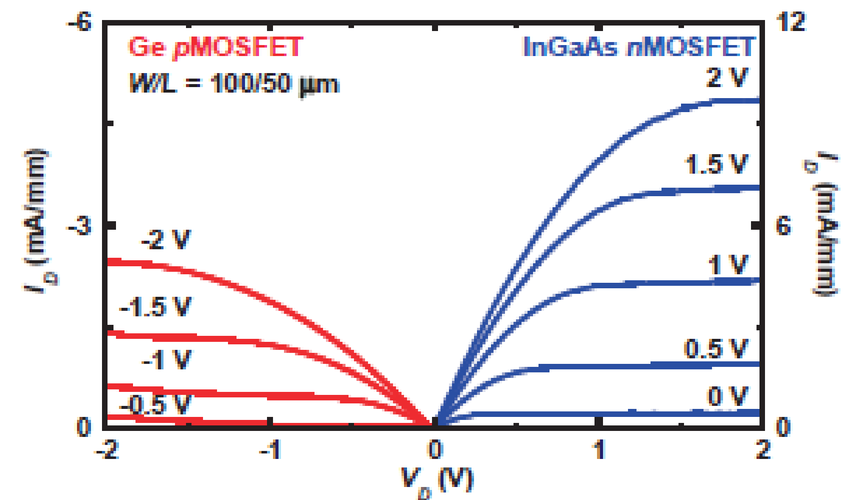
Direct Wafer Bonding

Dielectric bonding of InGaAs/InP wafer and Ge wafer





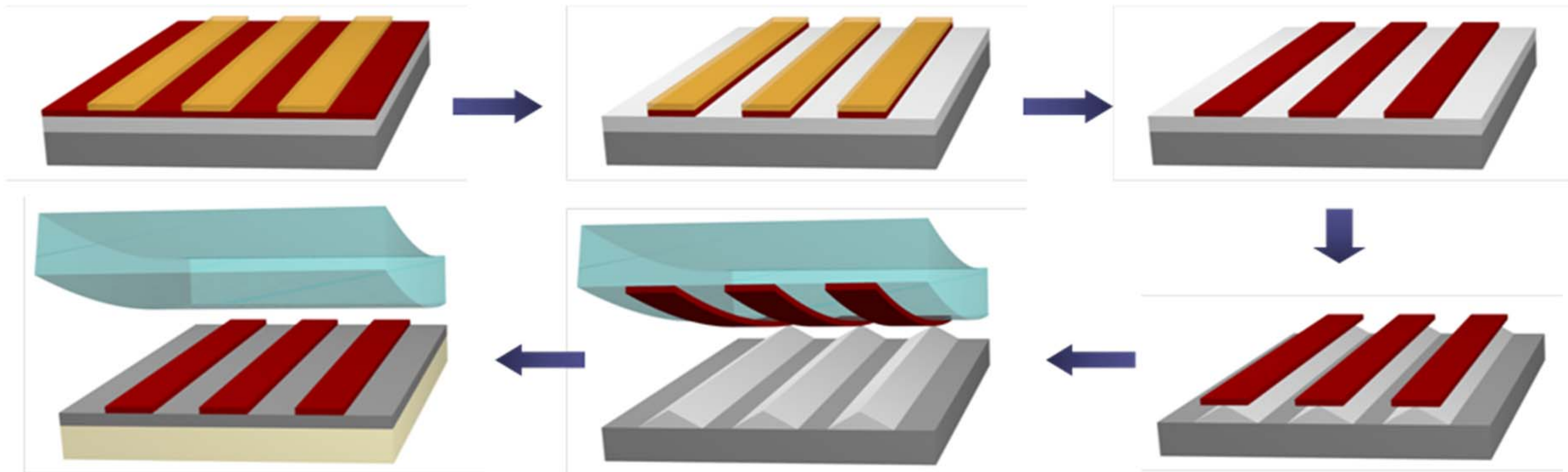
Yokoyama, VLSI Tech 2011



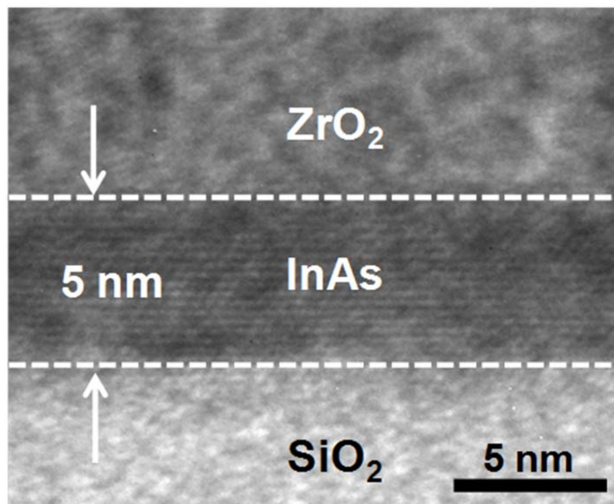
Device surfaces at two different levels

III-V on Insulator (XOI)

XOI platform: epitaxial layer transfer onto Si/SiO_2 substrate



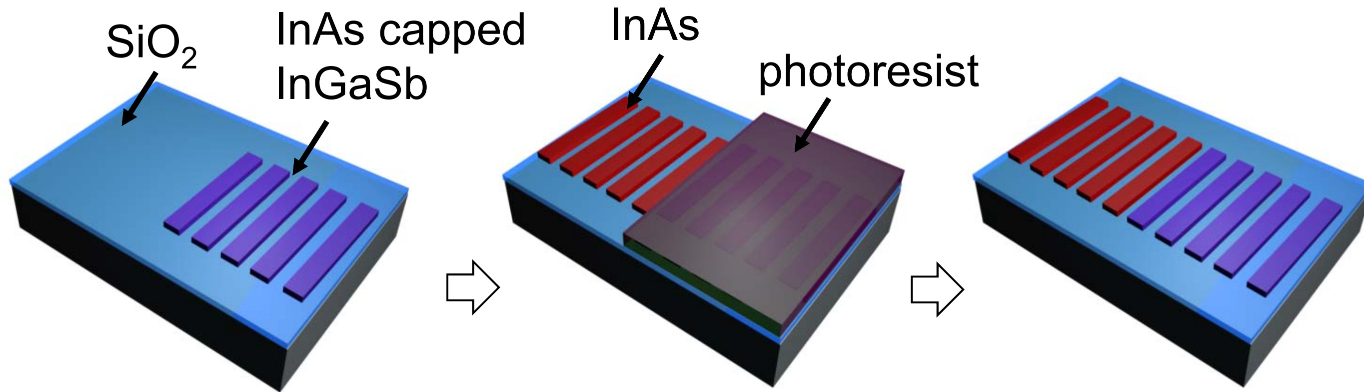
Produces freestanding materials on a receiver substrate

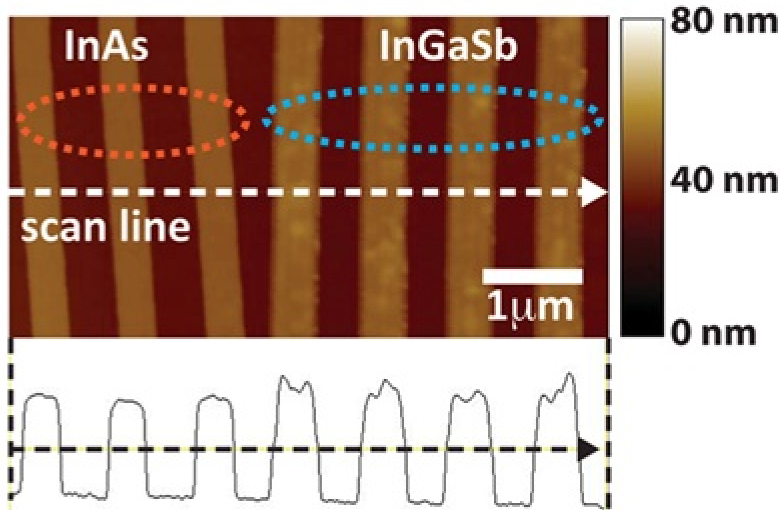


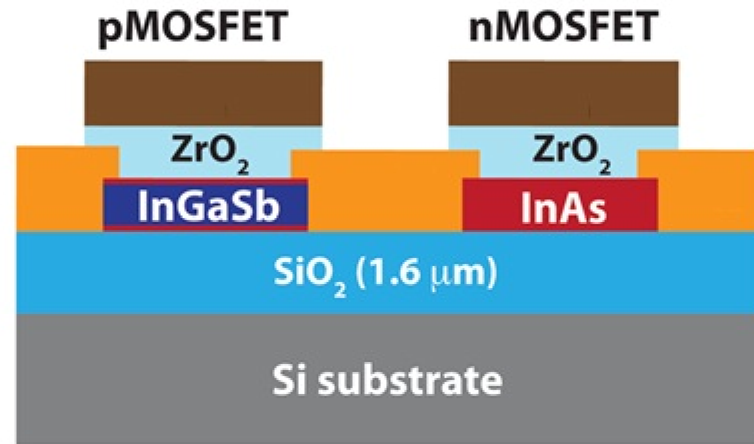
- Single crystal material
- Strain preserved
- Void-free interfaces

Ko, Nature 2010

III-V CMOS on Si







2-step transfer process

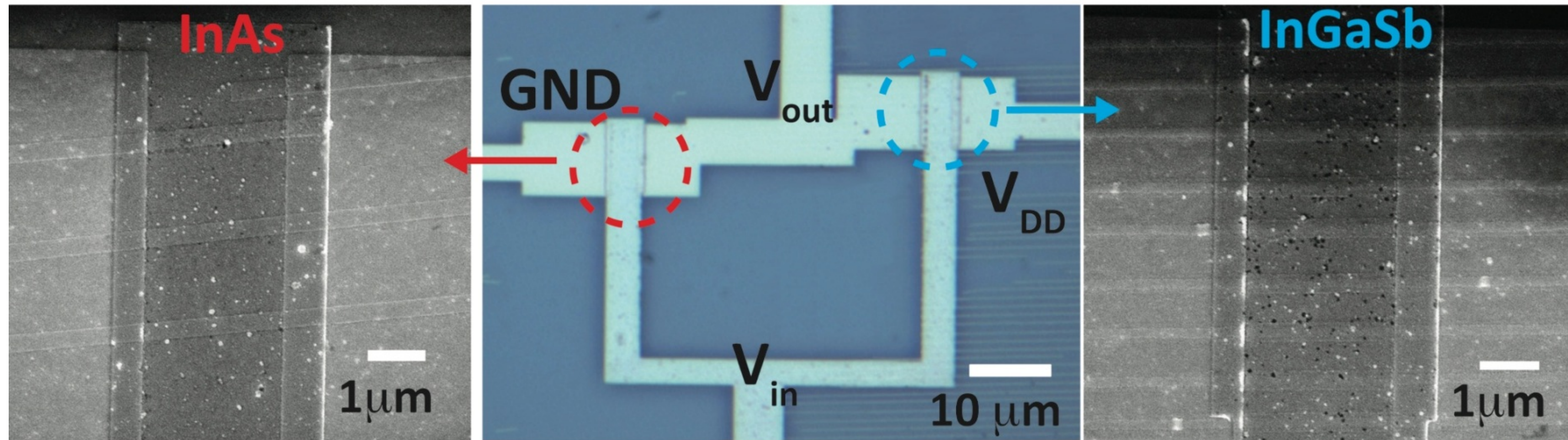
nFET: InAs (8 nm)

pFET: InAs/$In_{0.3}Ga_{0.7}Sb$/InAs: 2.5/7/2.5 nm

Both grown on GaSb wafer

Nah, Nano Lett 2012

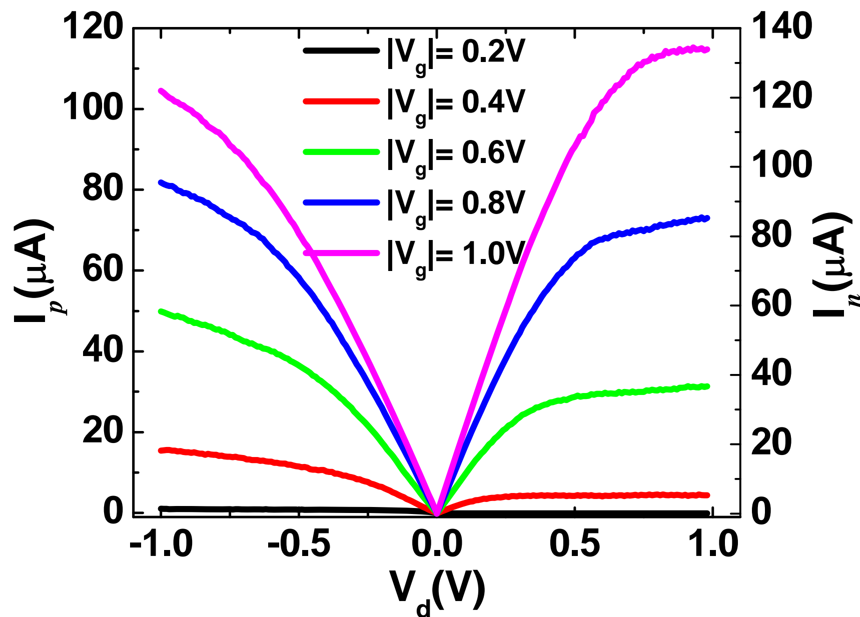
III-V CMOS on Si

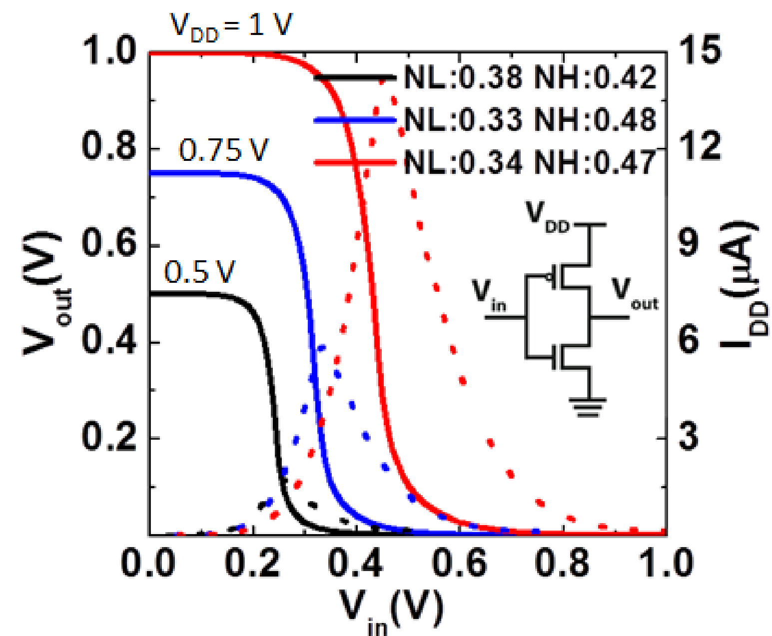


L_G = 2.9 μm

Nah, NanoLett 2012

L_G = 2.6 μm

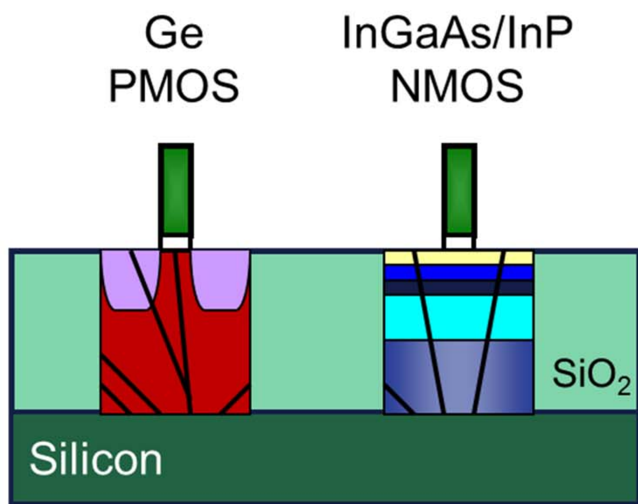




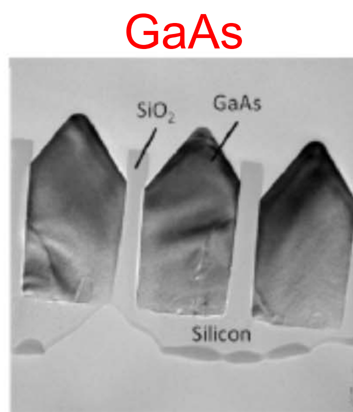
1st III-V CMOS on Si based on InAs n-FETs and InGaSb p-FETs

Aspect Ratio Trapping

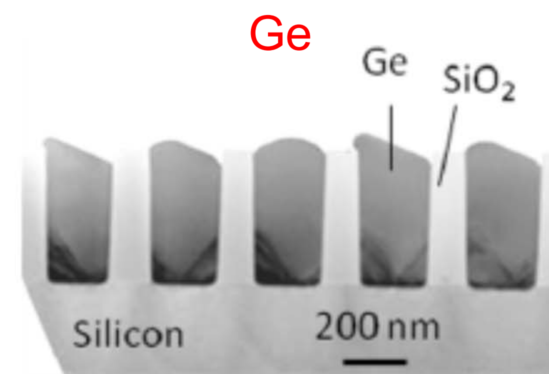
Growth in high aspect ratio trenches: dislocations “trapped” at sidewalls



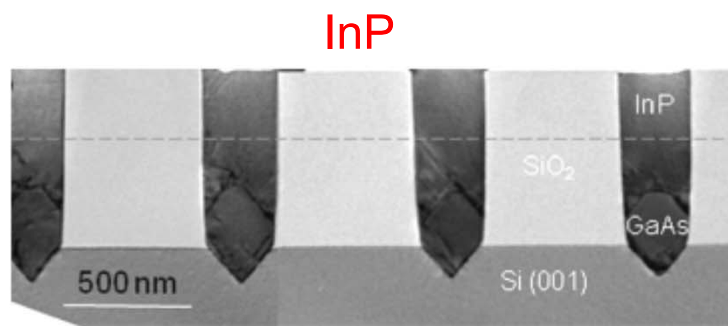
GaAs

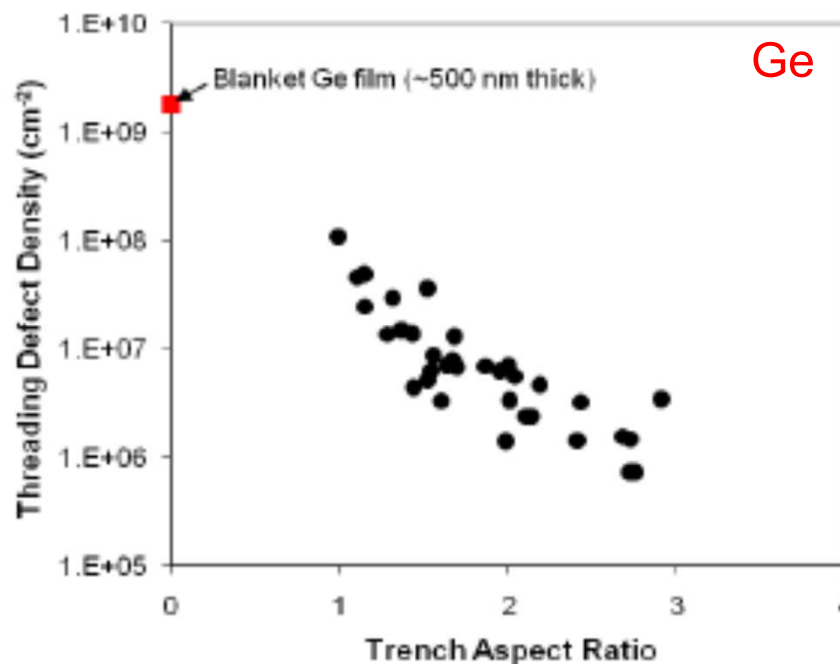


Ge



InP



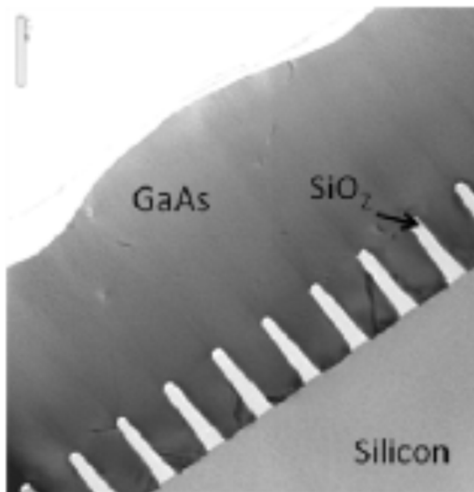


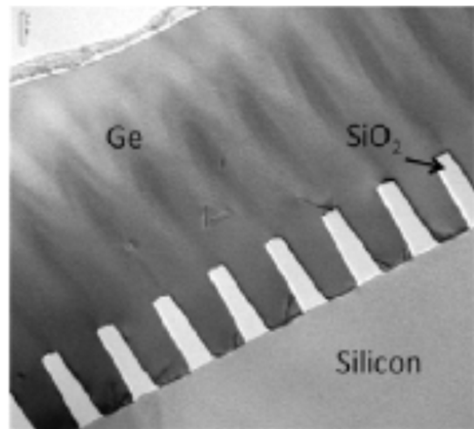
Fiorenza ECS 2010

Aspect Ratio Trapping + Epitaxial Lateral Overgrowth

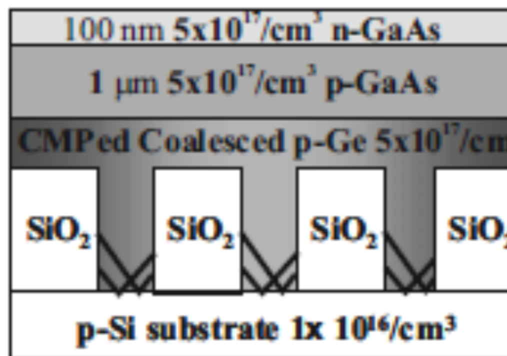
Planar surfaces obtained by epitaxial lateral overgrowth following ART

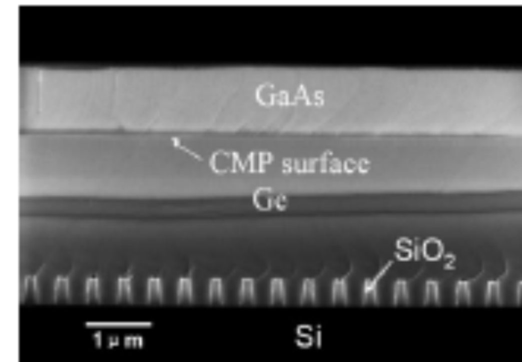
GaAs MOSFETs demonstrated



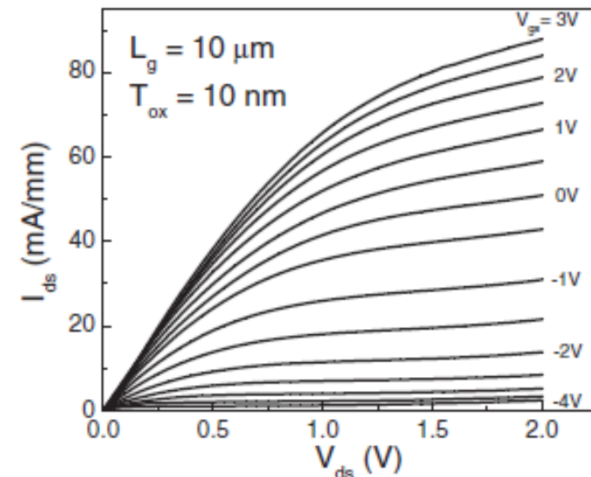


Fiorenza ECS 2010

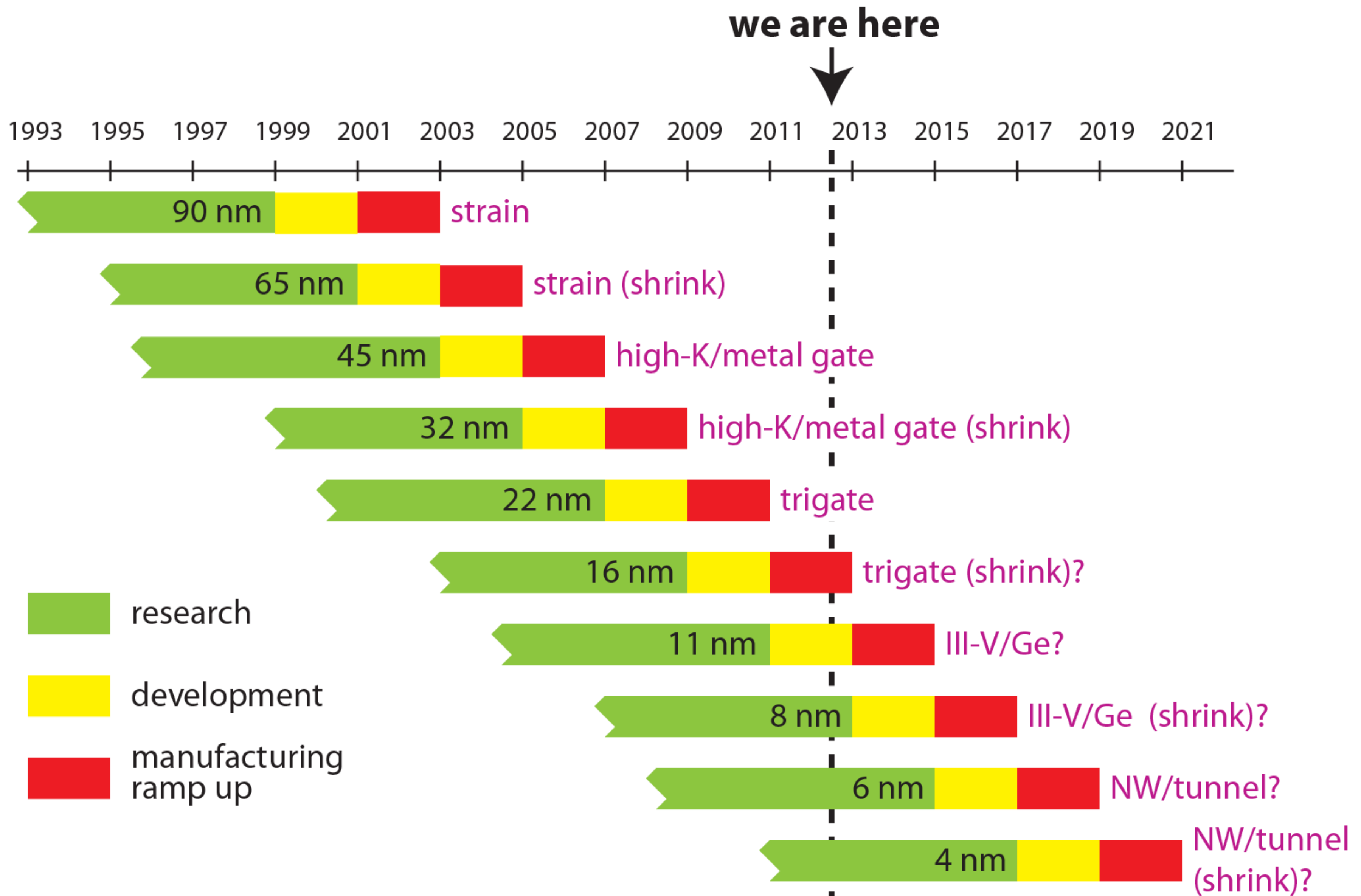




Wu, APL 2008

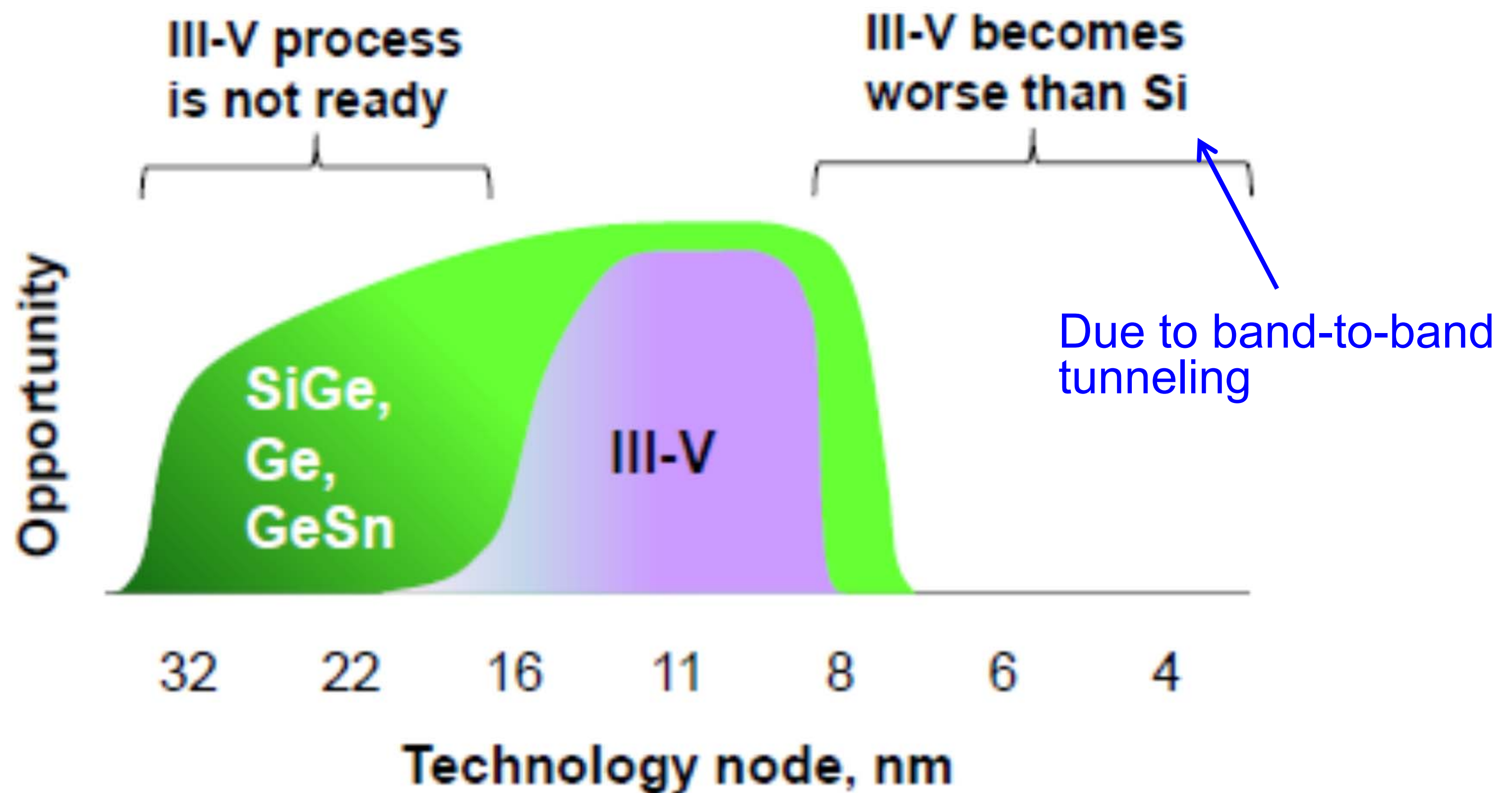


5. CMOS R&D roadmap*



*grossly oversimplified and biased towards Intel

III-Vs in CMOS: narrow window of opportunity



V. Moroz, UCB Seminar 2011

Conclusions

- New materials coming into CMOS roadmap:
  - InGaAs most promising III-V for n-MOSFET
  - InGaSb most promising III-V for p-MOSFET, also Ge

- Lots of fundamental research needed to chart a path for CMOS beyond Si:
  - Interface physics and chemistry with III-Vs
  - Structures for sub-10 nm gate lengths
  - MOS gate stack reliability
  - Integration of n-channel and p-channel devices based on different materials onto Si substrate