VLSI June 14th 2012

Accelerating the next technology revolution

InAs Quantum-Well MOSFET with Record High g_m, f_T and f_{max}

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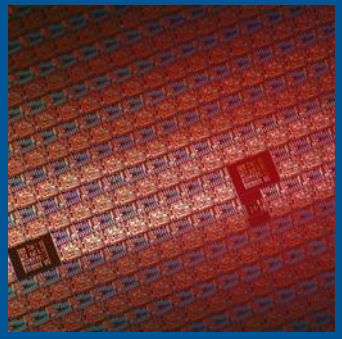


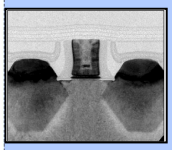
Outline

- Introduction
- Device design and process technology
- Device results from logic to microwave characteristics
- Conclusions

Possible Logic Technology Roadmap

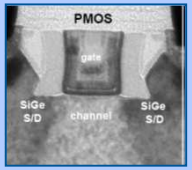
Manufacturing

HKMG 2007



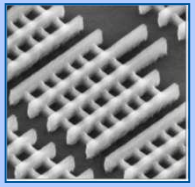
Intel

2nd Gen HKMG 2009



Intel,

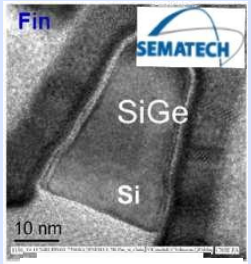
Si FinFET 2012

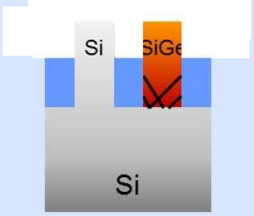


Intel

Development

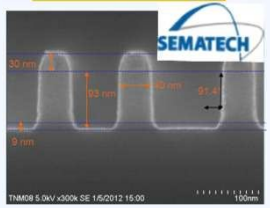
Ge pMOS; Si nMOS 2015

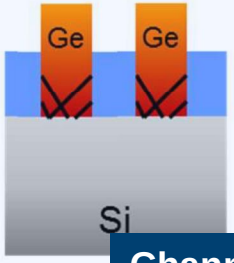




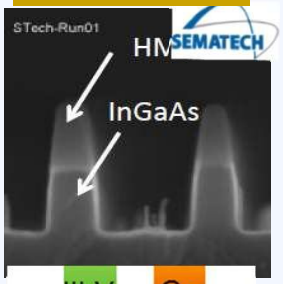
Pathfinding

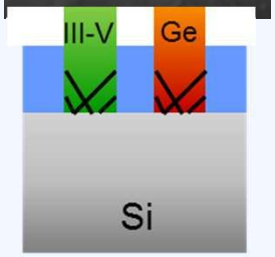
Ge CMOS 2017



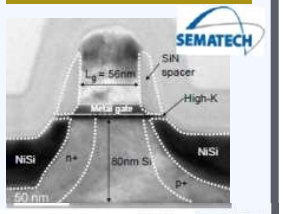


Ge pMOS; III-V nMOS 2019

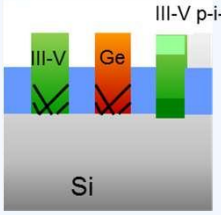




ULP TFET 2021



III-V p-i-n TFET



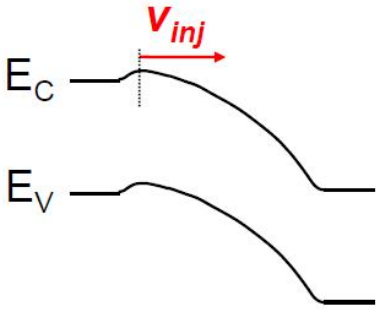
Channel Material

- Defect Metrology
- Junctions
- Gate Stack
- Manufacturability

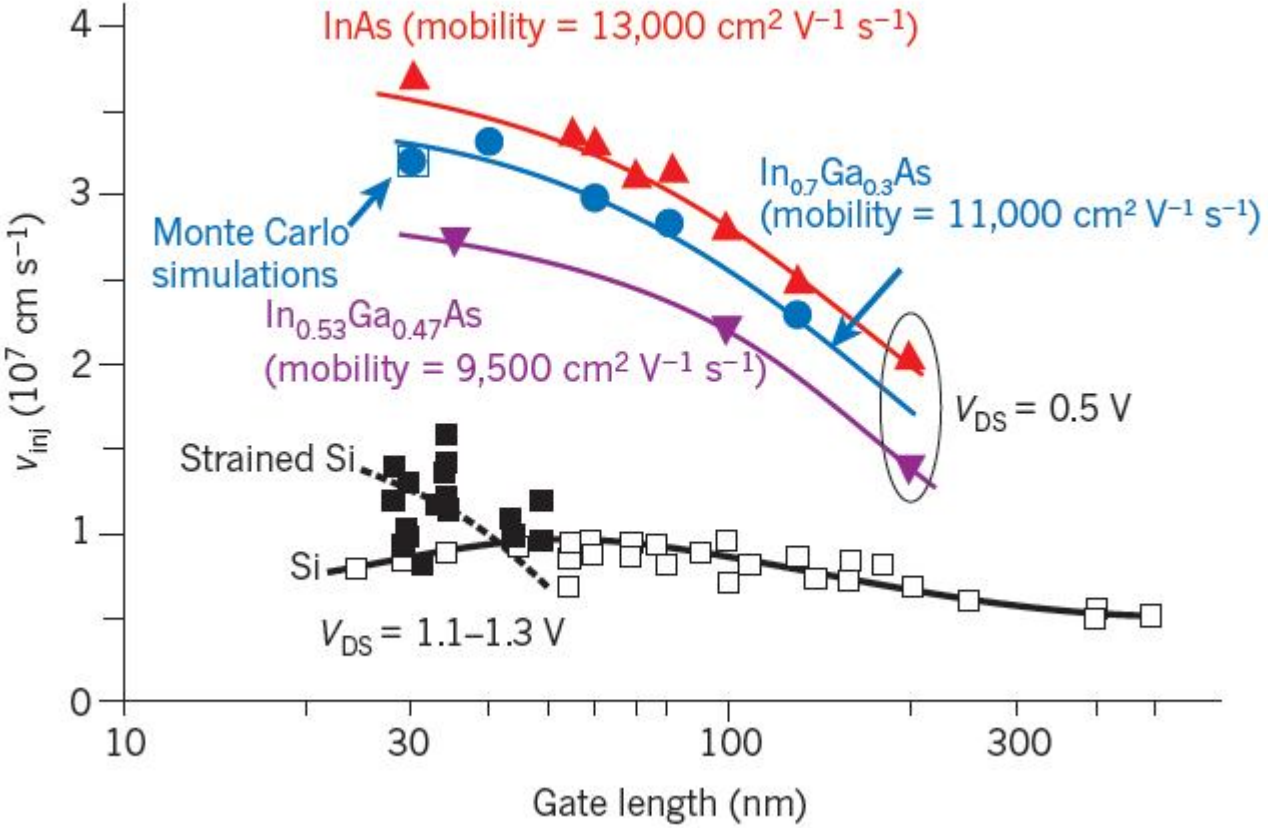
- Gate stack
- Sub 60mV
- Architecture
- Junction / Doping

45nm — 32nm — 22nm — 14nm — 10nm — 7nm — 5nm

Motivation for InAs vs. InGaAs

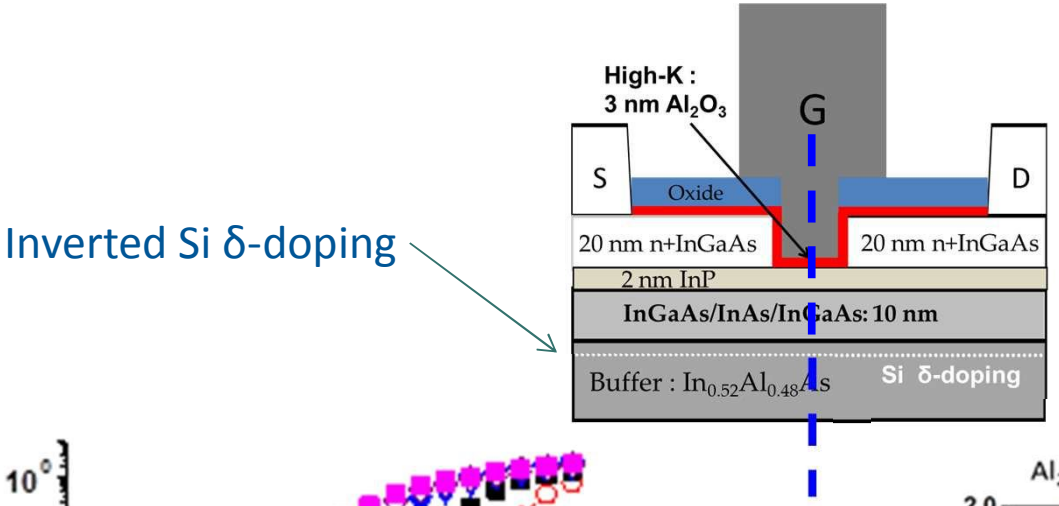


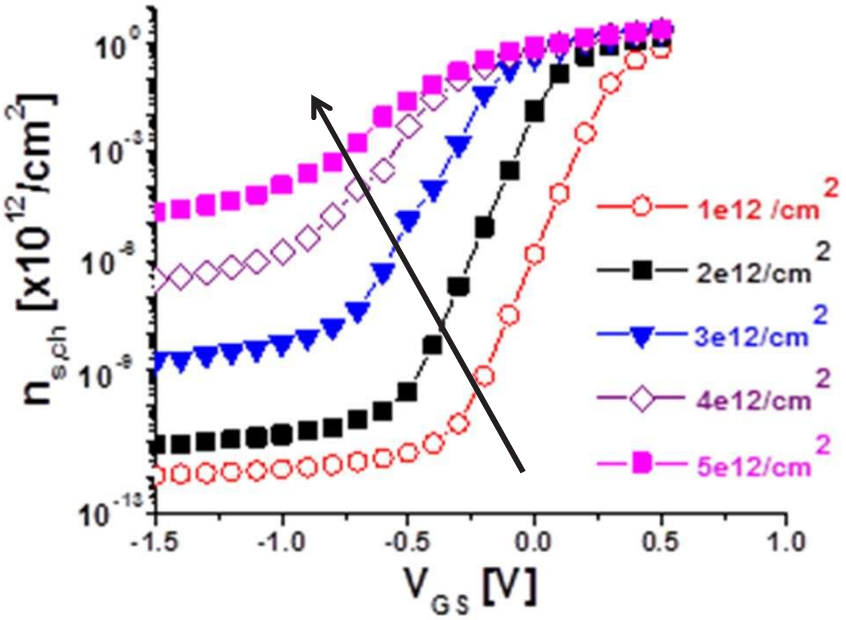
<del Alamo, Nature 2012>
<Kim, IEDM 2009>

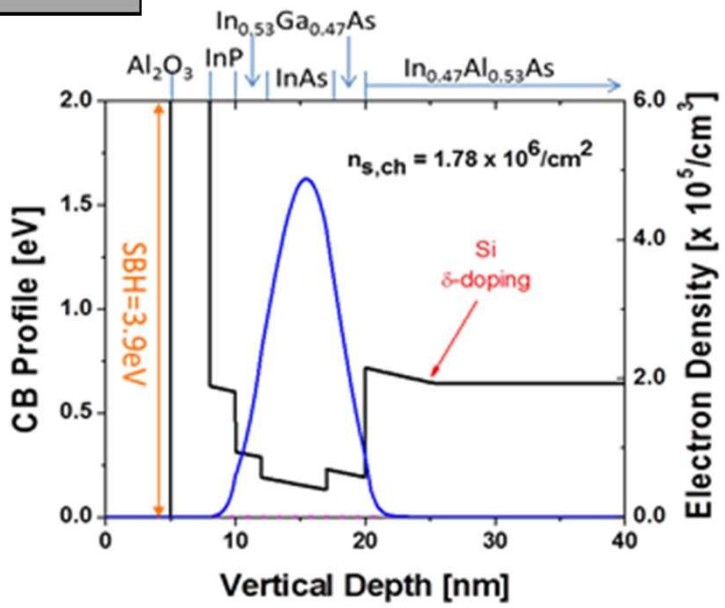


- v_{inj} (InAs>$In_{0.7}Ga_{0.3}As$/$In_{0.53}Ga_{0.53}As$) > $2v_{inj}$(Si) at less than half V_{DD}
- Derived v_{inj} values consistent with quasi ballistic transport (Collision-free)

Layer structure with inverted Si δ-doping



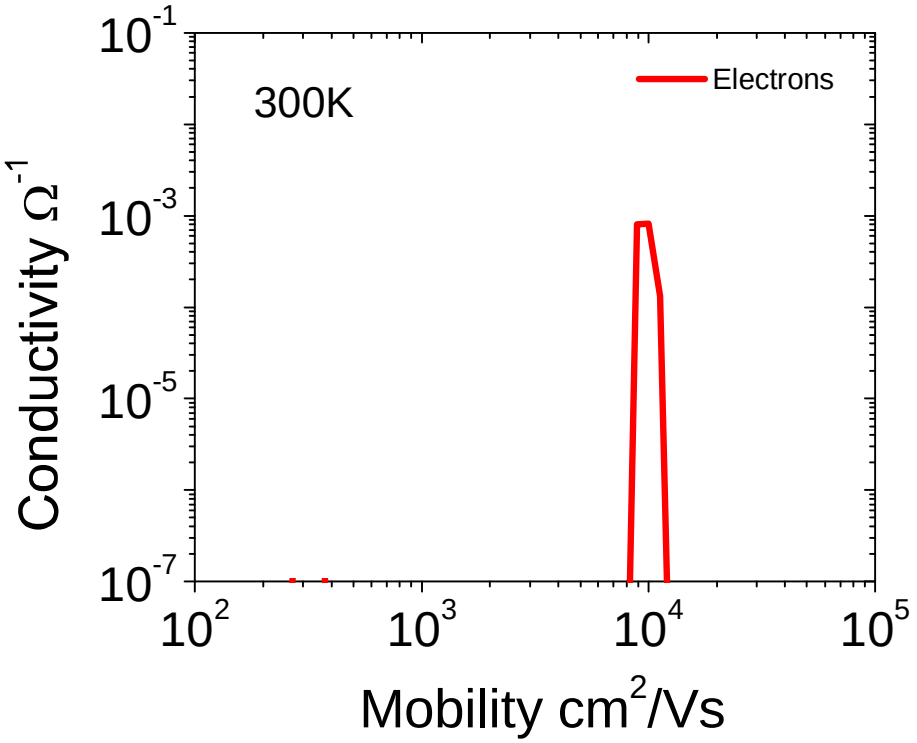


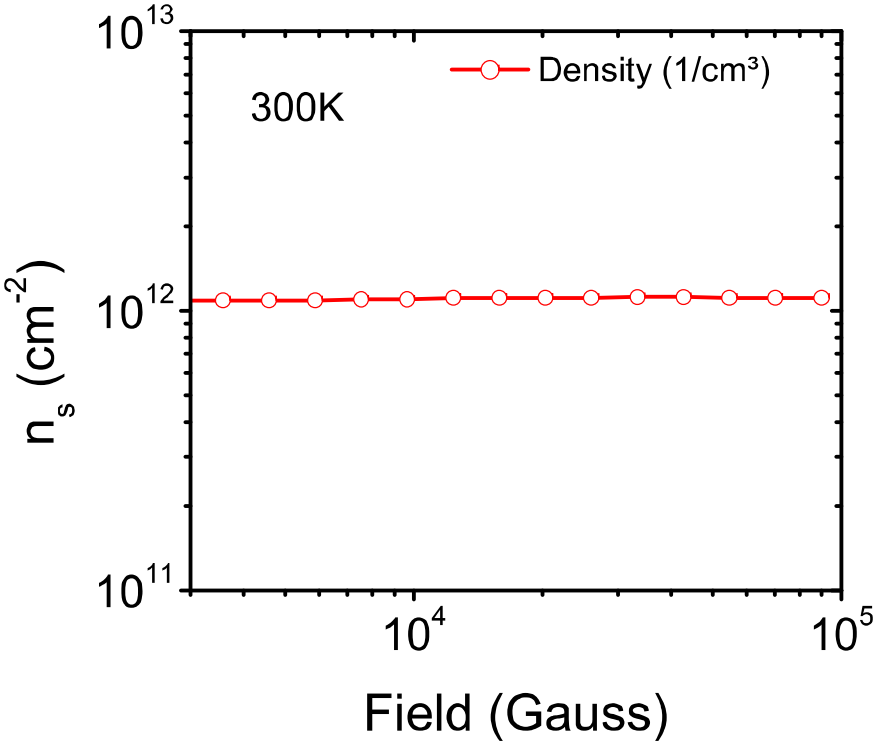


- Optimize Si δ-doping to better electrostatics

Validation of epi quality in this work

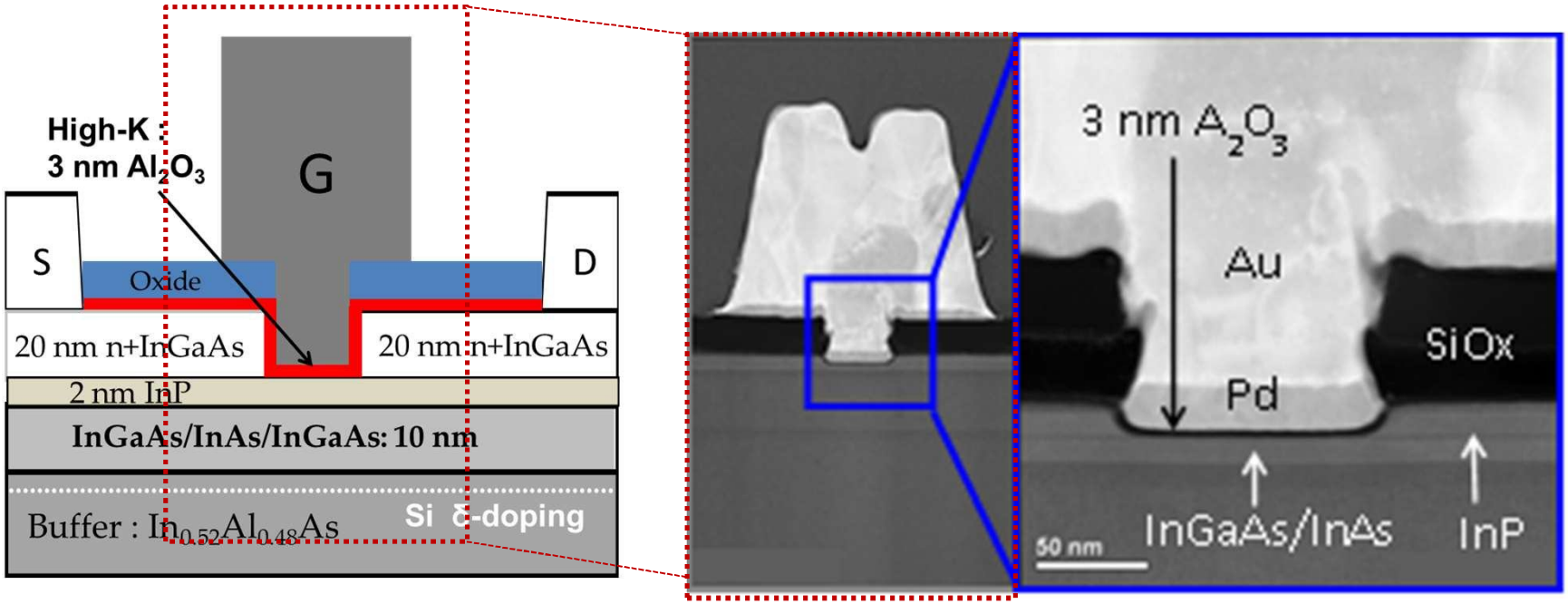
- QMSA results from calibration structure





- $\mu_{n,Hall}$ = 11,200 cm^2/V-sec and $n_{s,ch}$ = 1 x 10^{12}/cm^2 at 300K
- $\mu_{n,Hall}$ = 20,000 cm^2/V-sec and $n_{s,ch}$ = 1 x 10^{12}/cm^2 at 77K

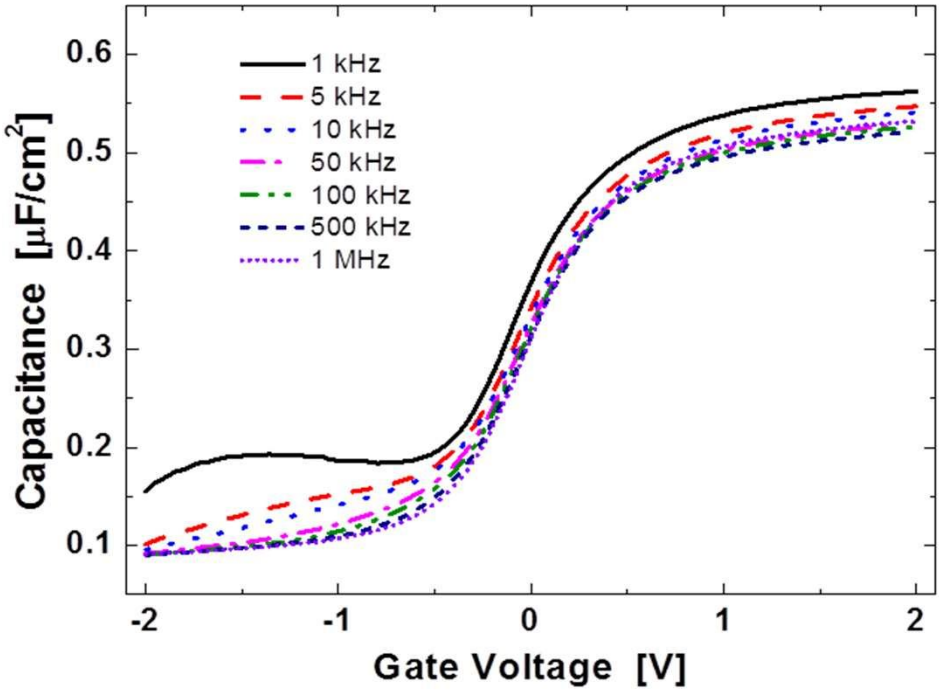
Test Structure Design

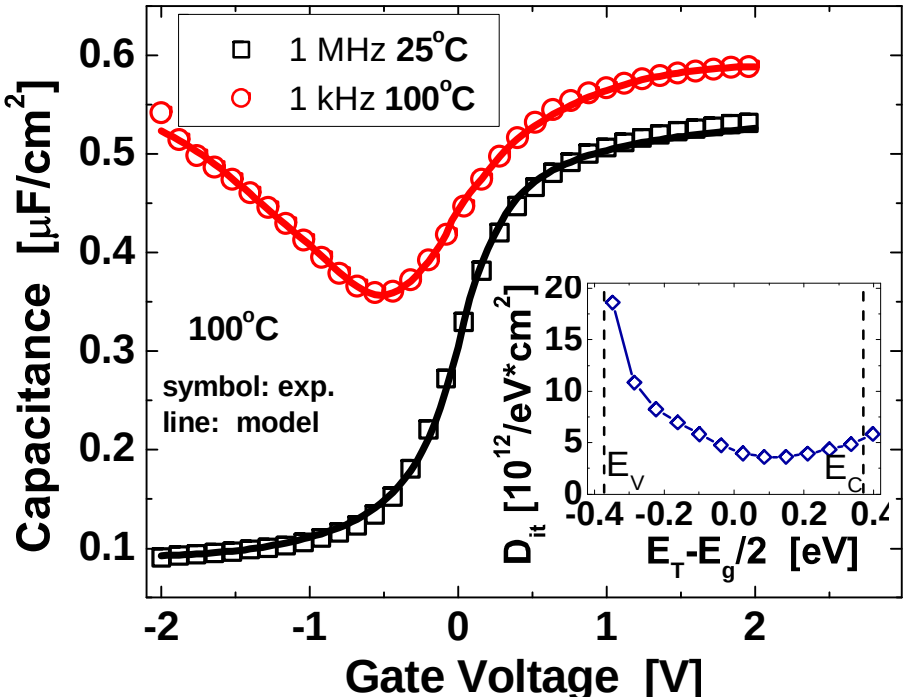


Unique features of this work:

- InAs channel for better transport
- Inverted Si δ-doping for low excess R_{SD} and excellent electrostatic control
- 3 nm Al_2O_3/2 nm InP gate stack to improve D_{it}

SEMATECH Generalized Technique[1)] for D_{it}

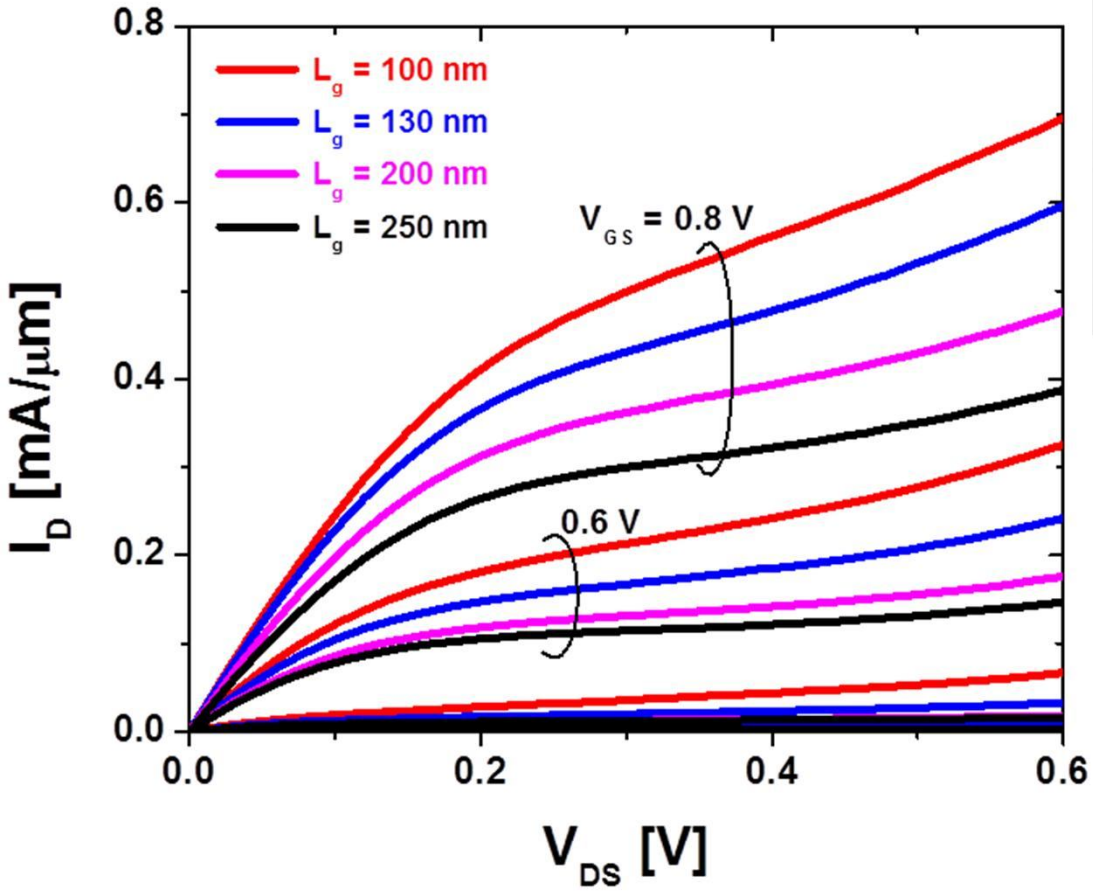


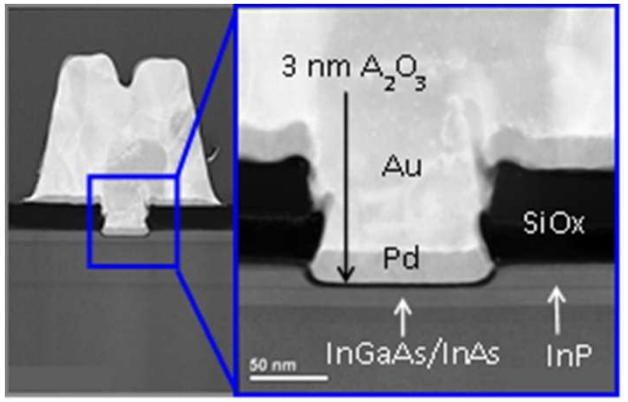


- Low frequency dispersion in both accumulation and depletion region
- D_{it} = 4 x 10^{12} /eV.cm^2 from temperature High-Low frequency and Terman D_{it} extraction method

1) M. Madan, DRC, p. 117 (2011)

InAs MOSFET Output Characteristics

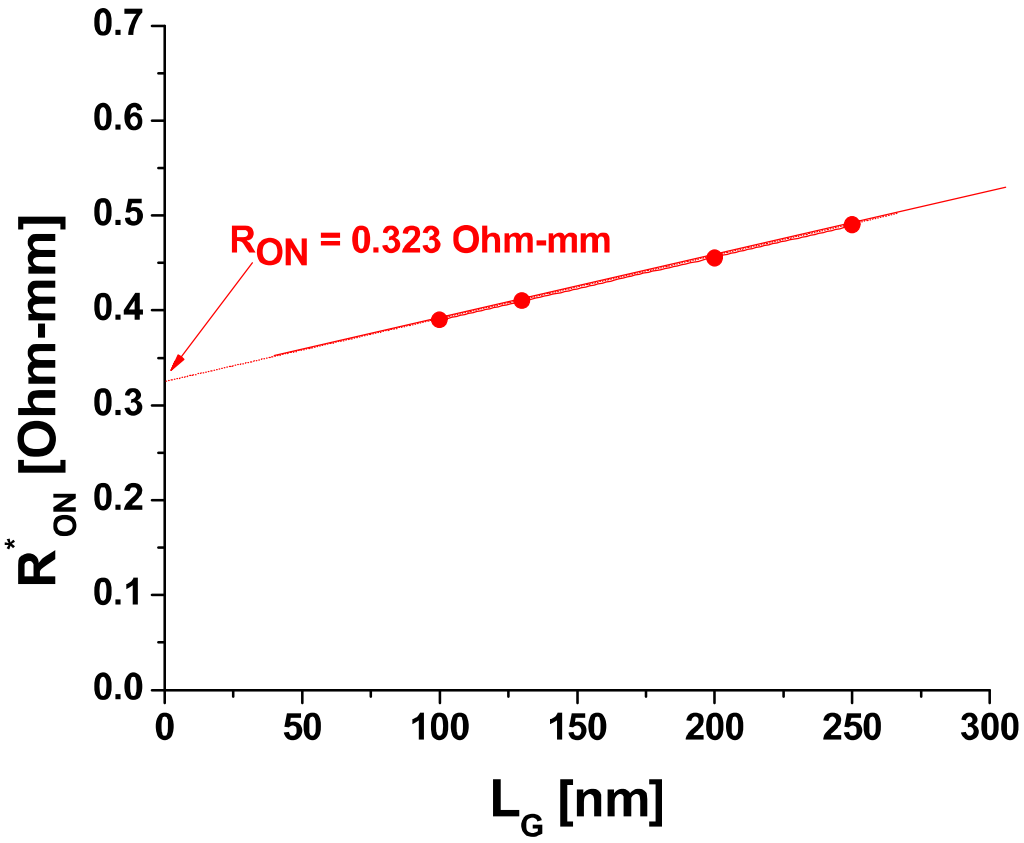




Optimized gate recess with L_{side} < 5 nm

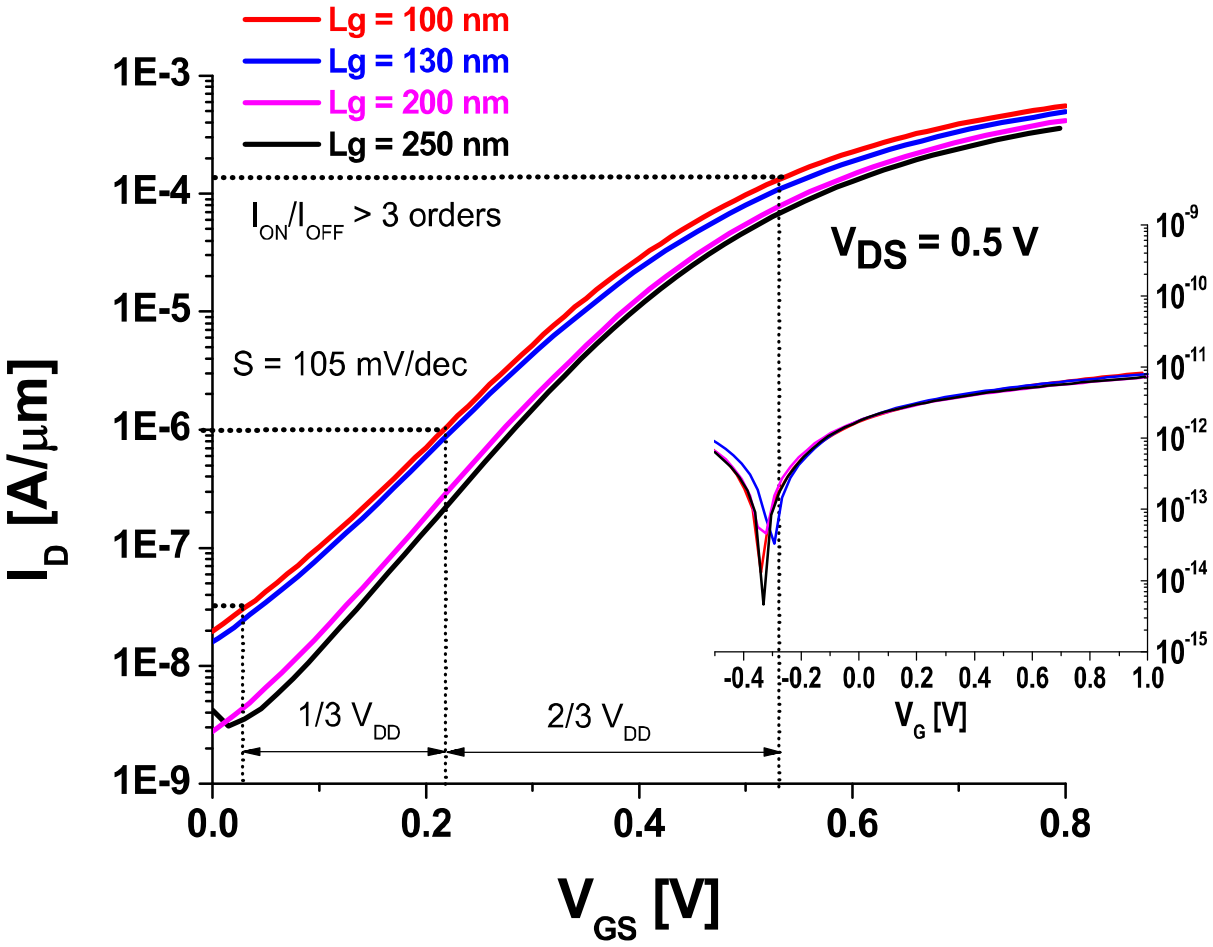
- Excellent I_D saturation and pinch off behavior
- $I_{D,sat}$ = 0.68 A/mm at V_{DS} = 0.6 V at L_g = 100 nm

R_{ON} Characteristic



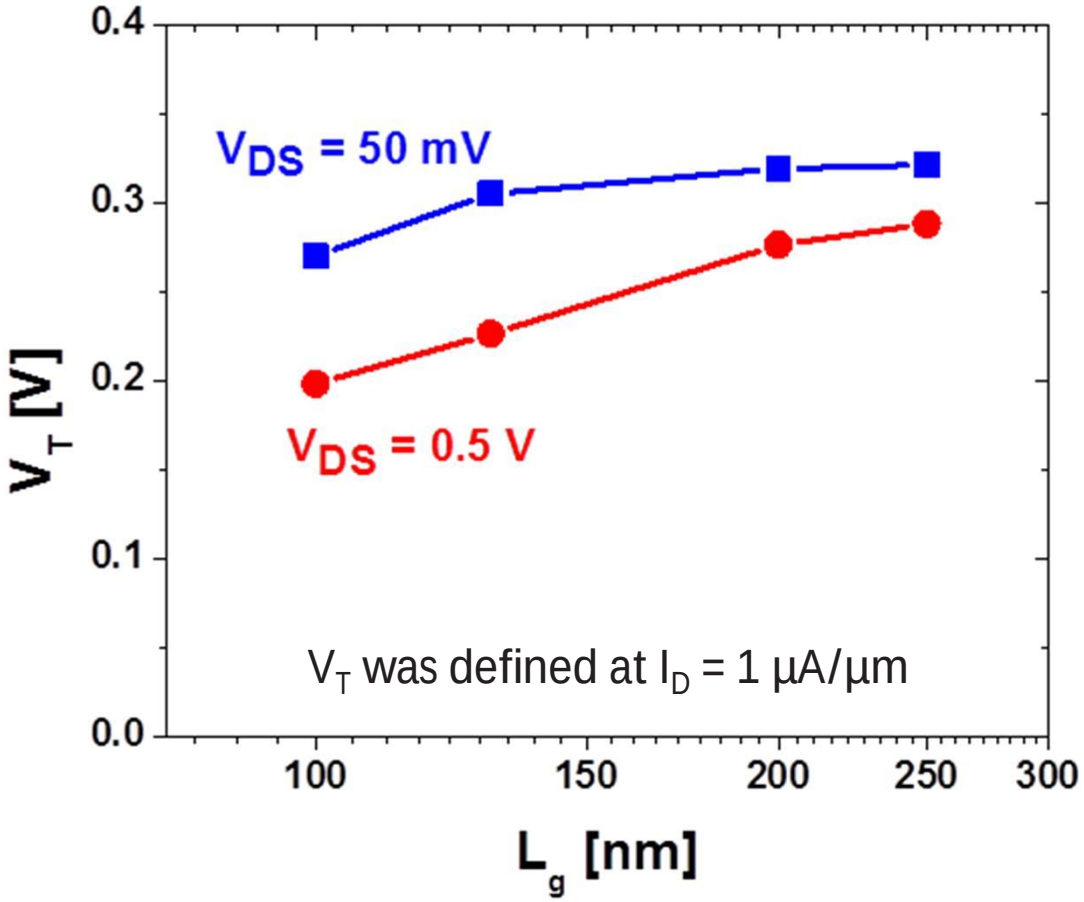
- R_{ON} = 0.323 Ohm-mm with optimized gate recess process (L_{side} < 5 nm)
- R_{ON} could be reduced with self-aligned architecture

InAs MOSFET Subthreshold Characteristics



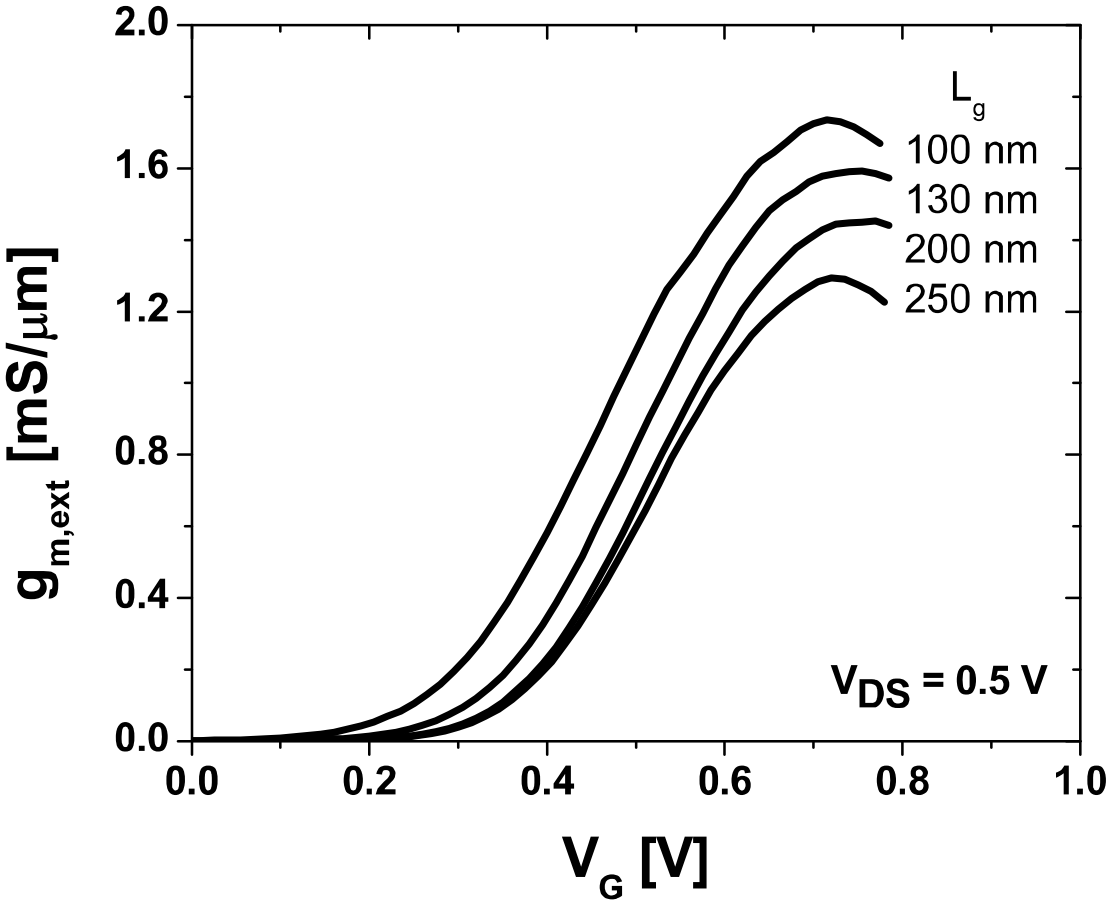
- SS = 105 mV/dec. at L_g = 100 nm with D_{it} = 4 x 10^{12} /eV.cm^2
- Excellent gate leakage ➔ A room for EOT scaling below 2 nm

V_T roll-off



- V_T = 0.2 V at L_g = 100 nm: Enhancement-mode operation

InAs MOSFET g_m Characteristic

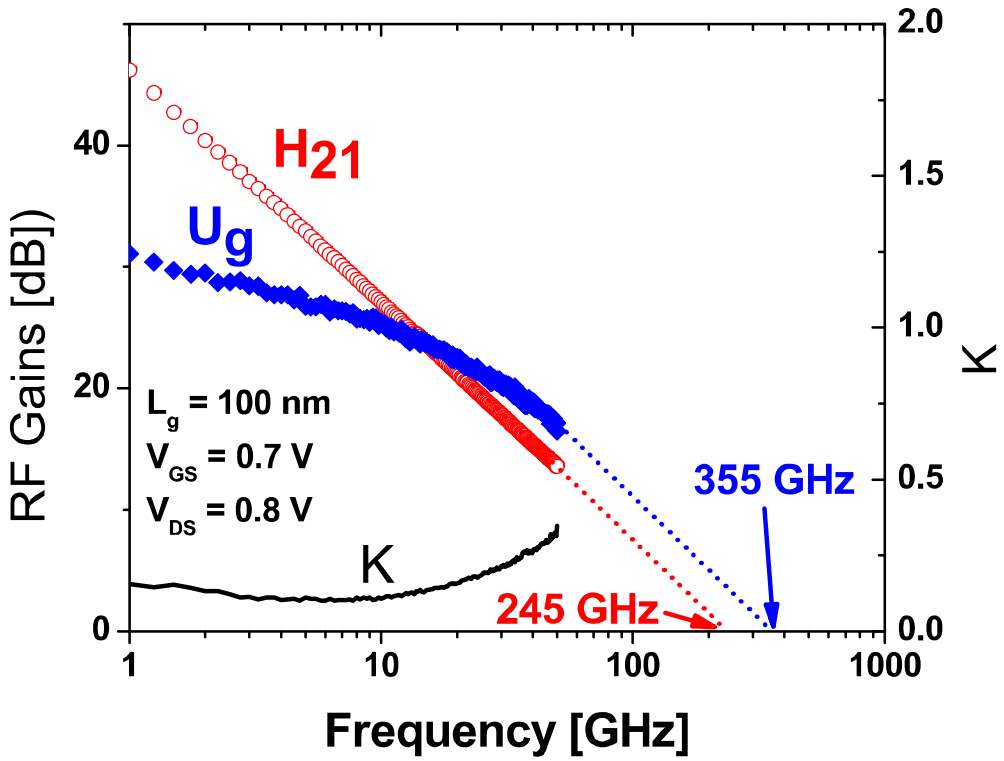


$g_{m,int} = C_g \times v_{inj}$

g_m = 1.73 mS/μm at V_{DS} = 0.5 V (A record $g_{m,ext}$ at L_g = 100 nm)

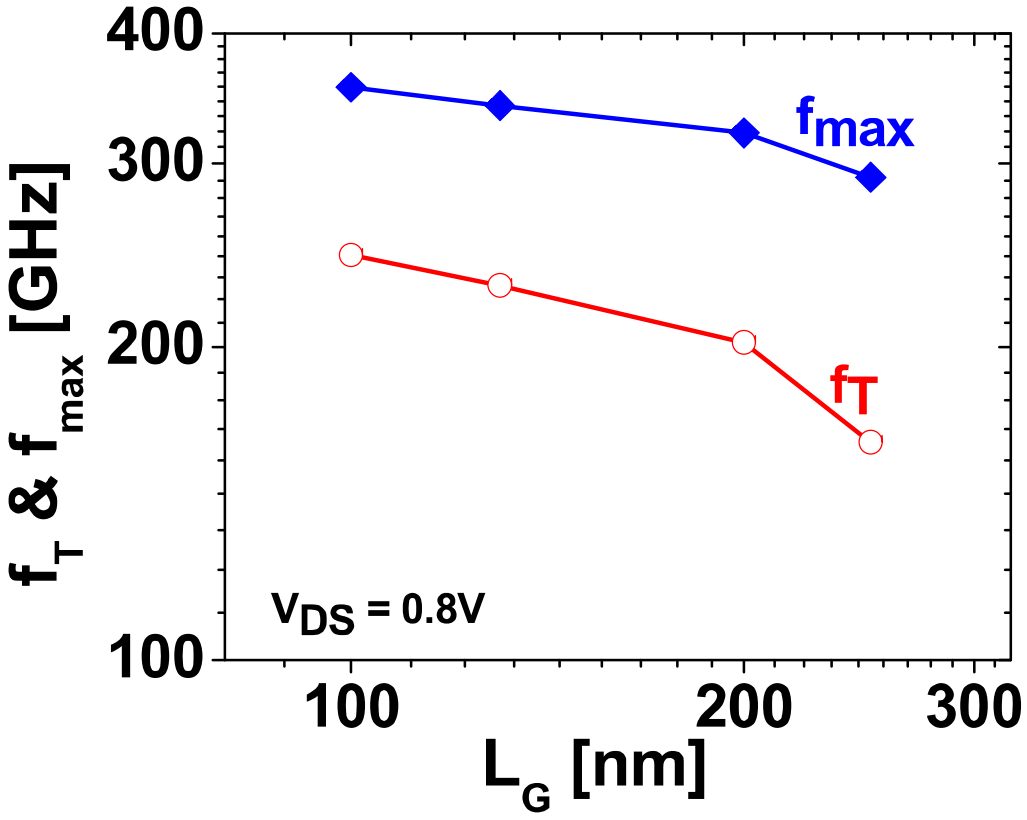
InAs MOSFET Microwave Characteristic

Calibration: LRRM, De-embedding: OPEN/SHORT



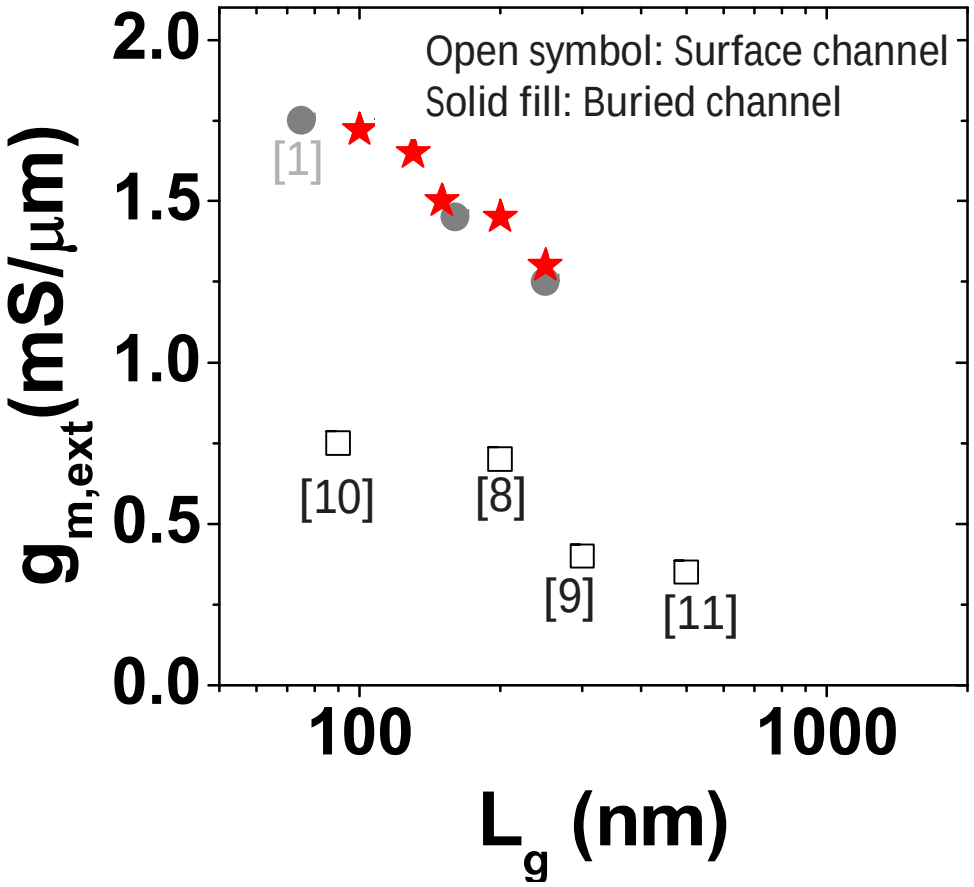
- L_g = 100 nm: f_T = 245 GHz & f_{max} = 355 GHz at V_{DS} = 0.8 V
  ➔ These f_T & f_{max} are record values for any III-V MOSFET

InAs MOSFET promising for RF Applications



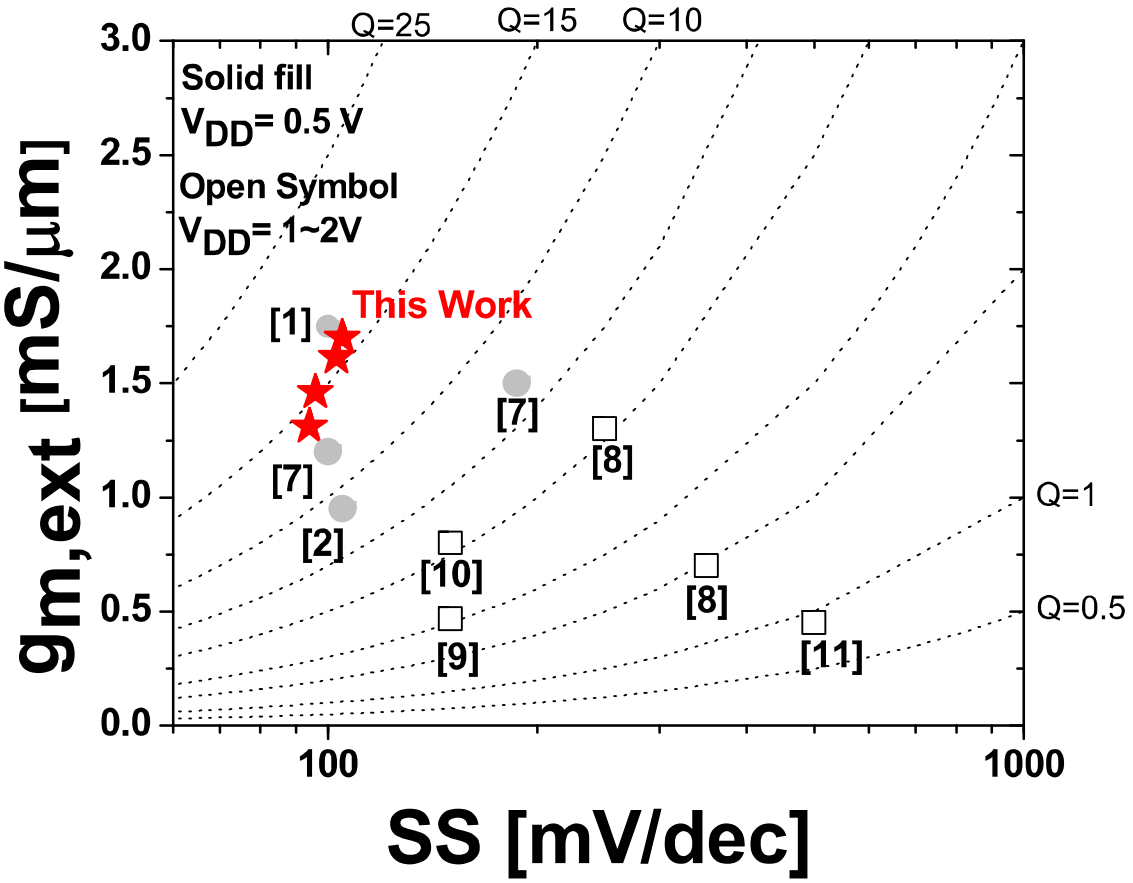
- L_g = 200 nm: f_T > 200 GHz & f_{max} = 300 GHz at V_{DS} = 0.8 V
- Excellent performance for millimeter wave applications

III-V MOSFET Benchmarking



- A record transconductance at L_g = 100 nm for III-V MOSFET

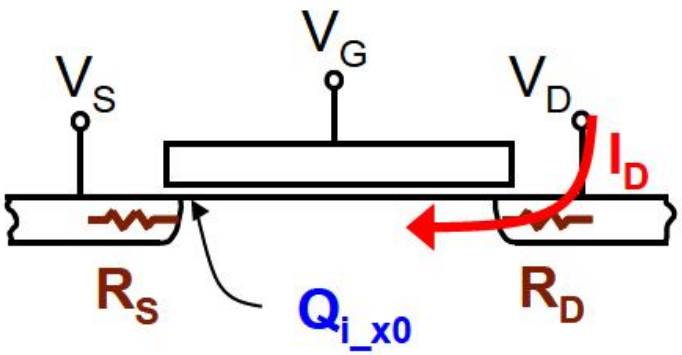
III-V MOSFET Q Benchmarking

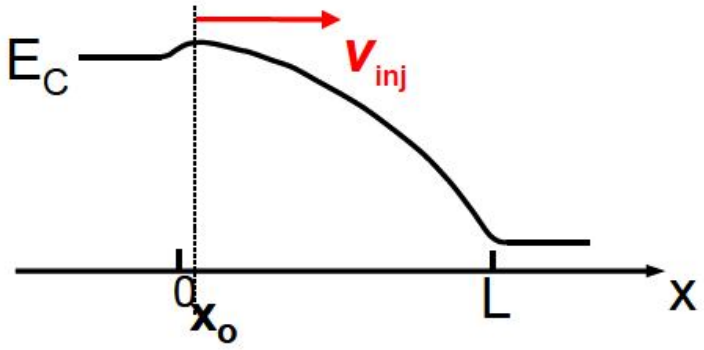


- FOM Q factor defined as g_m/S

  Q = 16 for L_g = 100 nm and V_{DD} =0.5 V.

Extraction methodology for v_{inj}





Kim, IEDM 2009

$$I_D = Q_{i\_x0} \times v_{inj} \Rightarrow v_{inj} = \frac{I_D}{Q_{i\_x0}}$$

- I_D: measured drain current
- Q_{i_x0}: sheet-charge density

$$Q_{i\_x0} = \int C_{gi}\, dV_{GS,i}$$

with C_{gi} @ V_{DS} = 10 mV

- C_{gi} extracted from S-parameters
- R_S and R_D correction:

$$V_{DSi} = V_{DS} - I_D \times (R_S + R_D)$$

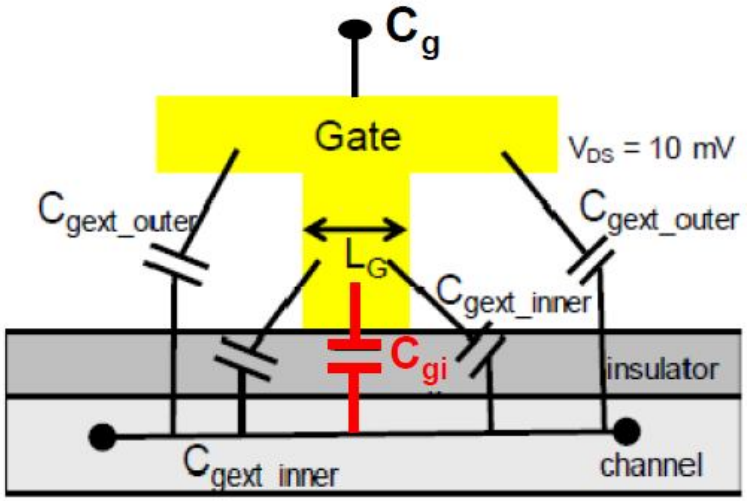
$$V_{GSi} = V_{GS} - I_D \times R_S$$

- V_T roll-off correction
- DIBL correction

C_{gi} – How to extract in small L_g device

C_{gi} → intrinsic gate capacitance per unit area [fF/μm²]

(from S-parameters at linear region, V_{DS} = 10 mV)

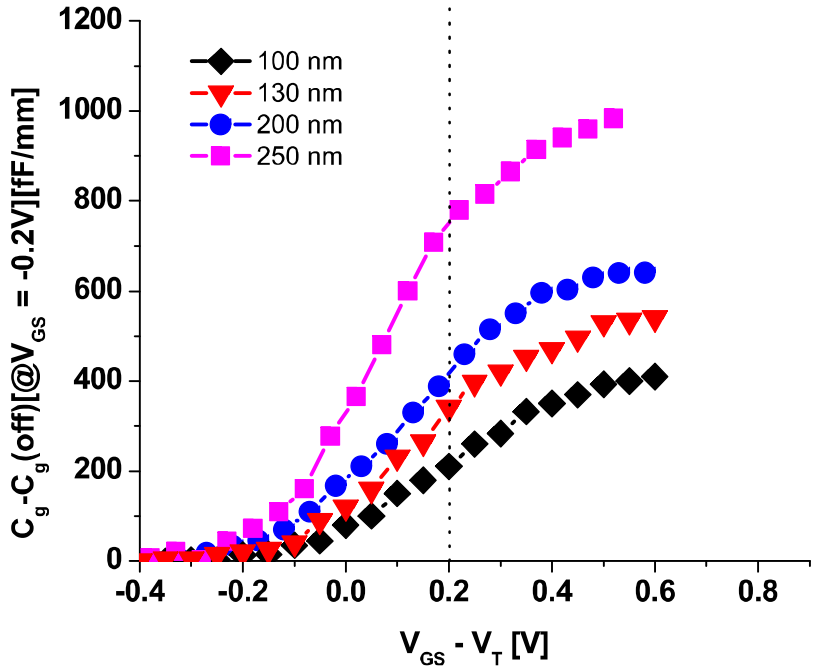


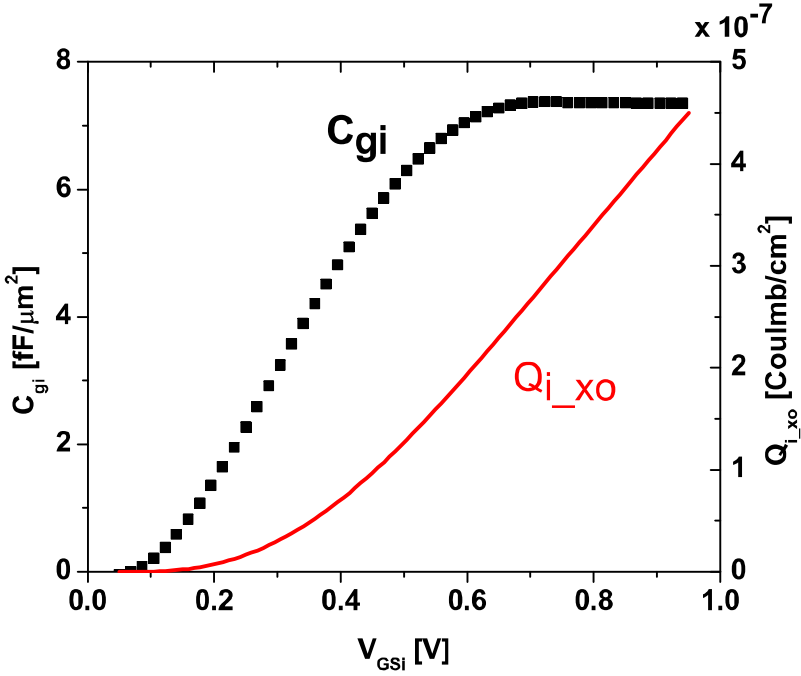
$$C_g = \underbrace{C_{gi} \times L_g + 2C_{gext\_inner}}_{\propto f(V_{GSi} - V_T)} + \underbrace{2C_{gext\_outer}}_{\approx C_g \text{ @ OFF}}$$

$$\rightarrow C_g - C_g(OFF) = \mathbf{C_{gi} \times L_g} + 2C_{gext\_inner}$$

Q_{I_xo} – How to extract

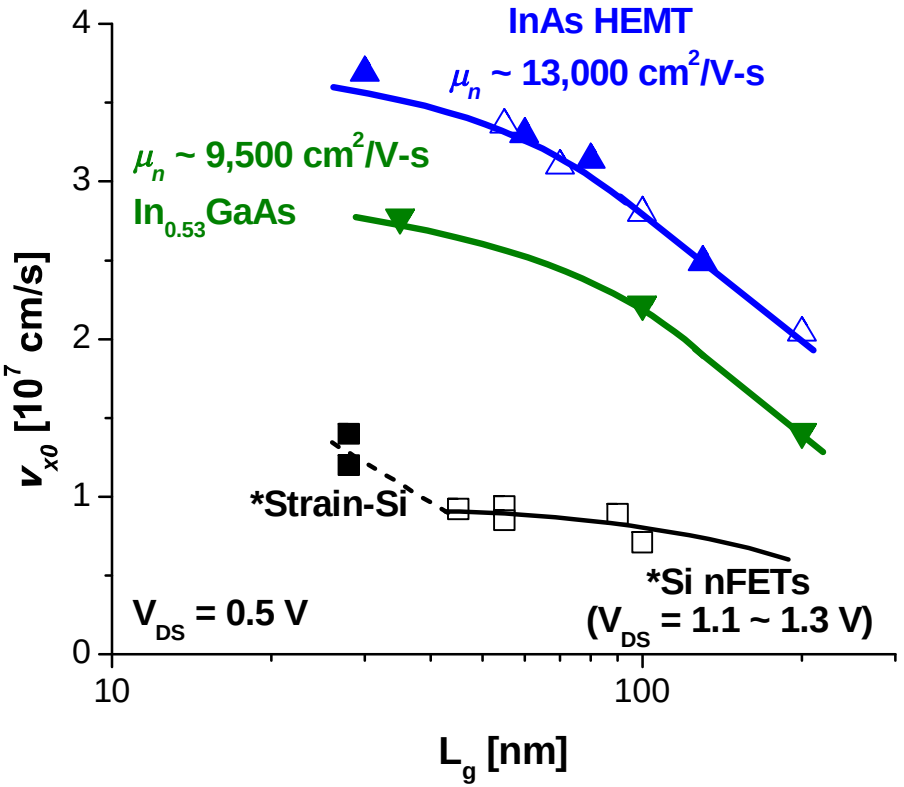
$$Q_{i\_x0} = \int C_{gi}\, d(V_{GS,i}), \text{ where } C_{gi} @ V_{DS} = 10 \text{ mV}$$





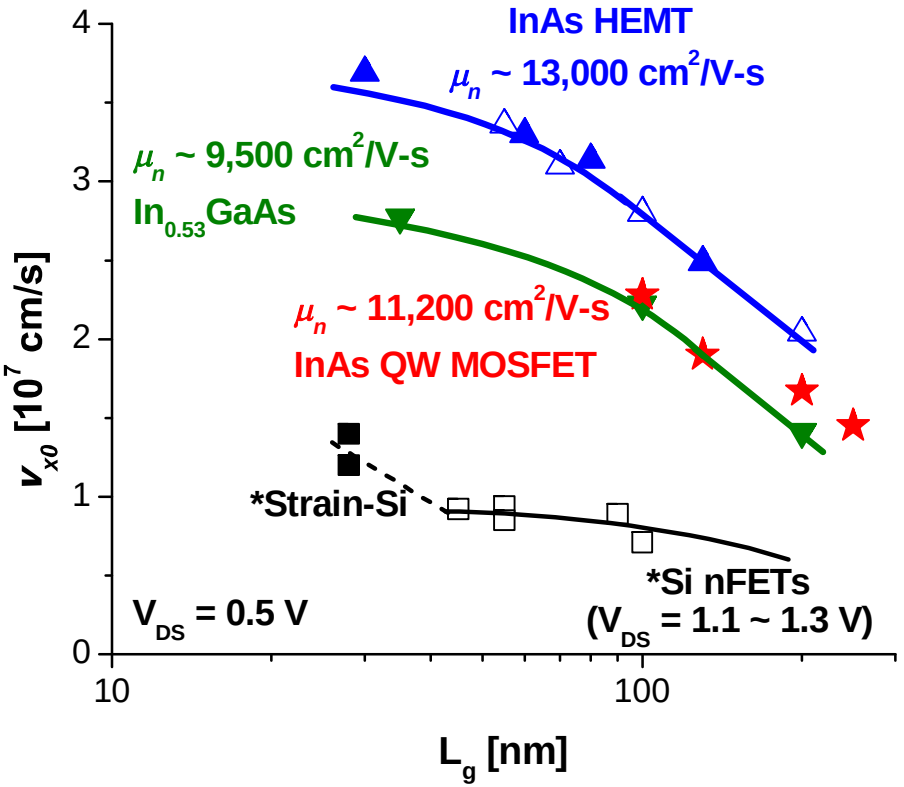
- Extracted intrinsic gate capacitance (C_{gi}) & charge (Q_{i_xo}) in channel with S-parameter

Benchmarking: Injection velocity (v_{inj})



- InAs MOSFET shows **2 X higher v_{inj}** than Si, even at V_{DS} = 0.5 V
- Consistent V_{inj} depending on channel mobility

Benchmarking: Injection velocity (v_{inj})



- InAs MOSFET shows **2 X higher v_{inj}** than Si, even at V_{DS} = 0.5 V
- Consistent V_{inj} depending on channel mobility

Conclusions

- InAs (rather than $In_xGa_{1-x}As$) enables:
  - Record g_m =1.73 mS/μm at V_{DS} = 0.5 V
  - No significant I_{OFF} penalty (S = 105 mV/dec)
  - 2× V_{inj} improvement vs. s-Si
- First rigorous v_{inj} benchmarking shows InAs MOSFET competitive with best known HEMT

InAs MOSFET (0.5V)	InAs HEMT (0.5V)	Strained Si MOSFET (1V)
2.3×10^7 cm/s	2.8×10^7 cm/s	1×10^7 cm/s