InAs Quantum-Well MOSFET (L_g = 100 nm) with Record High g_m, f_T and f_{max}

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Abstract: This paper reports InAs quantum-well (QW) MOSFETs with record transconductance ($g_{m,max}$ = 1.73 mS/µm) and high-frequency performance (f_T = 245 GHz and f_{max} = 355 GHz) at L_g = 100 nm. This record performance is achieved by using a low D_{it} composite Al_2O_3/InP gate stack, optimized layer design and a high mobility InAs channel. This work is significant because it shows a possible III-V material pathway from $In_{1-x}Ga_xAs$ to InAs with similar processing and generalized characterization, including D_{it}.

Introduction: III-V semiconductors have emerged as a promising channel material for future CMOS low power logic applications [1-2]. Their enhanced electron transport properties offer significant power reduction through aggressive supply power (V_{DD}) scaling. To maximize V_{DD} scaling for logic application, both transconductance ($g_{m,ext}$) and subthreshold slope (S) must be optimized. We report 3 significant advances towards these goals: first an InAs sub channel to improve carrier transport property, second an optimized gate stack process with thin EOT of 2 nm and low D_{it} to improve S, and third an improved layer structure with thin InP barrier (to reduce access resistance) and optimized Si δ-doping (to improve S and reduce R_{SD}).

Experimental: Fig. 1 shows a cross-section of the device structure and **Fig. 2** a corresponding TEM image of L_g = 100 nm device. A thin 2 nm InP barrier was used to reduce access resistance and improve charge control, EOT and immunity to short-channel effects as well as to improve D_{it} [3]. A 10 nm $In_{0.53}Ga_{0.47}As$/InAs/$In_{0.53}Ga_{0.47}As$ composite channel with inverted Si δ-doping was chosen to improve carrier transport and electron confinement in the channel. Inverted Si δ-doping 5 nm below the channel inside the InAlAs buffer was used to supply carriers to the S/D access region and reduce R_{SD} without adding to the barrier thickness and EOT. It is critical to carefully select the inverted Si δ-doping density to achieve the best trade-off of threshold voltage (V_T), subthreshold slope (S) and parasitic resistance (R_{SD}).

Fig. 3 shows channel carrier density as a function of gate potential for various Si δ-doping densities. The ability to modulate the channel charge degrades as Si δ-doping increases, indicating that Si δ-doping needs to be carefully optimized for acceptable subthreshold characteristics [4]. In this work, we selected δ-doping = $1\times10^{12}/cm^2$, which resulted in both low R_{SD} (enabling record high g_m) and excellent electrostatic control (enabling good S). **Fig. 4** shows the corresponding conduction band profile with Si δ-doping = $1 \times 10^{12}/cm^2$ at V_{GS} = 0 V. In a calibration sample, we measured $\mu_{e,Hall}$ = 11,200 cm^2/V-sec and $n_{s,ch}$ = $9 \times 10^{11}/cm^2$ at 300 K.

Device fabrication was similar to that of a conventional HEMT [4], with the addition of gate oxide deposition prior to metal gate formation (3 nm of Al_2O_3 for an EOT = 2 nm). Additionally, MOS capacitors were fabricated with a thicker 10 nm Al_2O_3/InGaAs to enable accurate interfacial state density (D_{it}) extraction.

Results and Discussion: Fig. 5 shows MOSCAP C-V characteristics from 1 kHz to 1 MHz with low frequency dispersion in both accumulation and depletion. Analysis of the interfacial state density (D_{it}) was performed using the SEMATECH generalized technique [5] that combines High-Low frequency and Terman D_{it} extraction methods. This technique is a significant improvement on previous methods as it allows D_{it}, trap energy (E_T) and oxide capacitance (C_{ox}) to be determined simultaneously. **Fig. 6** shows excellent agreement between model and measured data, confirming the accuracy of the D_{it} result. Fitting the model simultaneously to the high frequency C-V (25 ˚C) and low frequency C-V (100 ˚C in order to accelerate trap response) curves produces the D_{it} vs. E_T dependence (Fig. 6, inset). D_{it} is lower in the upper portion of the band gap (minimum D_{it} = 4×10^{12} /eV.cm^2), which is preferable for NMOS device operation.

Fig. 7 shows the device output characteristics, demonstrating excellent pinch off and low R_{SD} (323 Ohm-µm). **Fig. 8** shows typical subthreshold characteristics with excellent subthreshold behavior and I_{ON}/I_{OFF} ratio ~ 2×10^3 down to L_g = 100 nm. The gate leakage (I_g) is lower than 0.1 nA/µm at all measured bias conditions. InAs QW device with L_g = 100 nm exhibits V_T = +0.2 V (defined at I_D = 1µA/µm) and S = 105 mV/dec at V_{DS} = 0.5 V. This results in an I_{OFF} = 5×10^{-8} A/µm at V_{GS} = 0 V and V_{DS} = 0.5 V. The attainment of this I_{OFF} value in a device with low resistance parasitics and excellent subthreshold slope is significant because this is the first time that these three features are shown in combination in a III-V MOSFET. **Fig. 9** shows good immunity to short-channel effects with controlled V_T roll-off at V_{DS} = 50 mV and V_{DS} = 0.5 V. **Fig. 10** shows typical transconductance characteristics at V_{DS} = 0.5 V. The InAs QW MOSFET exhibits $g_{m,max}$ > 1.73 mS/µm at V_{DS} = 0.5 V. This is a record transconductance for a III-V MOSFET of this gate length and V_T and it is the result of both the optimized Si δ-doping density that contributes to reduced access resistance and the high electron mobility associated with the InAs subchannel.

Microwave performance was characterized from 0.5 GHz to 50 GHz. **Fig. 11** plots h_{21}, U_g and stability-factor (k) against frequency. We obtained a current-gain cut-off frequency f_T = 245 GHz and a maximum oscillation frequency f_{max} = 355 GHz. These are record values for any III-V MOSFET. The device also exhibits f_T = 238 GHz at V_{DS} = 0.5 V. Small-signal parameter extraction from measured S-parameters gave good consistency between DC and RF transconductance.

We benchmarked our devices with other state-of-the-art III-V MOSFETs (including surface, buried-channel and non-planar devices) using the figure of merit Q = g_m/S [6], as shown in **Fig. 12** [7-11]. Our devices exhibit excellent transconductance and subthreshold slope with Q ~ 16, which can only be achieved with optimized layer structure, ohmic contacts (low R_{SD}) and low D_{it} / EOT gate-stack.

Conclusions: We have demonstrated quantum-well InAs MOSFETs with outstanding logic characteristics (S = 105 mV/dec, V_T = 0.2 V, I_{OFF} = 5×10^{-8} A/µm and $g_{m,max}$ > 1.73 mS/µm at V_{DS} = 0.5 V). In addition, our devices show record f_T = 245 GHz and f_{max} = 355 GHz. These results emerge from an optimized layer structure (with thin InP barrier and inverted Si δ-doping), high quality Al_2O_3/InP gate stack, and high mobility InAs channel.

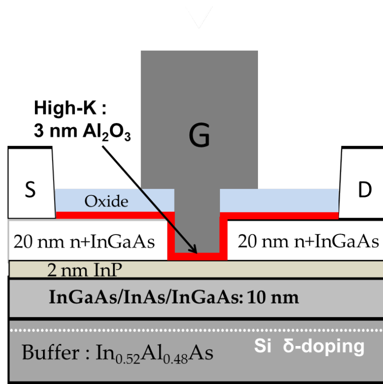

Fig. 1: Cross-sectional schematic of QW device with 3 nm ALD Al_2O_3, 2 nm InP barrier and InAs composite channel.

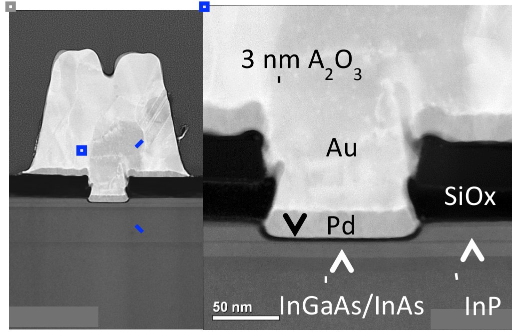

Fig. 2: TEM cross-section of fabricated device. Note well optimized recess with minimal L_{side}

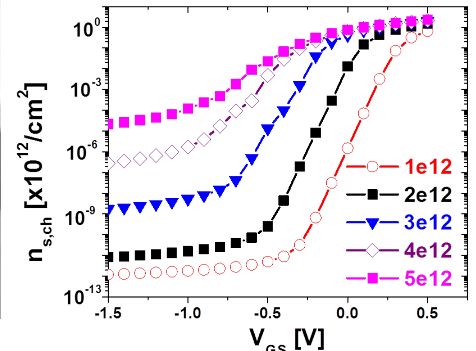

Fig. 3: 1d Poisson-Schrödinger simulations of channel electron density as a function of gate bias. High δ -doping density limits charge modulation.

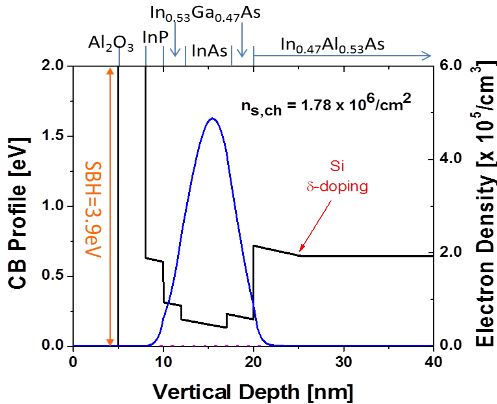

Fig. 4: 1d Poisson-Schrödinger simulation of conduction band profile and electron wave-function for the optimized Si δ -doping condition.

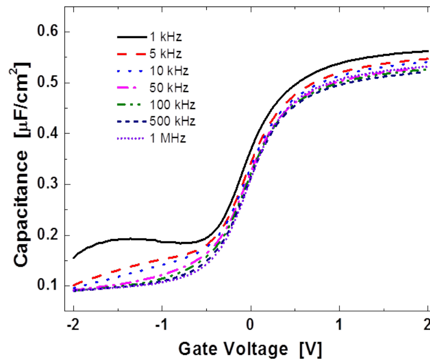

Fig. 5: Room temperature CV characteristics of partner $In_{0.53}Ga_{0.47}As$ MOSCAP with 10 nm ALD Al_2O_3 (reduced leakage for accurate CV measurement)

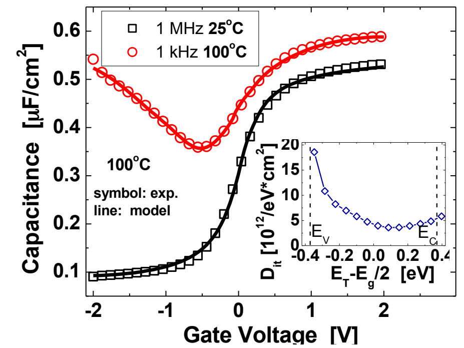

Fig. 6: Measured and simulated CV curves with inset of D_{it} extracted using the generalized technique as a function of energy. Note mid-gap D_{it} of ~4x10^{12} eVcm^2

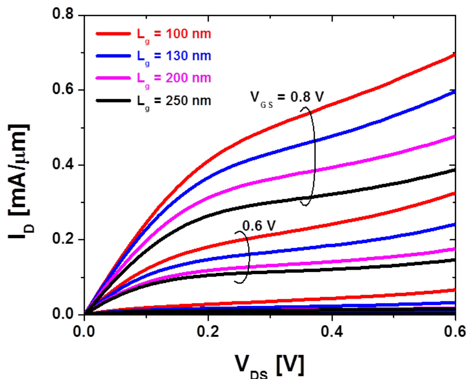

Fig. 7: I_dV_d output characteristics showing excellent charge control and low series resistance (323 Ω-μm).

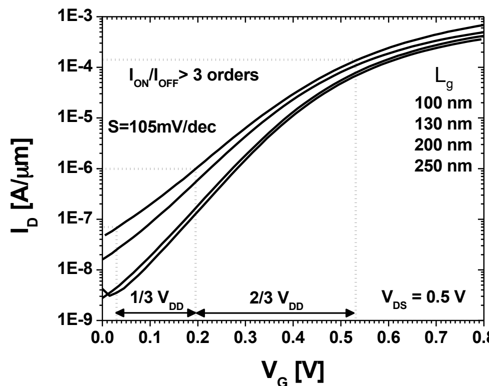

Fig. 8: Semi-log scale I_dV_g L_g = 100 nm device has SS of 105 and I_{on}/I_{off} >1000.

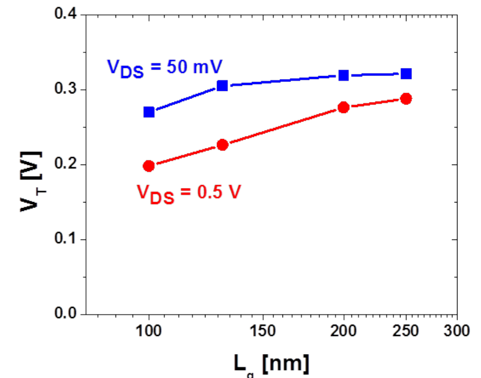

Fig. 9: V_T vs L_g. Devices display reasonable immunity to V_T roll-off given EOT of 2 nm and buried channel design

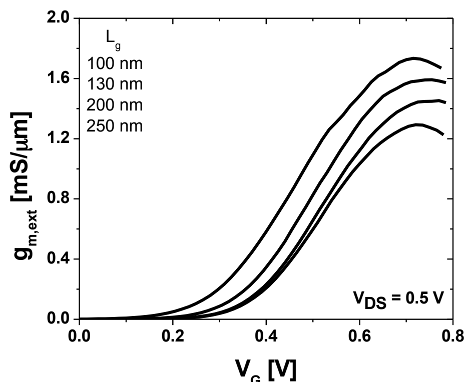

Fig. 10 $g_{m,ext}V_G$. L_g = 100 nm device has $g_{m,max}$ = 1.73 mS/μm

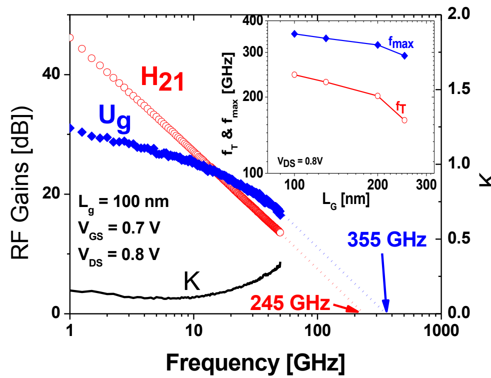

Fig. 11 Microwave characteristics of L_g = 100 nm InAs MOSFET with the highest f_T = 245 GHz and f_{max} = 355 GHz of any III-V MOSFET

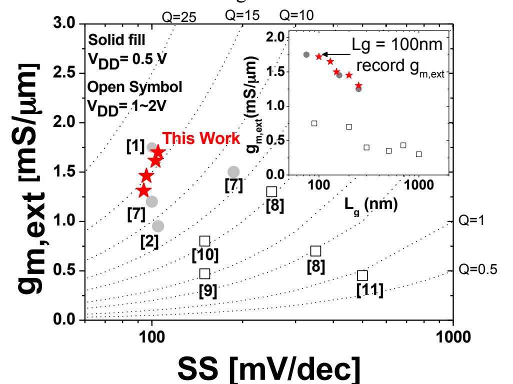

Fig. 12 $g_{m,ext}$ versus S or quality factor. This work has state of the art performance with record $g_{m,ext}$ for a given gate length.

Reference:[1] R. Chau *et al.*, IEEE T-Nano., p. 153 (2005). [2] Y. Sun *et al.*, IEDM, p. 367 (2008). [3] M. Radosavljevic *et al.*, IEDM, p.319 (2009) [4] T.-W. Kim *et al.*, IEDM, p. 483 (2009). [5] M. Madan *et al.*, DRC, p. 117 (2011). [6] G. Doornbos *et al.*, EDL, p. 1110 (2010). [7] M. Egard *et al.*, IEDM, p. 303 (2011). [8] Y. We *et al.*, IEDM, p. 331 (2009). [9]R. Hill *et al.*, IEDM, p. 130 (2010). [10]C. Thelander *et al.*, EDL, p. 206 (2008). [11] U. Singisett *et al.*, EDL, p. 1128 (2009).