InAs HEMTs:
the path to THz electronics?

J. A. del Alamo

Microsystems Technology Laboratories, MIT

Short Course on: **High-Performance narrow-bandgap HEMT technology for advanced microwave front-ends: Towards the end of the roadmap?**

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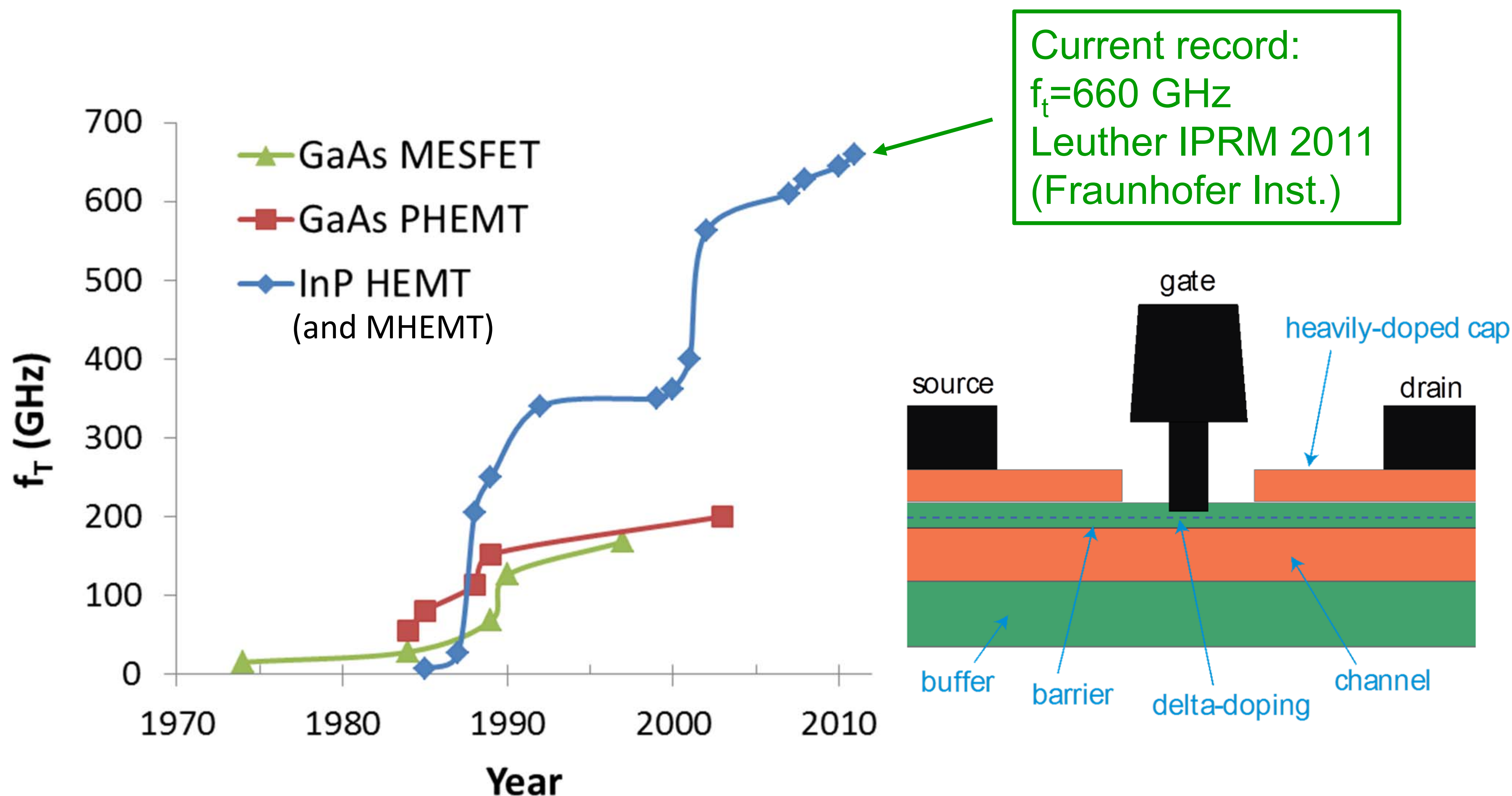
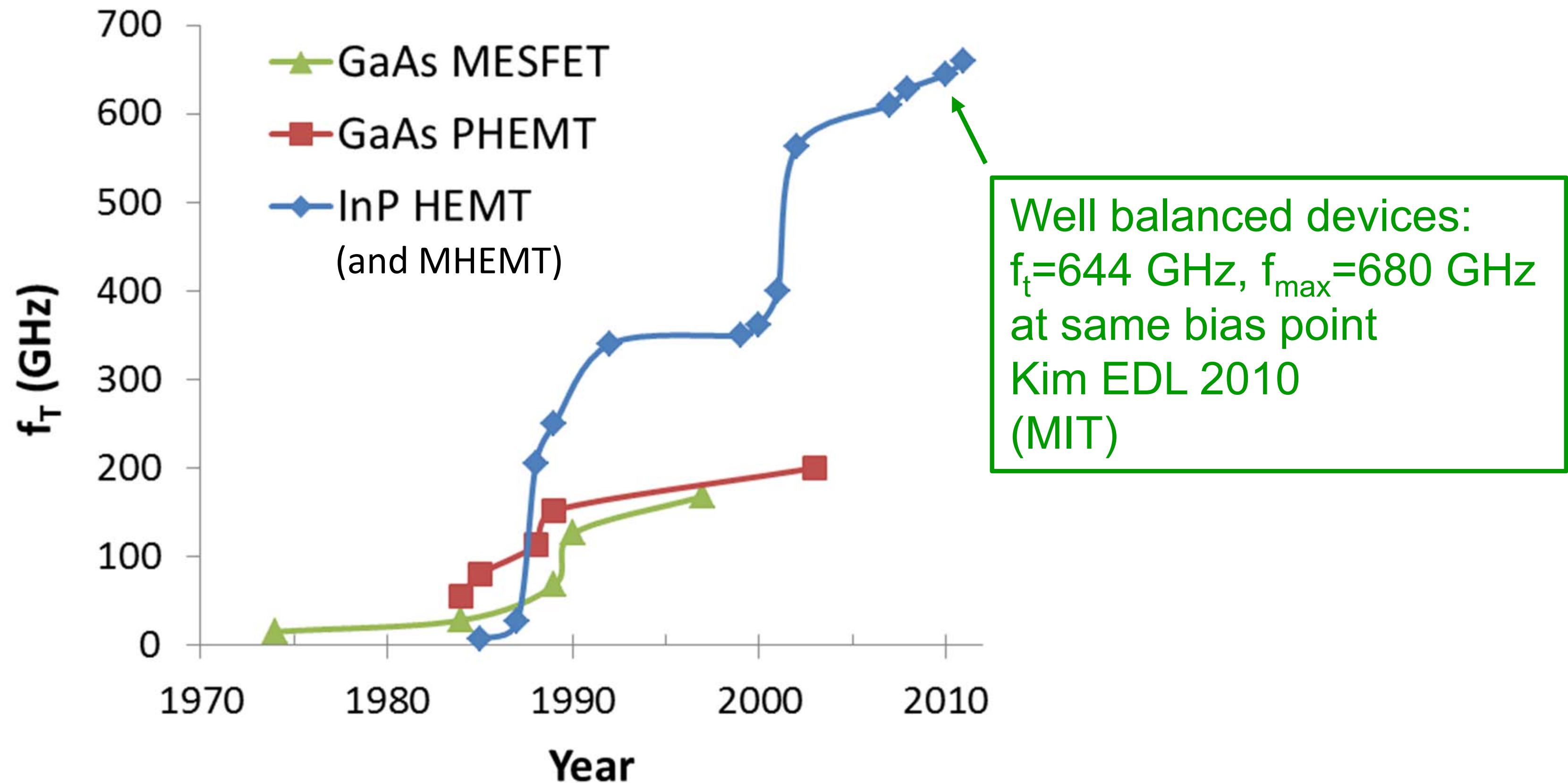
III-V HEMT: record f_T vs. time



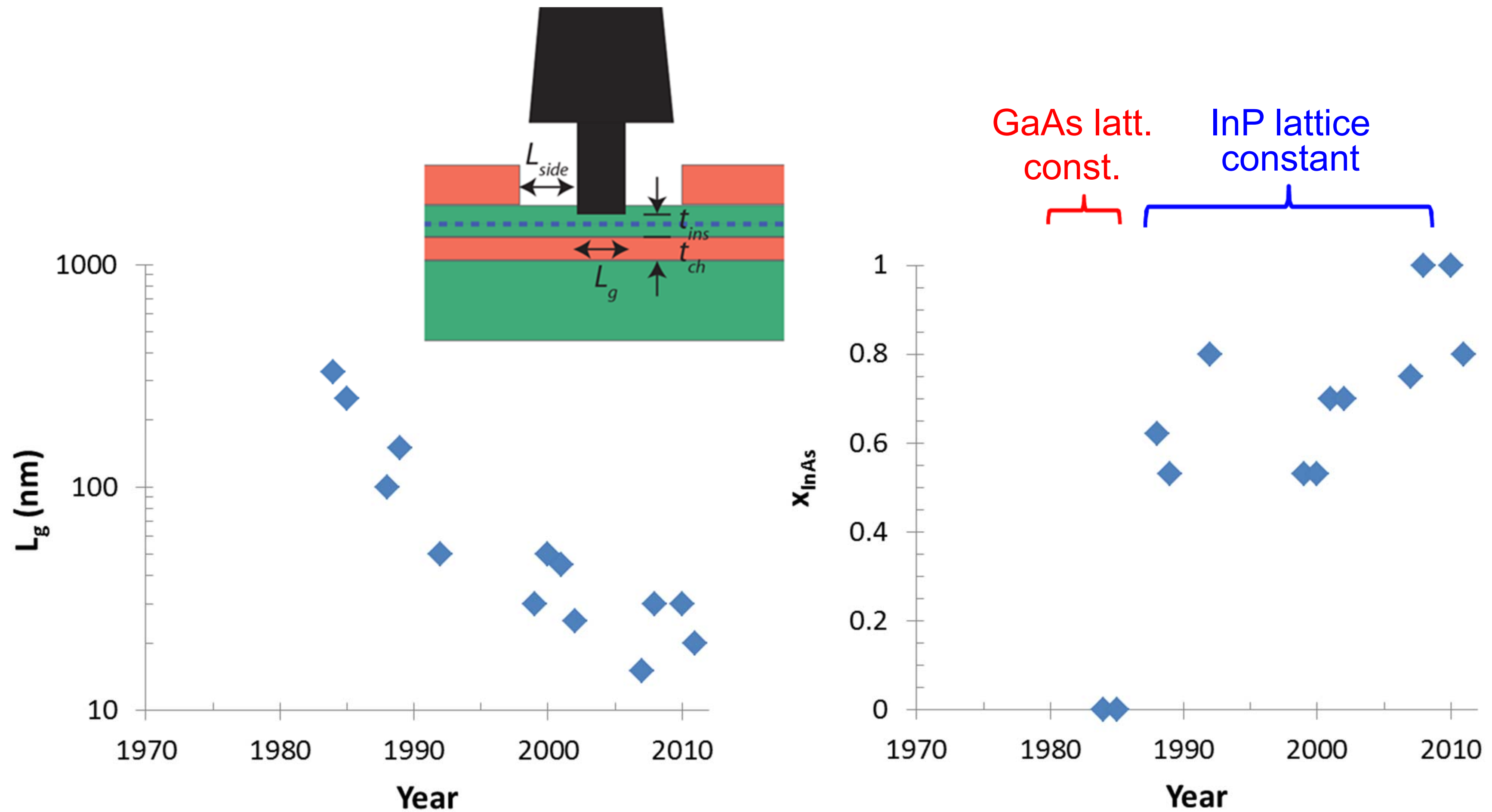
For >20 years, record f_T obtained on InGaAs-channel HEMTs

III-V HEMT: record f_T vs. time



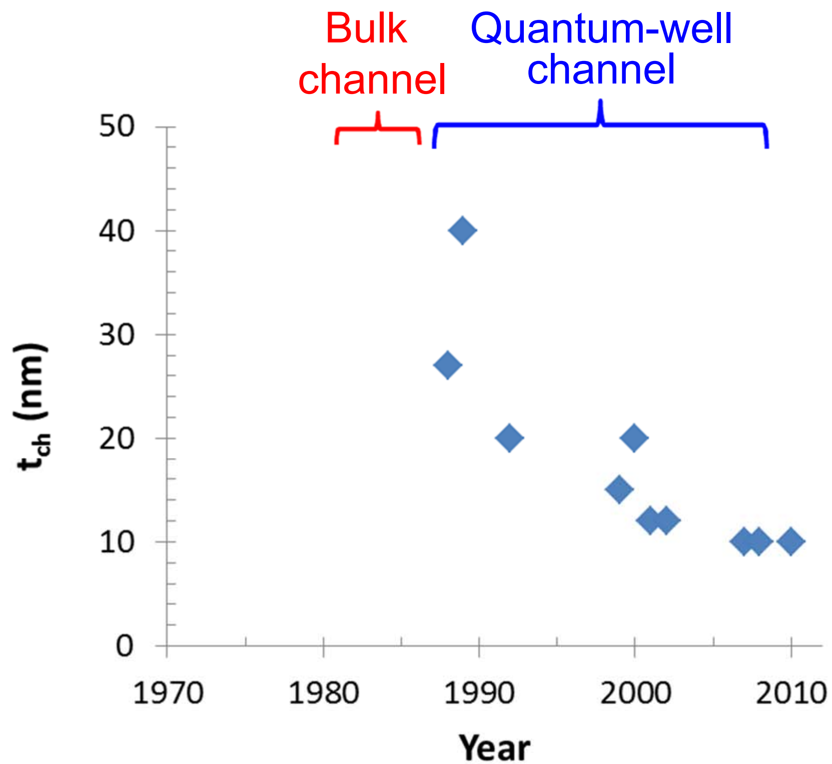
InGaAs-channel HEMTs offer record balanced f_T and f_{max}

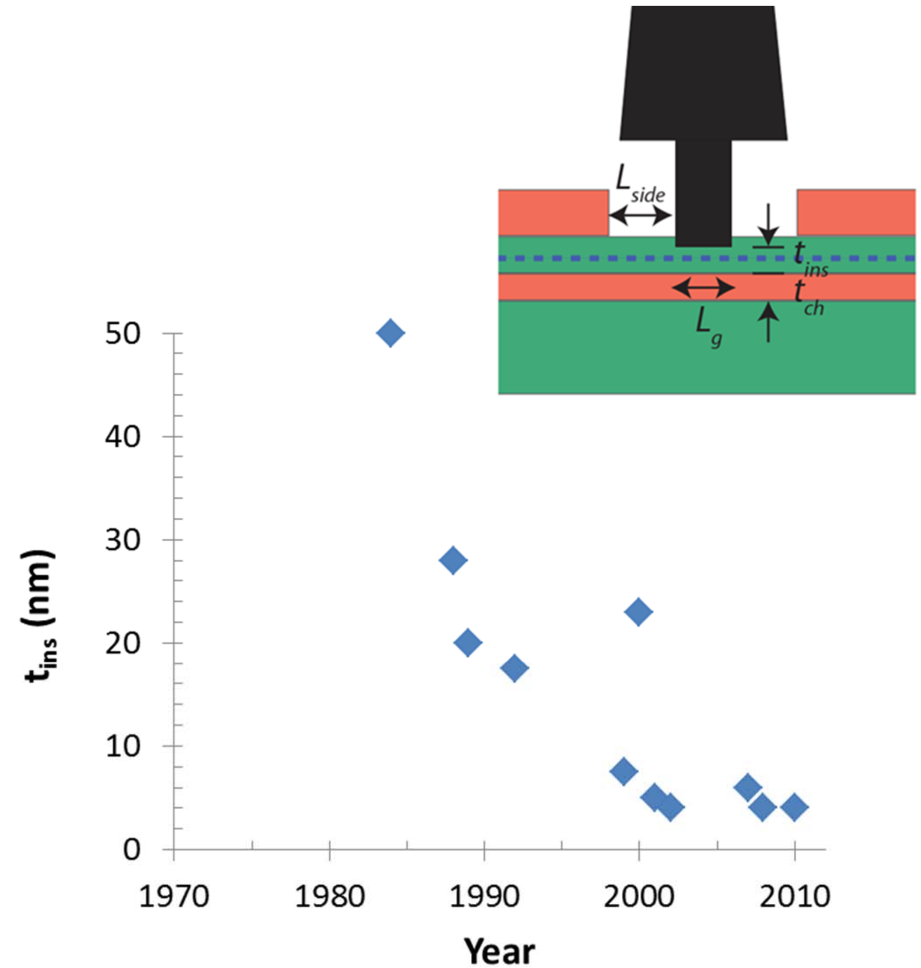
Record f_T III-V HEMTs: megatrends



Over time: L_g↓, $In_xGa_{1-x}As$ channel x_{InAs}↑

Record f_T III-V HEMTs: megatrends





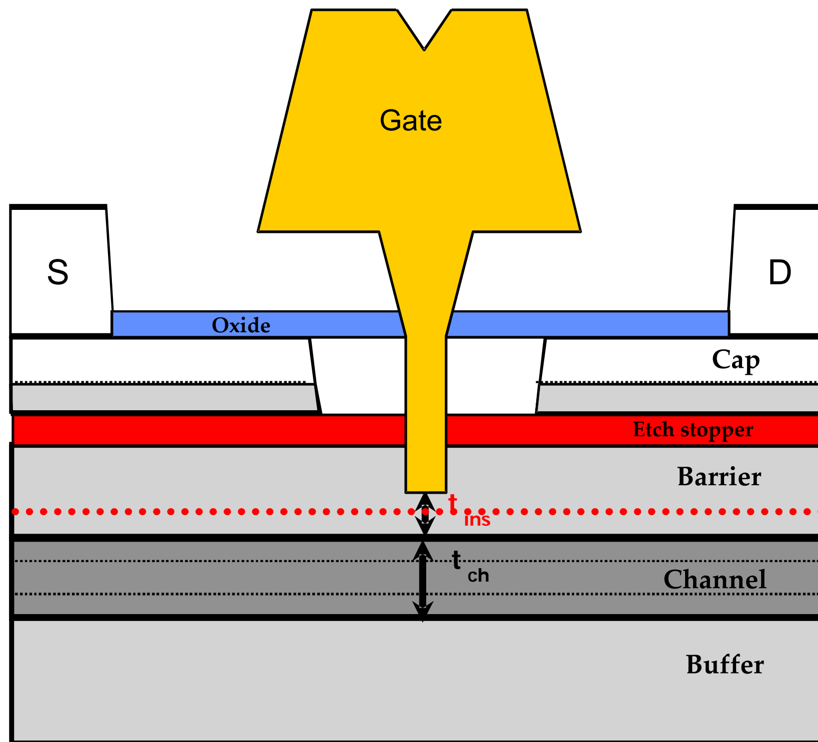
Over time: $t_{ch}\downarrow$, $t_{ins}\downarrow$

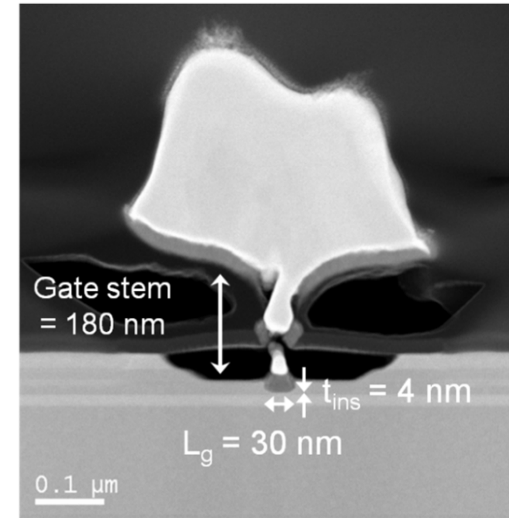
Outline

1. Example of high-frequency InAs HEMT
2. f_T measurements
3. f_T analysis
4. How to improve f_T
5. Limits to HEMT scaling and future prospects

1. Example of high-frequency InAs HEMT

L_g=30 nm InAs HEMT

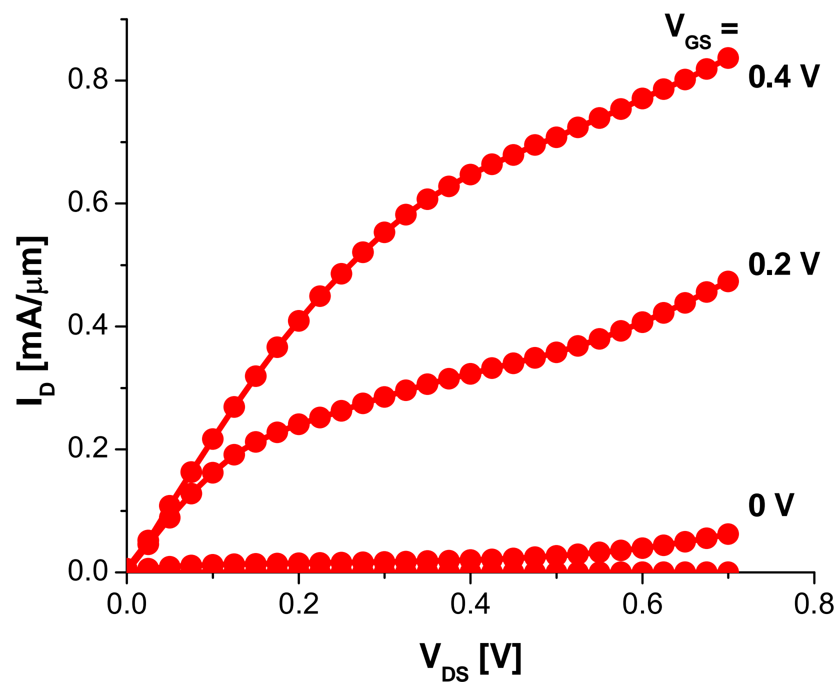


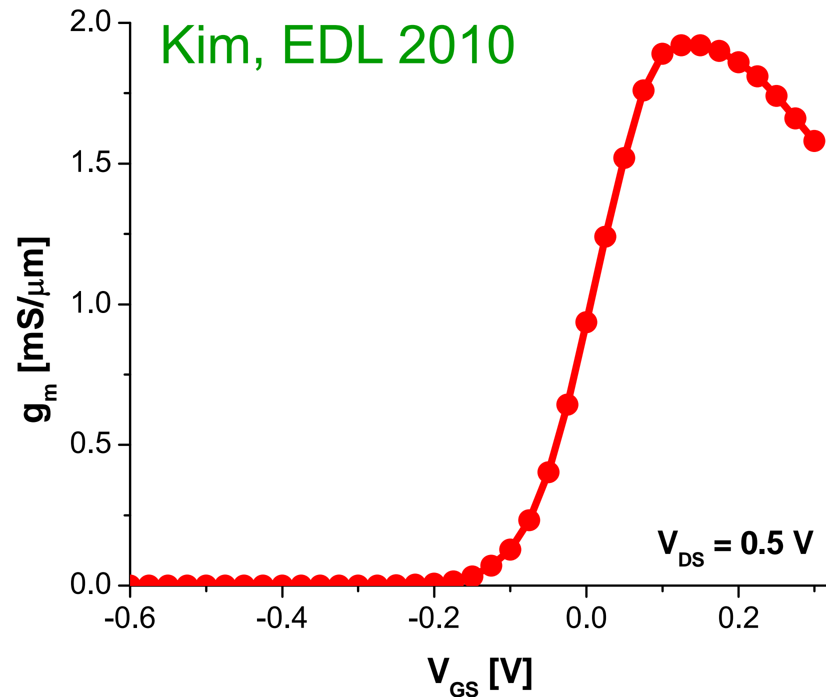


- QW channel (t_{ch} = 10 nm):
  - InAs core (t_{InAs} = 5 nm)
  - InGaAs cladding
- $\mu_{n,Hall}$ = 13,200 cm^2/V-sec
- InAlAs barrier (t_{ins} = 4 nm)
- Ti/Pt/Au Schottky gate
- L_g=30 nm
- L_{side}=150 nm

Kim, EDL 2010

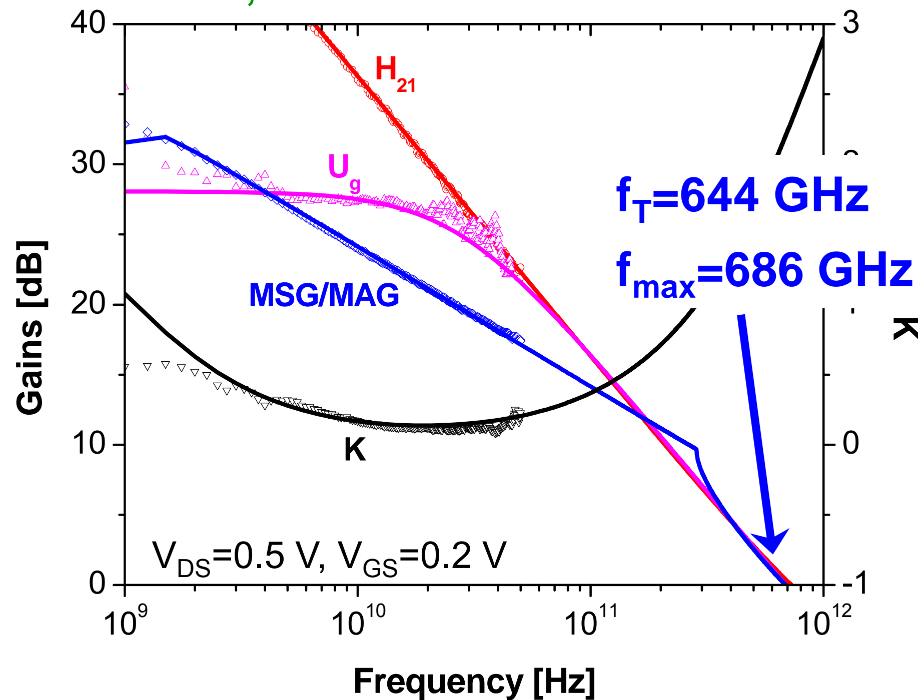
L_g=30 nm InAs HEMT

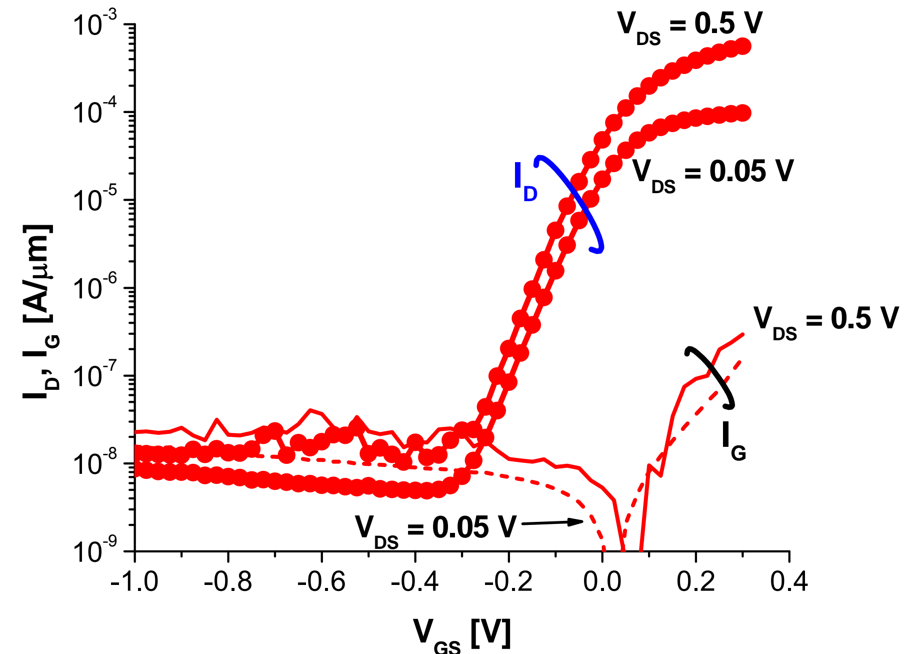




- Large current drive: I_{ON}>0.5 mA/μm at V_{DD}=0.5 V
- V_T = -0.15 V, R_S=190 Ohm.μm
- High transconductance: g_{mpk}= 1.9 mS/μm at V_{DD}=0.5 V

L_g=30 nm InAs HEMT





- Only transistor of any kind with both f_T and f_{max} > 640 GHz at same bias point
- Subthreshold characteristics:
  - S = 74 mV/dec, DIBL = 80 mV/V, I_{on}/I_{off} ~ $5x10^3$

2. f_T measurements

- Extraordinary claims demand extraordinary evidence!

- Verification of f_T and f_{max} measurements:
  1. Gummel technique
  2. Small-signal equivalent circuit model
  3. Measurements on multiple devices
  4. Measurements on multiple test benches

Gummel technique for f_T extraction

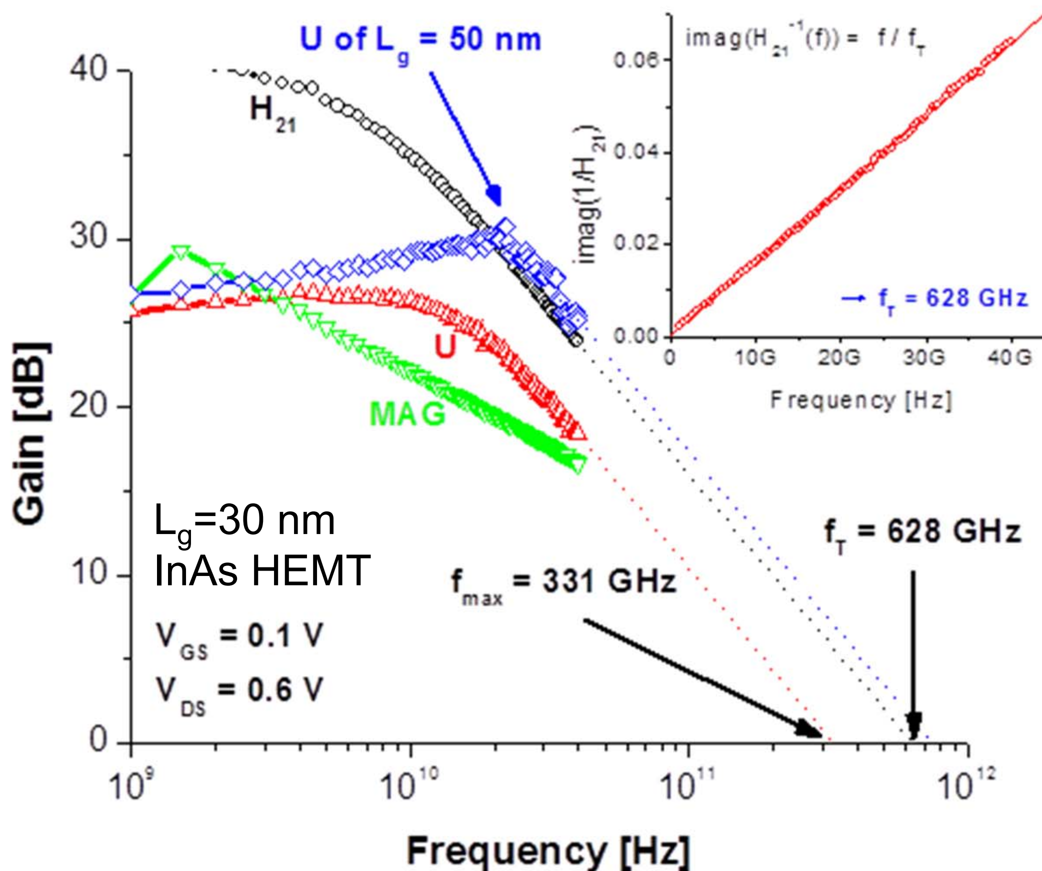
In one-pole system:

$$h_{21}(f) = \frac{h_{21}(DC)}{1 + jf\frac{h_{21}(DC)}{f_T}}$$

Then:

$$Im[\frac{1}{h_{21}(f)}] = \frac{f}{f_T}$$

Slope gives f_T



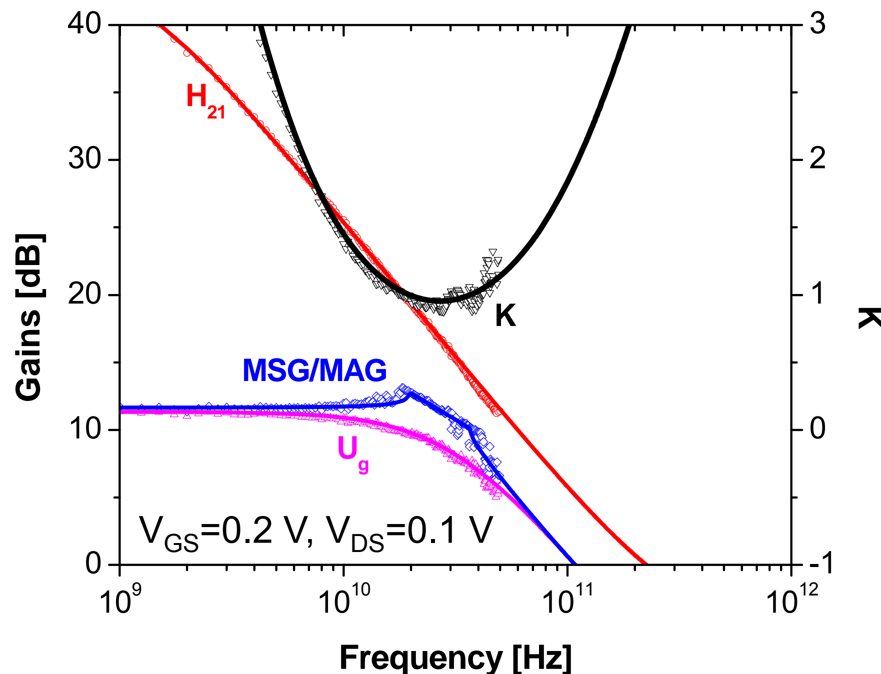
Kim, EDL 2008

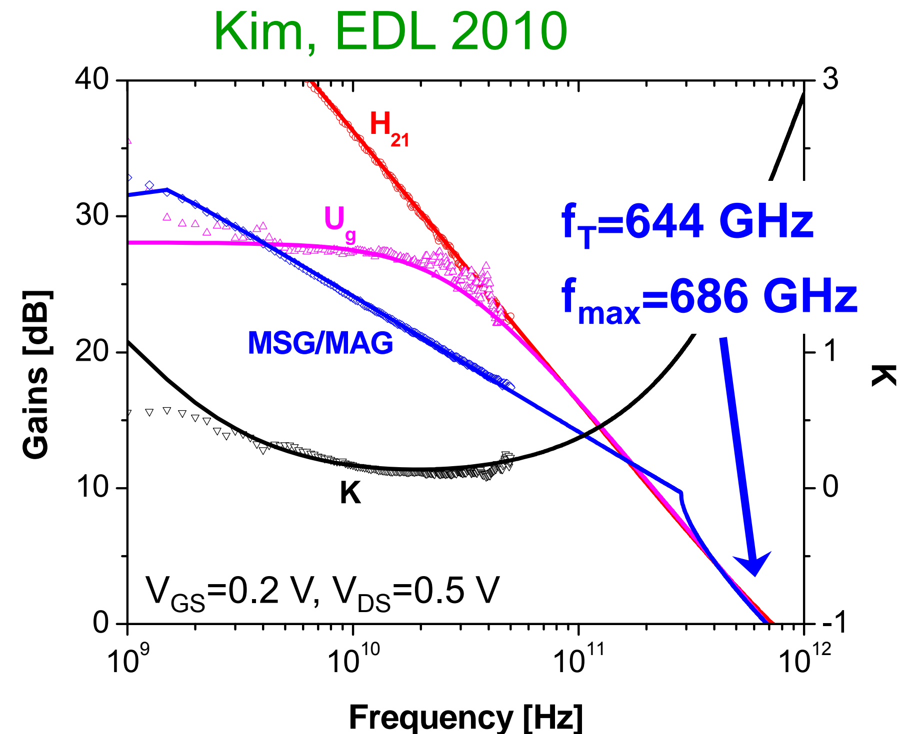
Gummel, Proc IEEE 1969

f_T extraction from equivalent-circuit model

Small-signal equivalent circuit model in linear and saturation regimes at V_{GS} of peak f_T:

Kim, EDL 2010





Extrapolation from small-signal model yields:

→ f_T=648 GHz

→ f_{max}=686 GHz

Also model S parameters (see below)

Measurements on multiple devices and systems

Measurements of one device in three different test benches:

		8510C @MIT	8510C @TSC	PNA @UCSB	Avg.	STD
f_T [GHz]	From H_{21}	645	645	643	644.3	0.9
	From Gummel's approach	644	644	645	644.3	0.5
f_{max} [GHz]		681	686	677	681.3	3.7

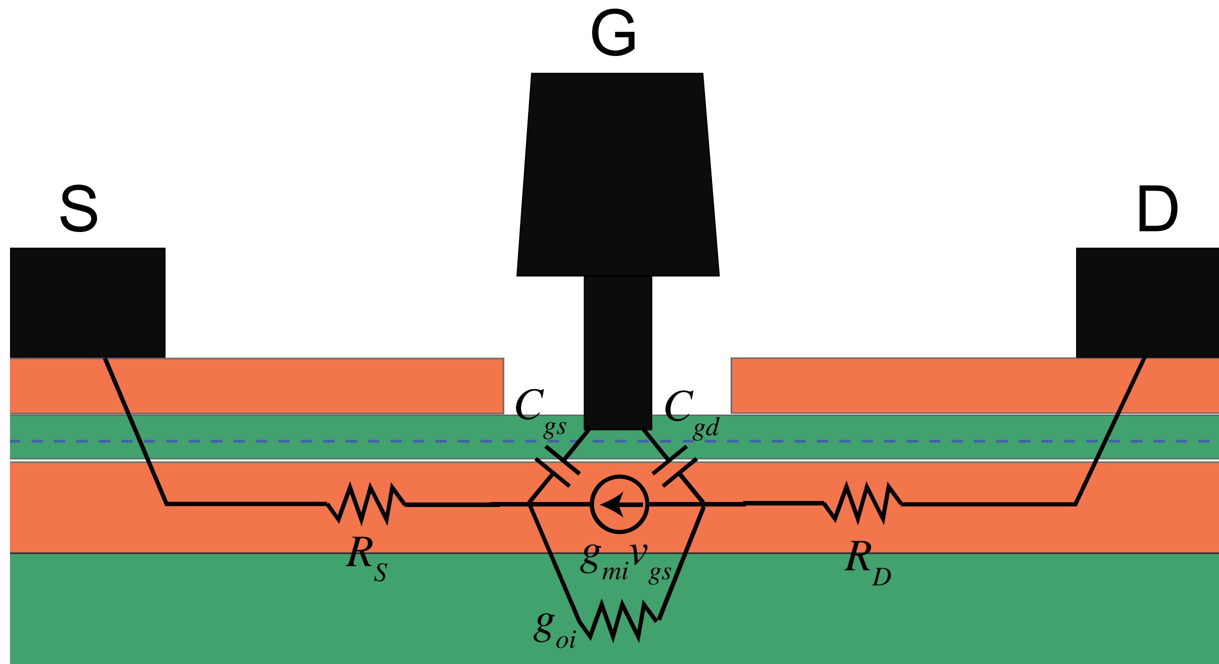
Kim, EDL 2010

Measurement of three devices on one test bench:

→ f_T=645, 644, 644 GHz.

All measurements at same bias point: V_{GS}=0.2 V, V_{DS}=0.5 V

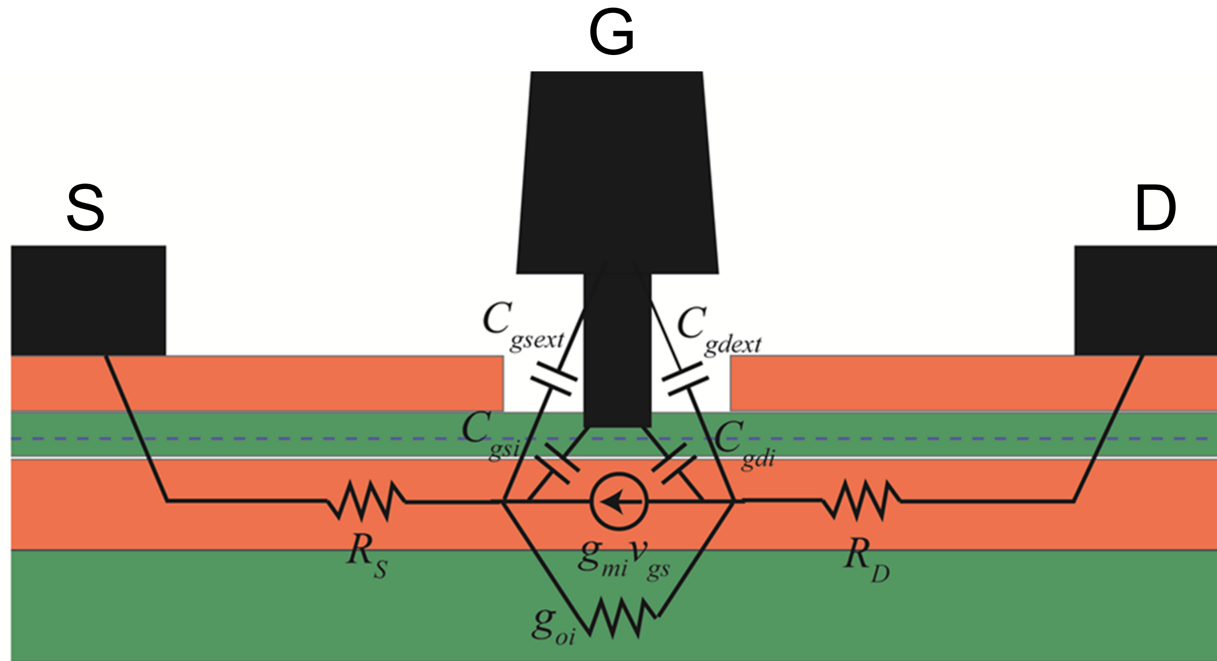
3. f_t analysis



- First-order f_T expression for HEMT:

$$f_T = \frac{1}{2\pi} \frac{g_{mi}}{C_{gs} + C_{gd} + g_{mi}(R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]}$$

Break out parasitic capacitances



- Capacitance components:

$$C_{gs} = C_{gsi} + C_{gsext} \qquad C_{gd} = C_{gdi} + C_{gdext}$$

Delay time analysis

- Delay time:

$$\tau = \frac{1}{2\pi f_T} = \tau_t + \tau_{ext} + \tau_{par}$$

- Components of delay time:

$$\tau_t = \frac{C_{gsi} + C_{gdi}}{g_{mi}} = \frac{L_g}{v_e}$$

Intrinsic delay (transit time)

Extrinsic delay

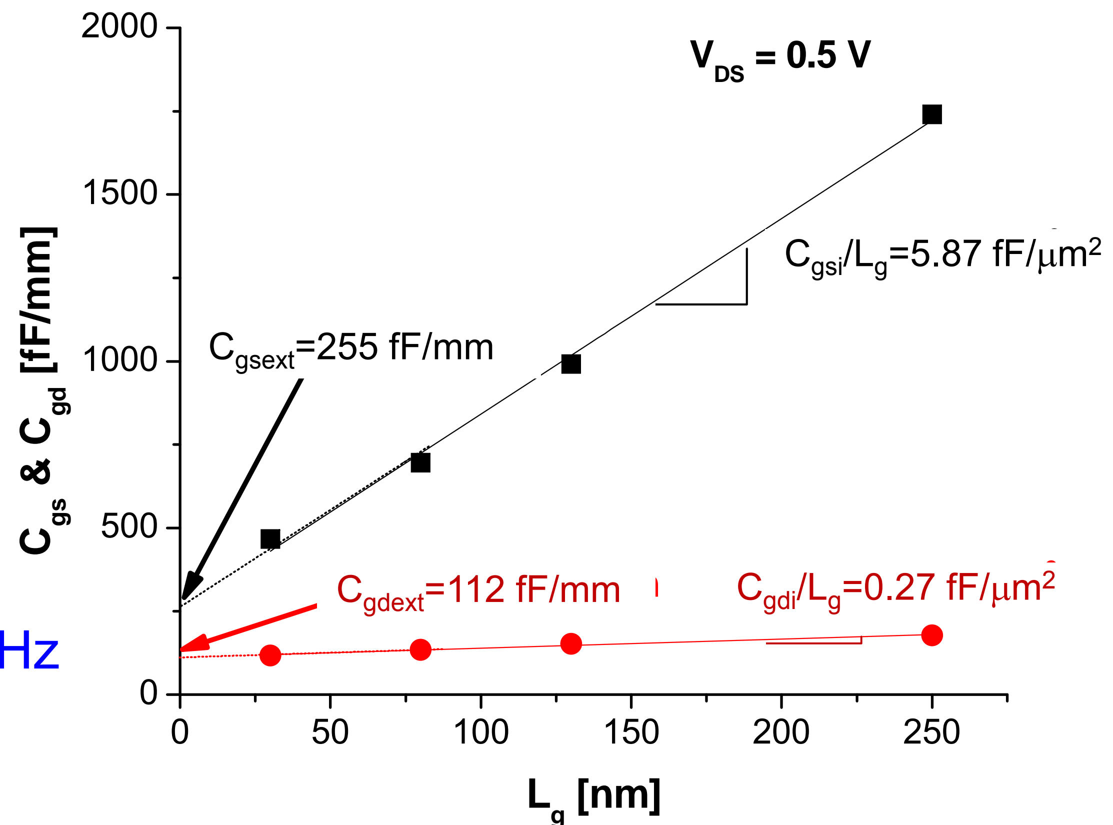
$$\tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}}$$

Parasitic delay

$$\tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]$$

Extraction of parasitic capacitances

- Need devices with different L_g
- Bias them at same V_{GS} overdrive around peak f_T point
- Extract small-signal equivalent circuit models
- Study L_g scaling behavior of C_{gs} and C_{gd}



InAs HEMTs

(f_t=601 GHz, f_{max}=609 GHz at L_g=30 nm)

Kim, IEDM 2008

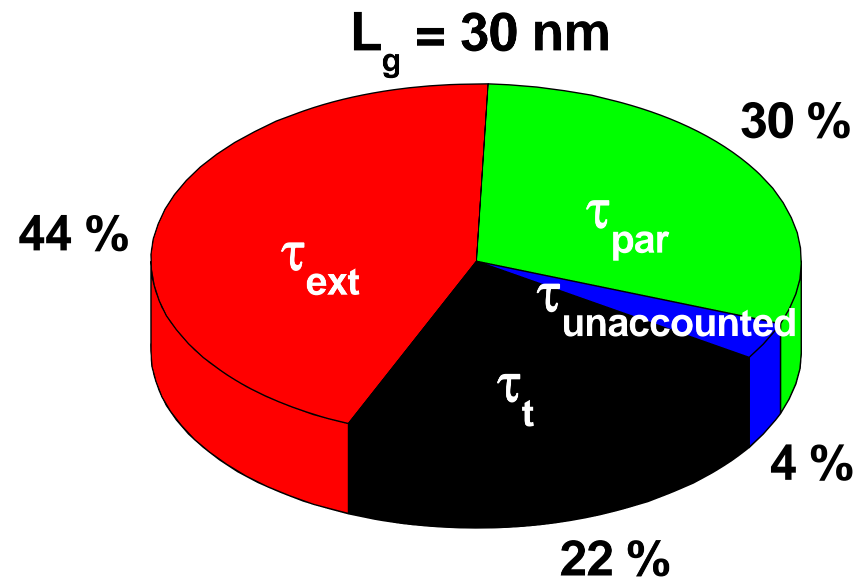
Delay components of L_g=30 nm InAs HEMT

Delay time from f_t: ~265 fs

- Intrinsic delay: ~59 fs
- Extrinsic delay: ~117 fs
- Parasitic delay: ~80 fs
- Unaccounted: ~9 fs

least significant, yields v_e=5.1x10^7 cm/s

most significant

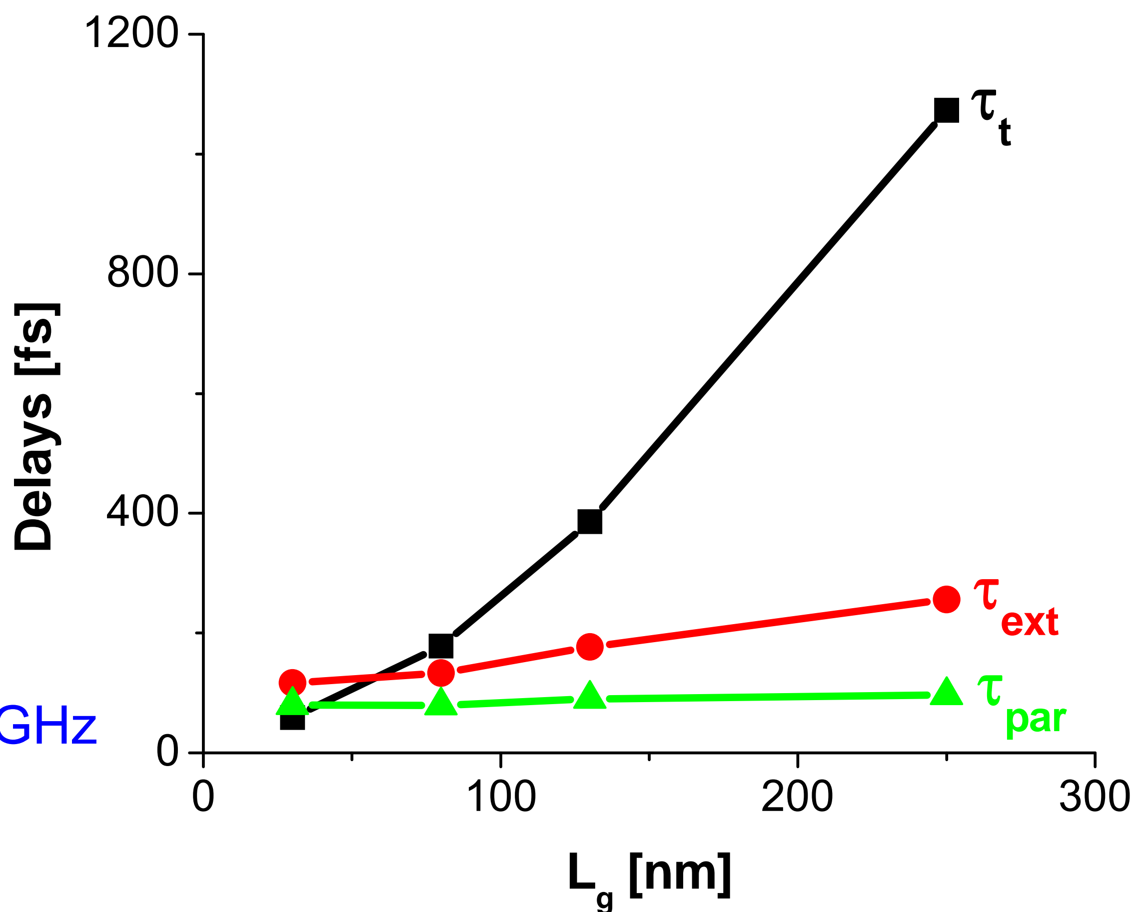


InAs HEMTs

(f_t=601 GHz, f_{max}=609 GHz at L_g=30 nm)

Kim, IEDM 2008

Scaling of delay components



InAs HEMTs

(f_t=601 GHz, f_{max}=609 GHz at L_g=30 nm)

Kim, IEDM 2008

τ_{ext} and τ_{par} do not scale, become dominant for L_g< 60 nm

4. How to improve f_T

- Intrinsic delay:

$$\tau_t = \frac{C_{gsi} + C_{gdi}}{g_{mi}} = \frac{L_g}{v_e}$$

→ L_g ↓ (without degrading g_{mi})
→ v_e ↑ → channel engineering

- Extrinsic delay:

$$\tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}}$$

→ C_{gsext}, C_{gdext} ↓ → gate engineering
→ g_{mi} ↑ → harmonious scaling

How to improve f_T

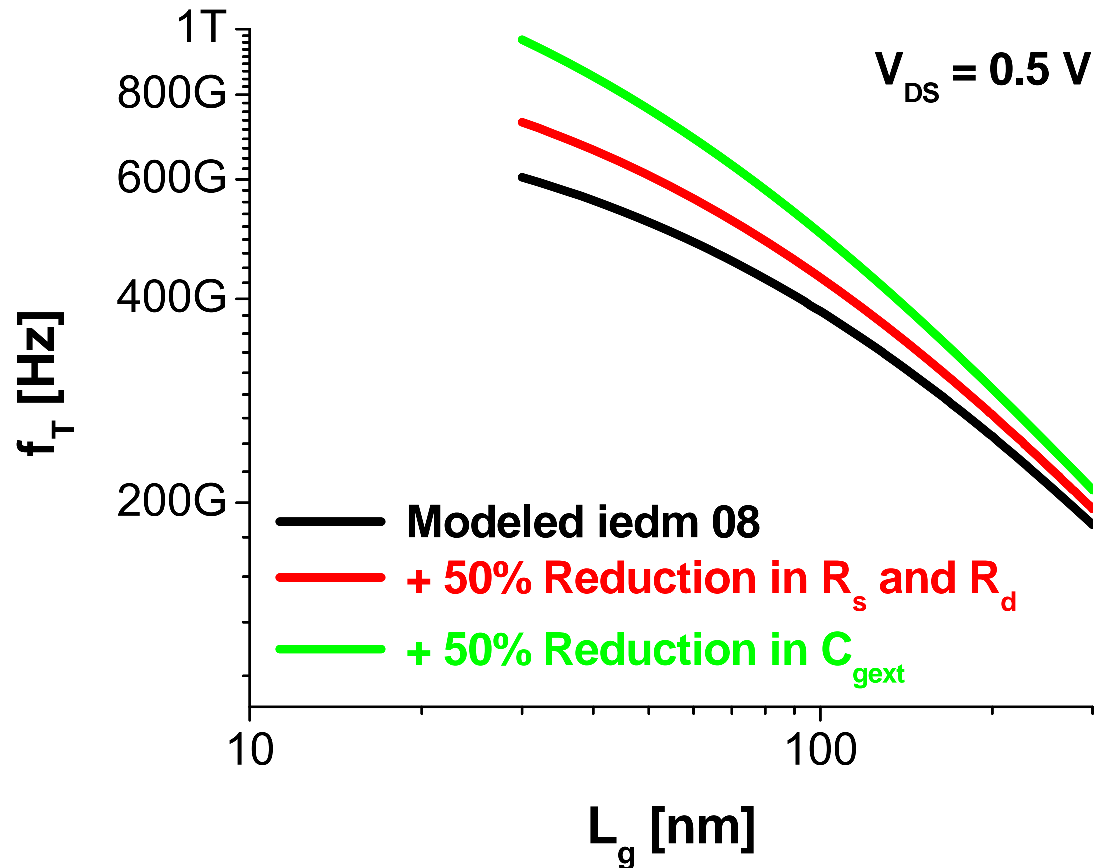
- Parasitic delay:

$$\tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]$$

→ $R_S + R_D$ ↓

→ increase electrostatic integrity: g_{oi}/g_{mi} ↓

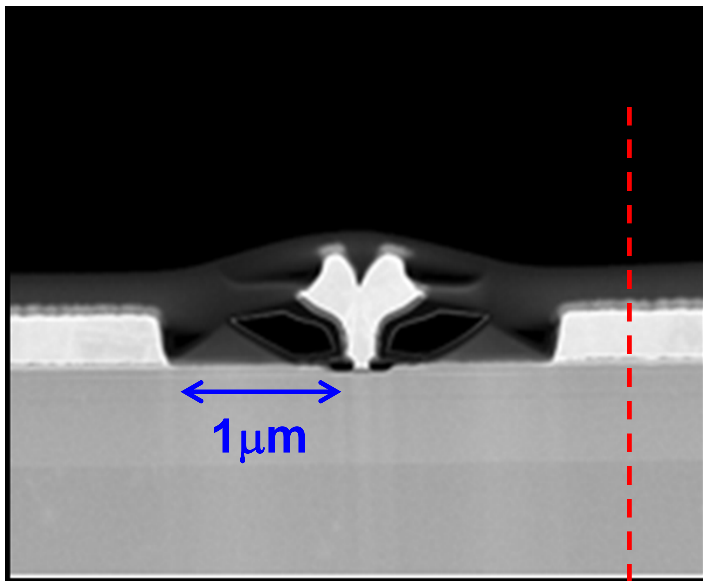
How far can we expect to go?



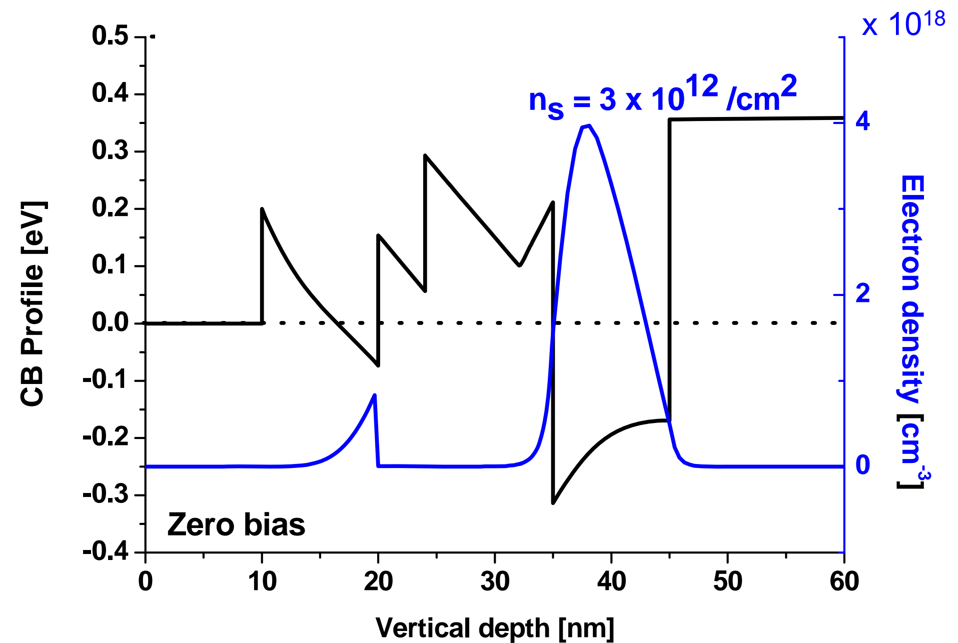
f_t=1 THz feasible even at L_g=30 nm

a) $R_S + R_D \downarrow$

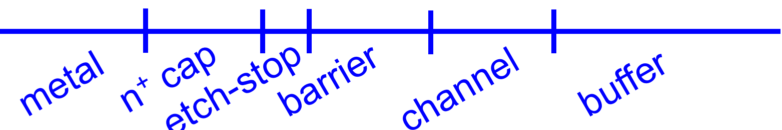
- In typical HEMTs:
  - large G-S, G-D gaps
  - barrier in extrinsic region
  - limited electron concentration in extrinsic channel



R_S ~ 200 Ohm.μm



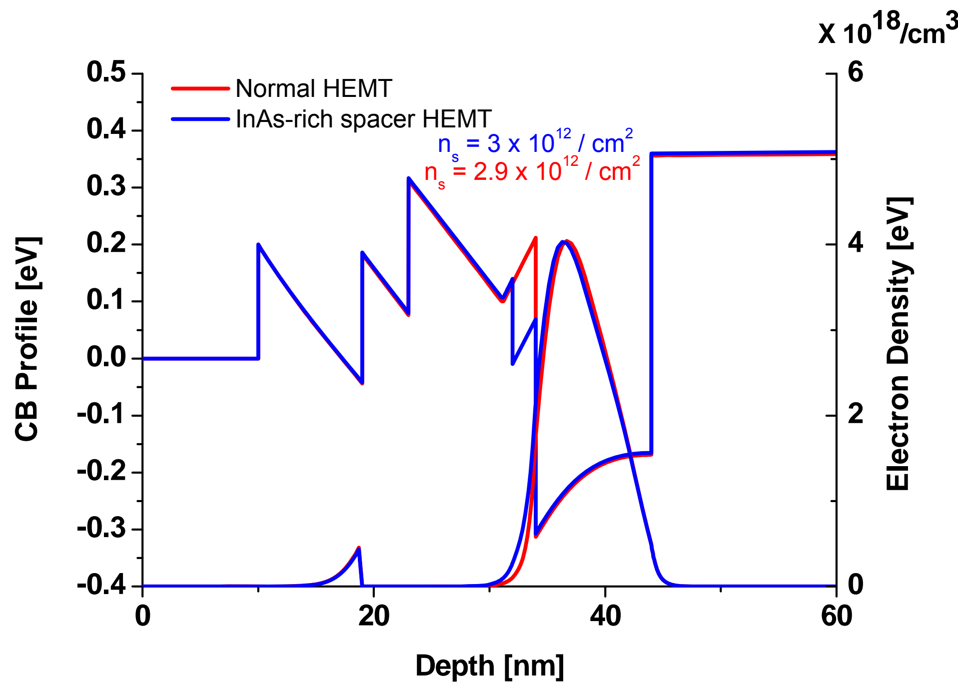
E_C and n in cross section

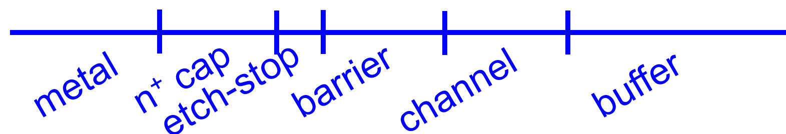


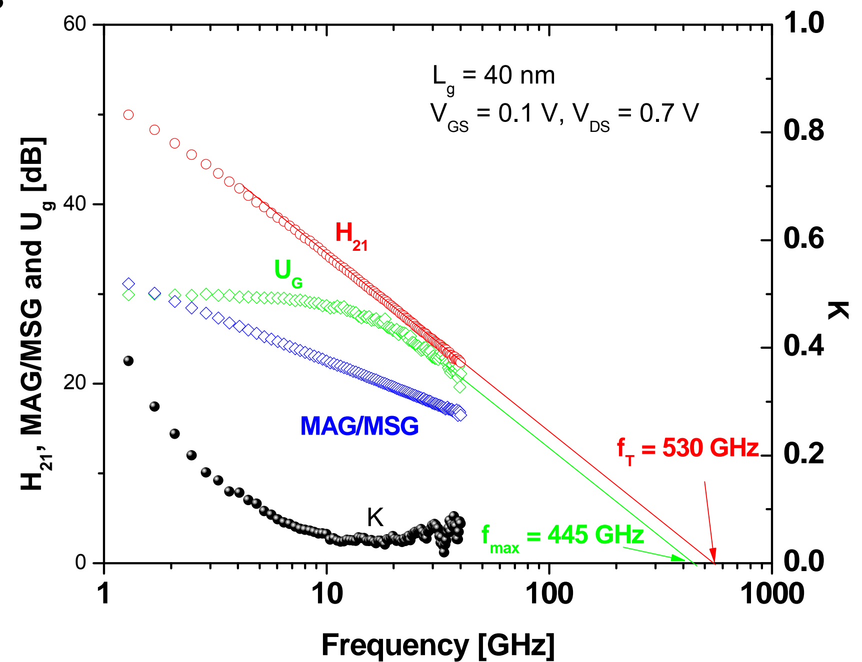
Kim, IEDM 2010

Approaches to reducing barrier and $n_{s,ext}$ ↑

- InAs-rich InAlAs sub-barrier:







L_g=40 nm $In_{0.7}Ga_{0.3}As$ HEMT:

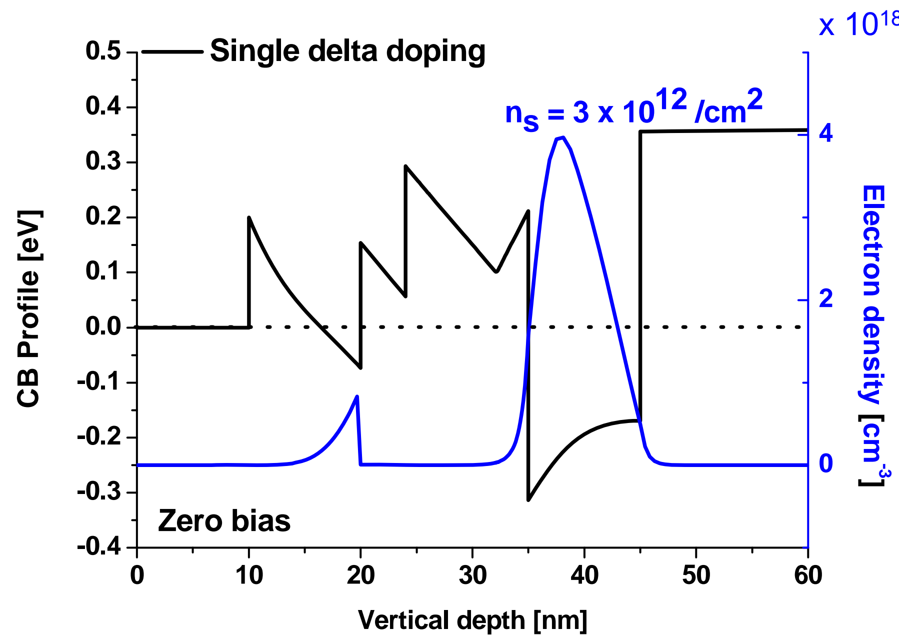
R_s ~ 170 Ohm.µm

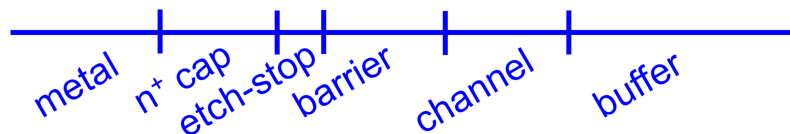
f_T=530 GHz at V_{DS}=0.7 V

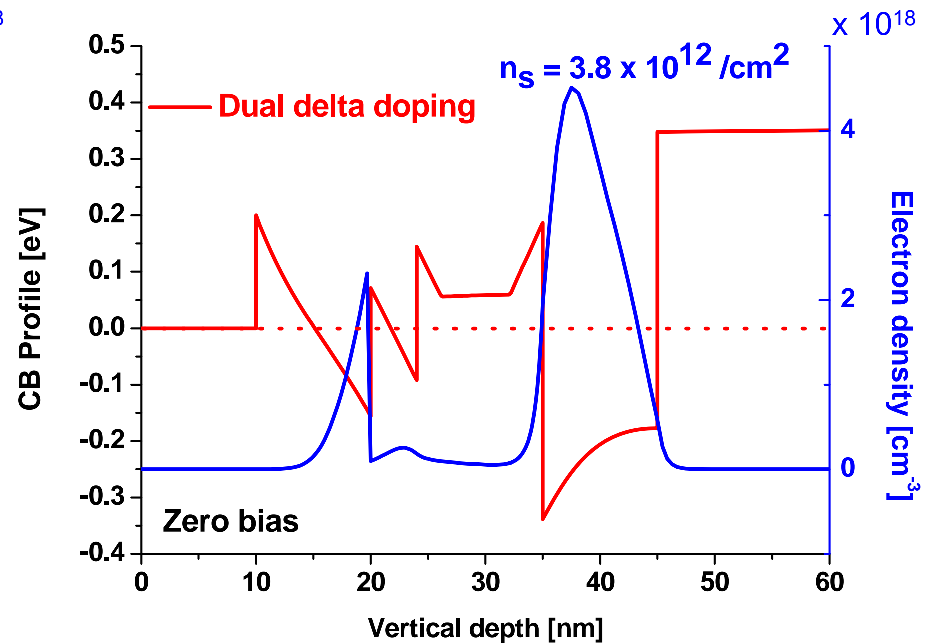
Kim, Electron Lett 2011

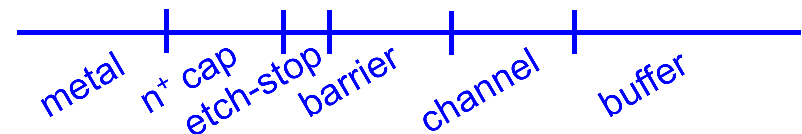
Approaches to reducing barrier and $n_{s,ext}$ ↑

- Dual delta-doping in barrier:





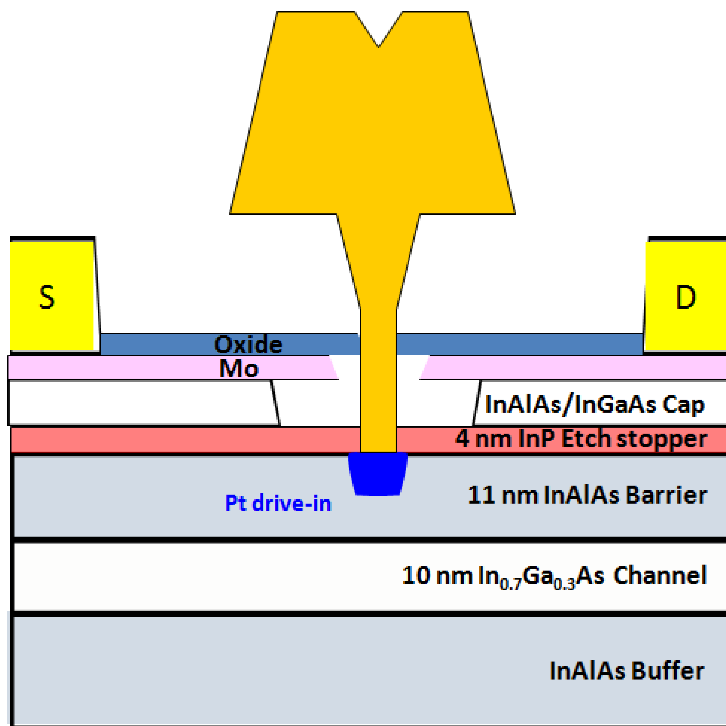


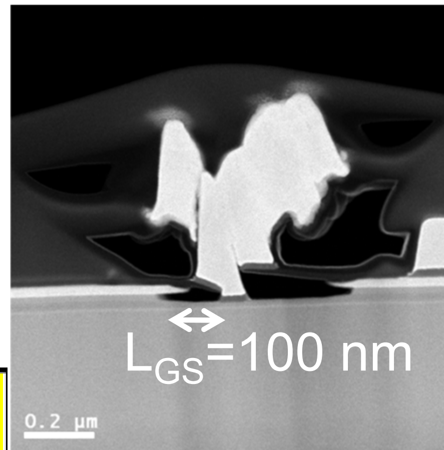


Kim, IEDM 2010

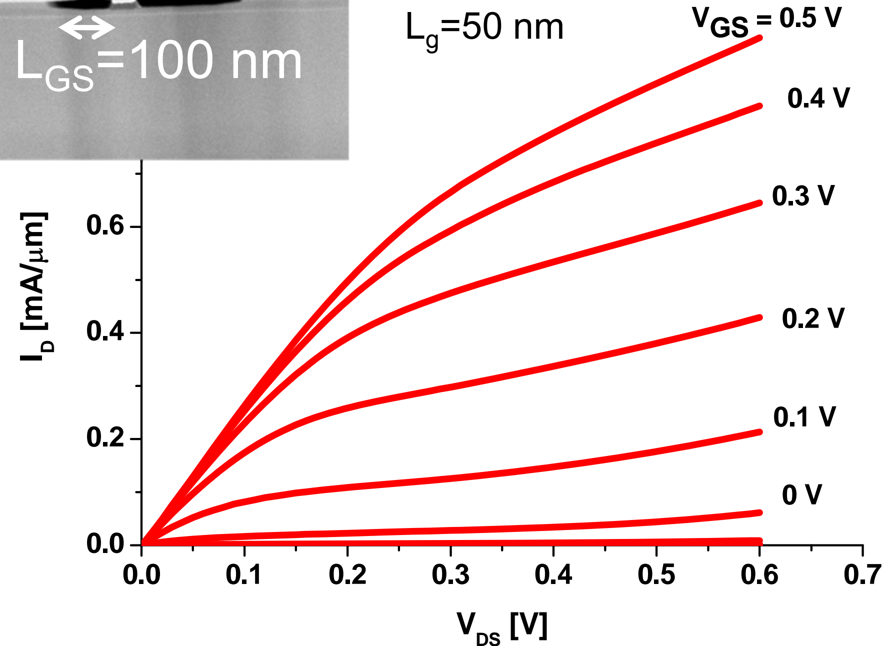
Approaches to reducing L_{GS} and L_{GD}

Self-aligned process:



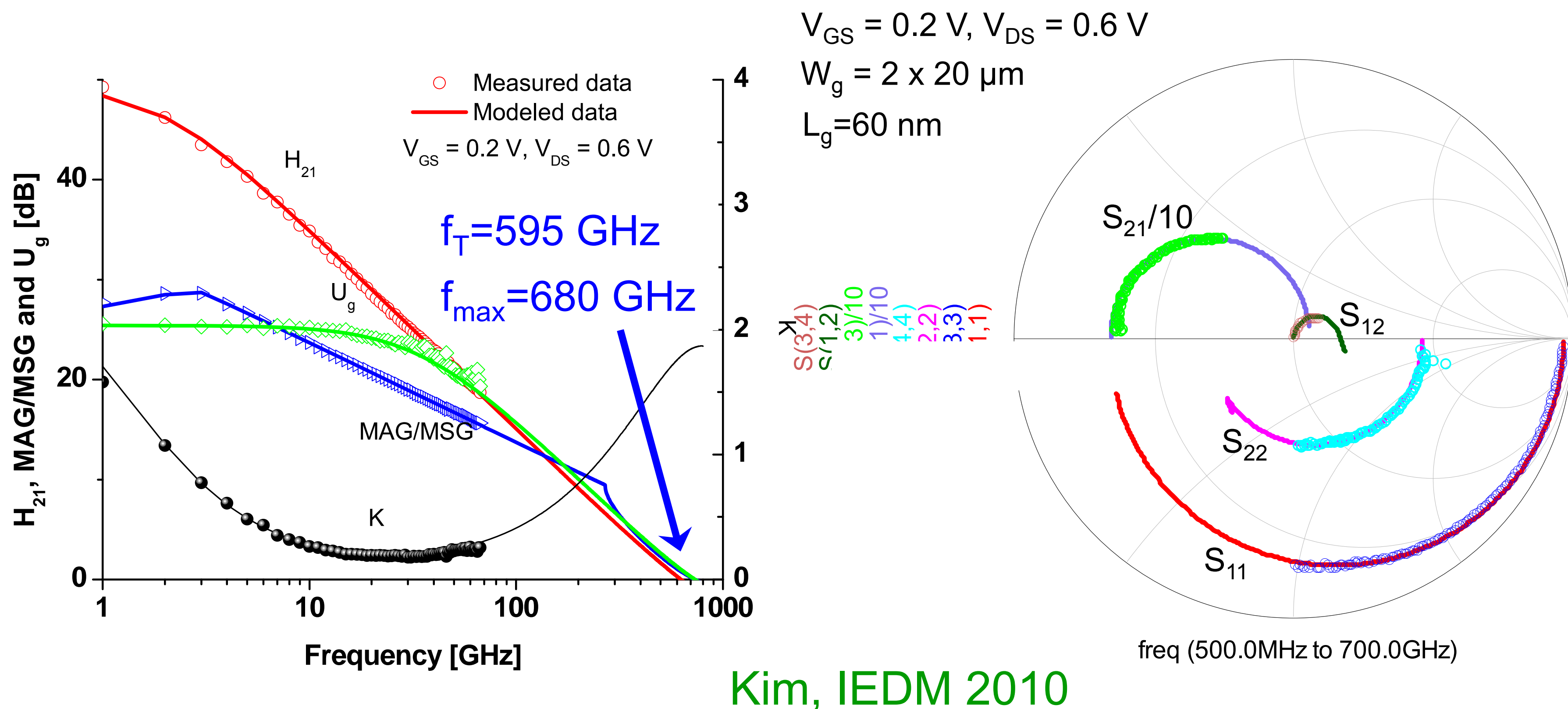


Kim, IEDM 2010



- Heterostructure with dual delta doping in InAlAs
- Dry-etched Mo contacts: R_c = 7 Ohm.μm, stable to 600 °C
- L_G=50 nm, R_S=144 Ohm.μm, g_m=2.2 mS/μm @ V_{DS}=0.5 V

L_g=60 nm self-aligned $In_{0.7}Ga_{0.3}As$ HEMT



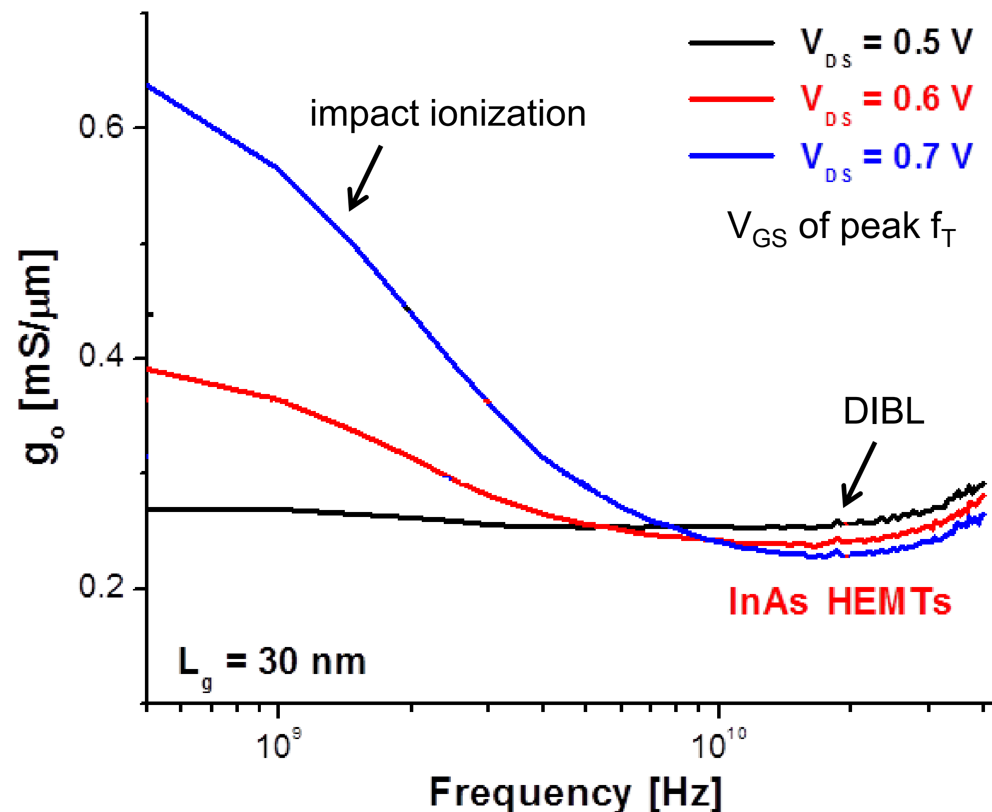
Kim, IEDM 2010

- Good agreement between modeled and measured HF characteristics
- Highest f_T and f_{max} at $L_g \geq 60$ nm of any FET

b) Increase electrostatic integrity: $g_{oi}/g_{mi}\downarrow$

Sources of output conductance in InAs HEMTs:

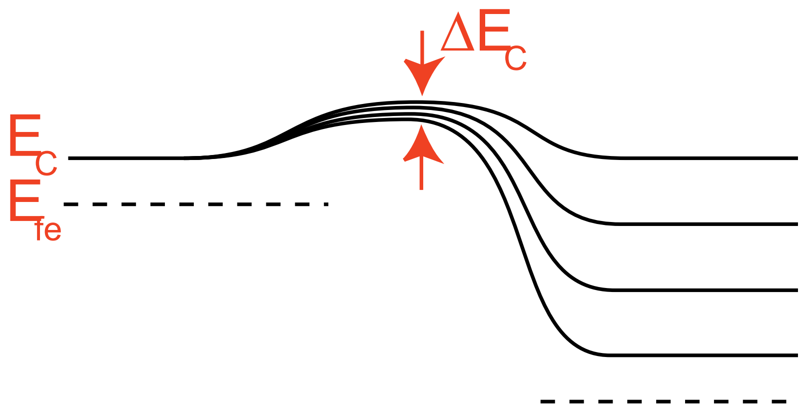
- impact ionization: slow → irrelevant at RF
- drain-induced barrier lowering (DIBL)

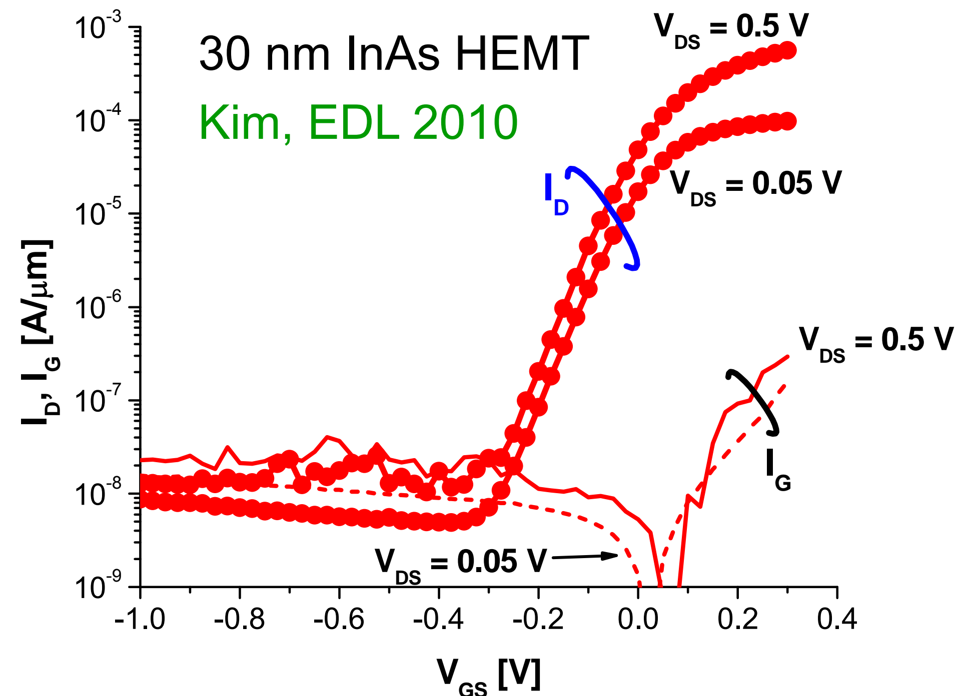


Kim, IPRM 2009

Drain-Induced Barrier Lowering (DIBL)

- Negative shift of V_T with V_{DS}
- Due to reduction in channel barrier as V_{DS} ↑





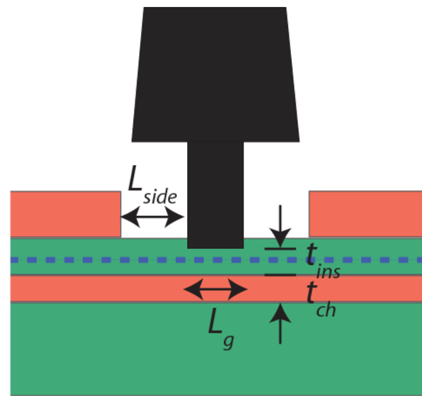
DIBL = 80 mV/V

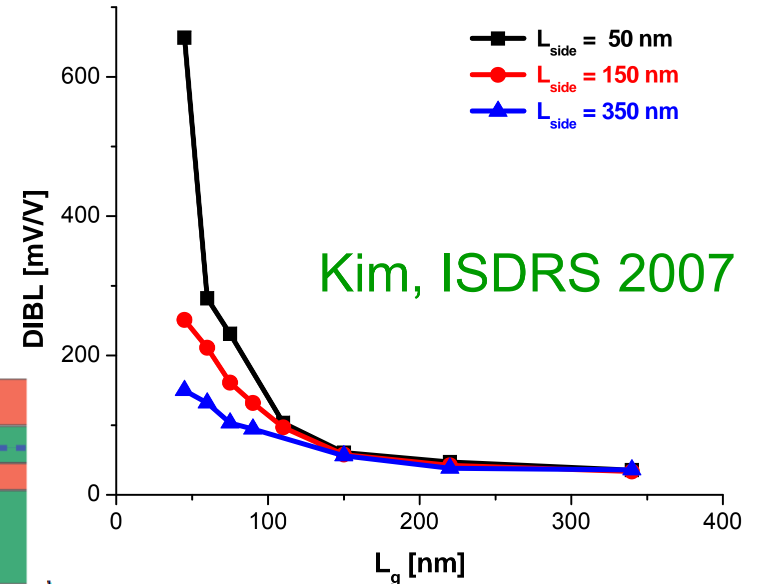
- DIBL Figure of Merit: $DIBL = \frac{dV_T}{dV_{DS}}|_{V_{GS}}$

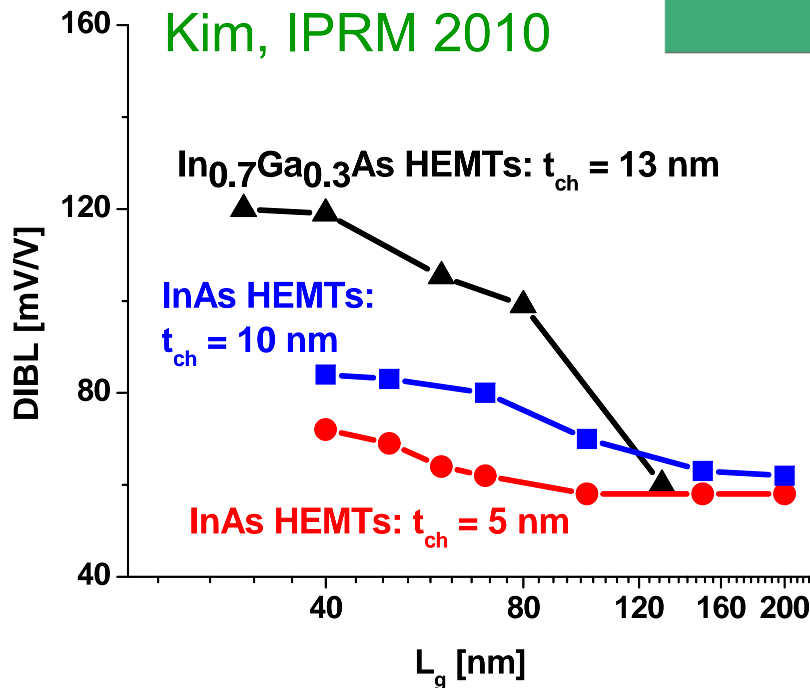
Drain-Induced Barrier Lowering (DIBL)

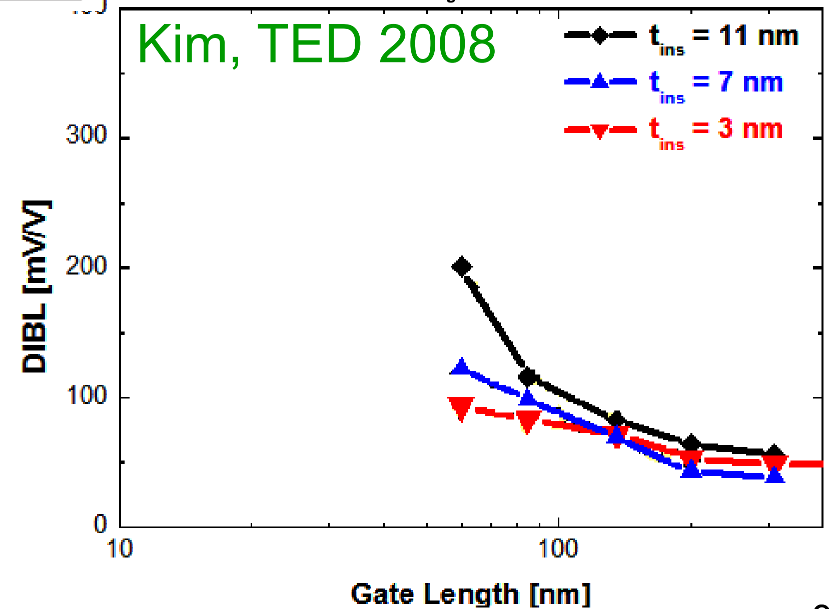
Factors affecting DIBL:

- Gate length: L_g
- Channel thickness: t_{ch}
- Barrier thickness: t_{ins}
- Side etch length: L_{side}

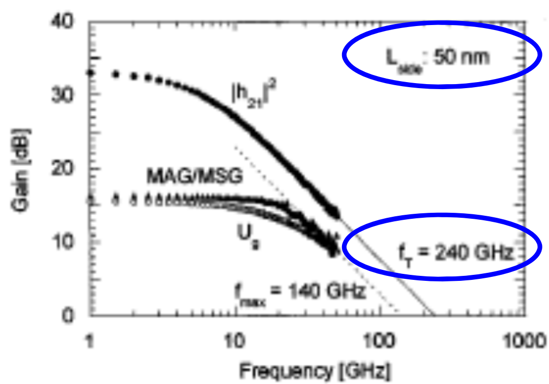








The role of L_{side} in f_T



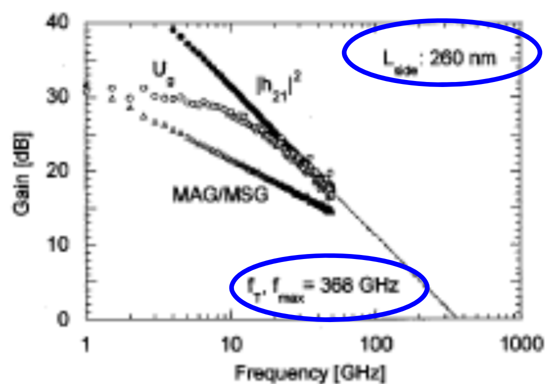
(a) L_g: 30 nm, L_{side}: 50 nm

As L_{side} ↑

→ g_{oi} ↓ → τ_{par} ↓

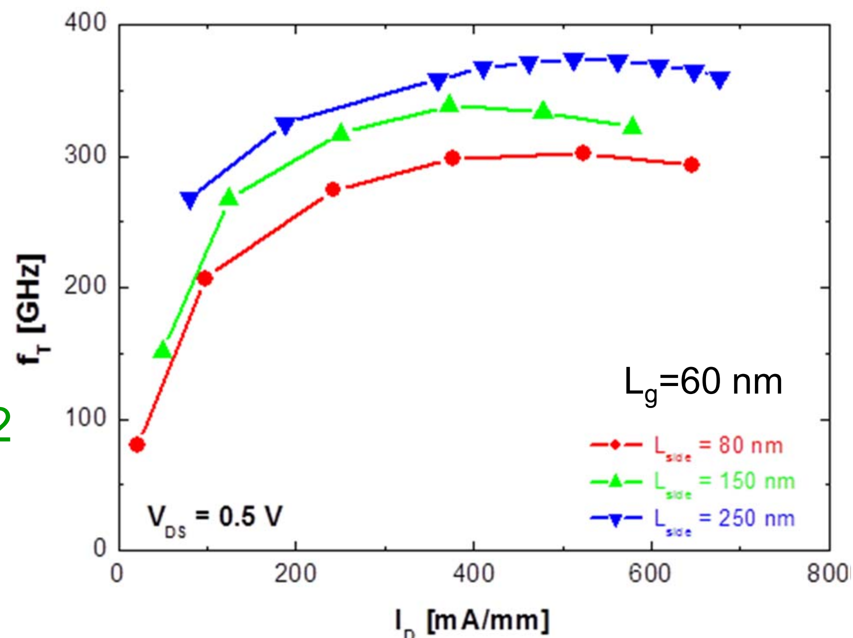
→ C_{gsext}, $C_{gd\ ext}$ ↓→ τ_{ext} ↓

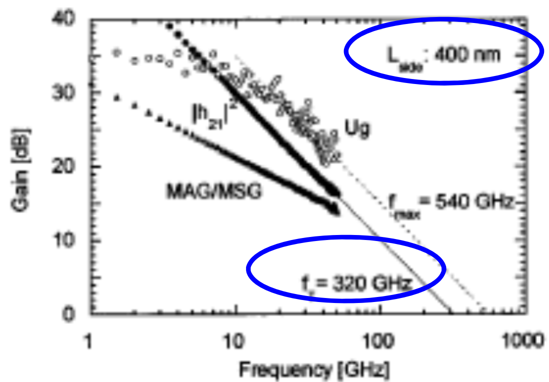
→ R_S, R_D ↑→ τ_{par} ↑



(b) L_g: 30 nm, L_{side}: 260 nm

Kim, JSTS 2006





(c) L_g: 30 nm, L_{side}: 400 nm

Suemitsu, TED 2002

There is an optimum L_{side} which depends on rest of device design

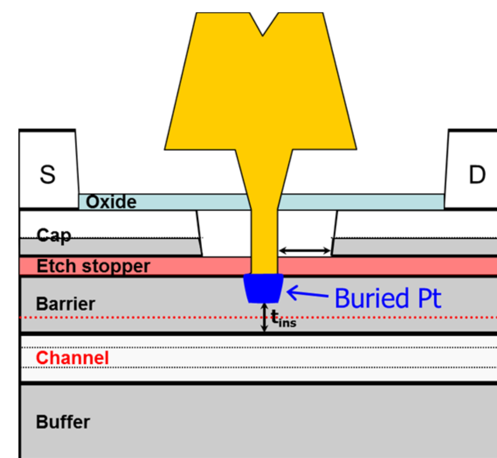
The role of t_{ins} in f_T

As t_{ins} ↓

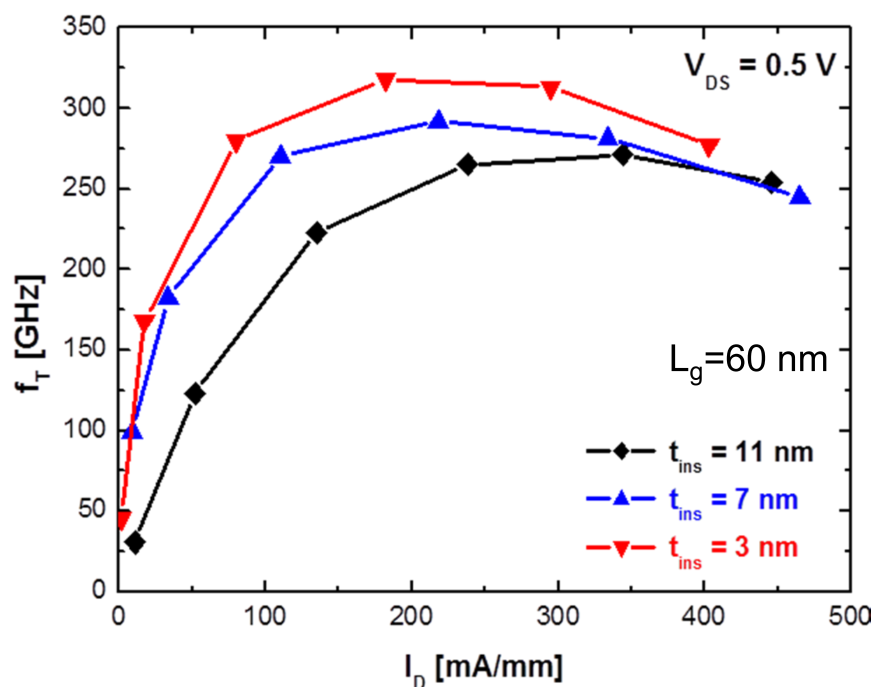
→ g_{oi} ↓ → τ_{par} ↓

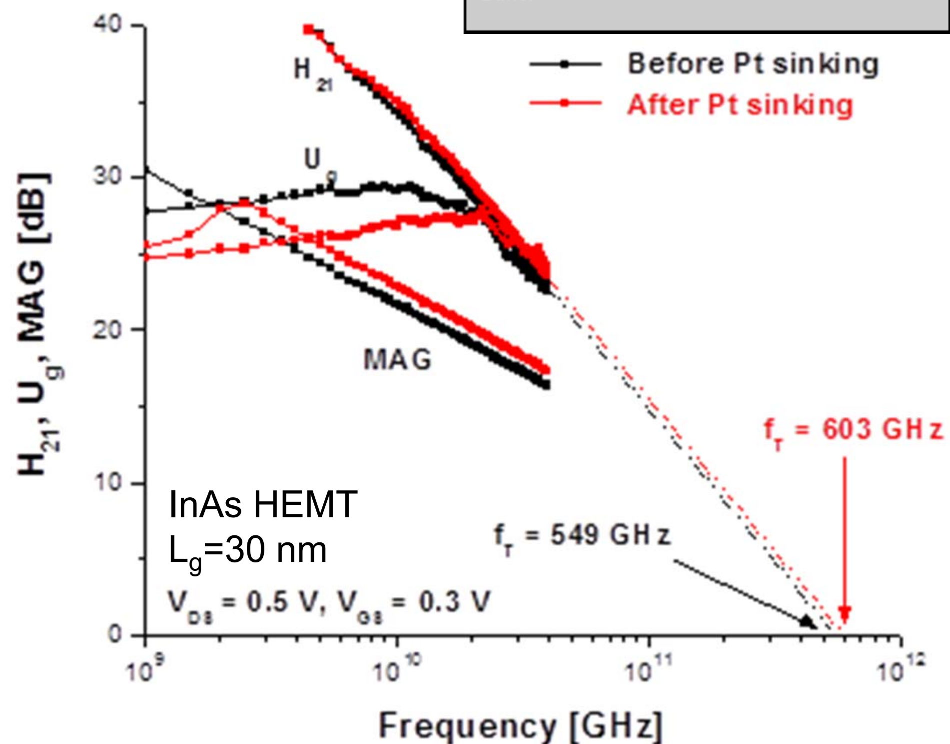
→ g_{mi} ↑ → τ_{par} ↓, τ_{ext} ↓

→ R_S, R_D ↑ → τ_{par} ↑



Kim, IEDM 2008





Kim, TED 2008

f_T tends to improve as t_{ins} ↓

The role of t_{ch} in f_T

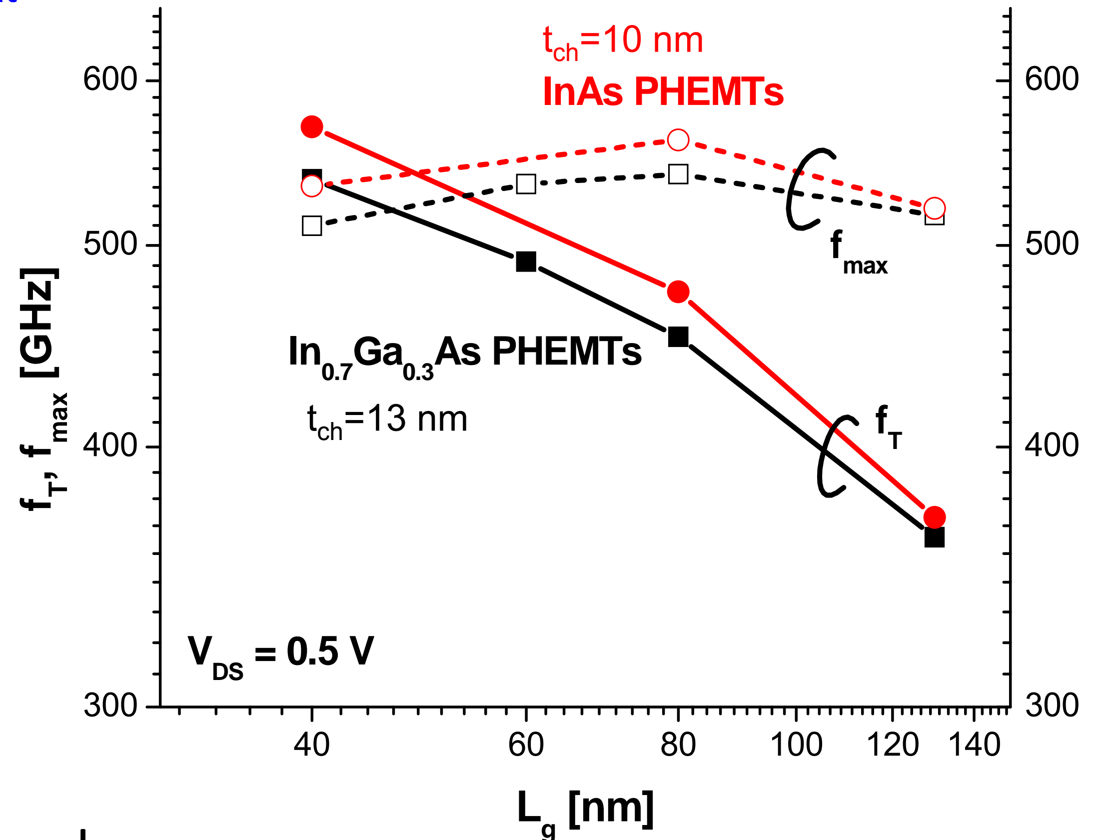
As t_{ch} ↓

→ g_{oi} ↓ → τ_{par} ↓

→ g_{mi} ↑ → τ_{par} ↓, τ_{ext} ↓

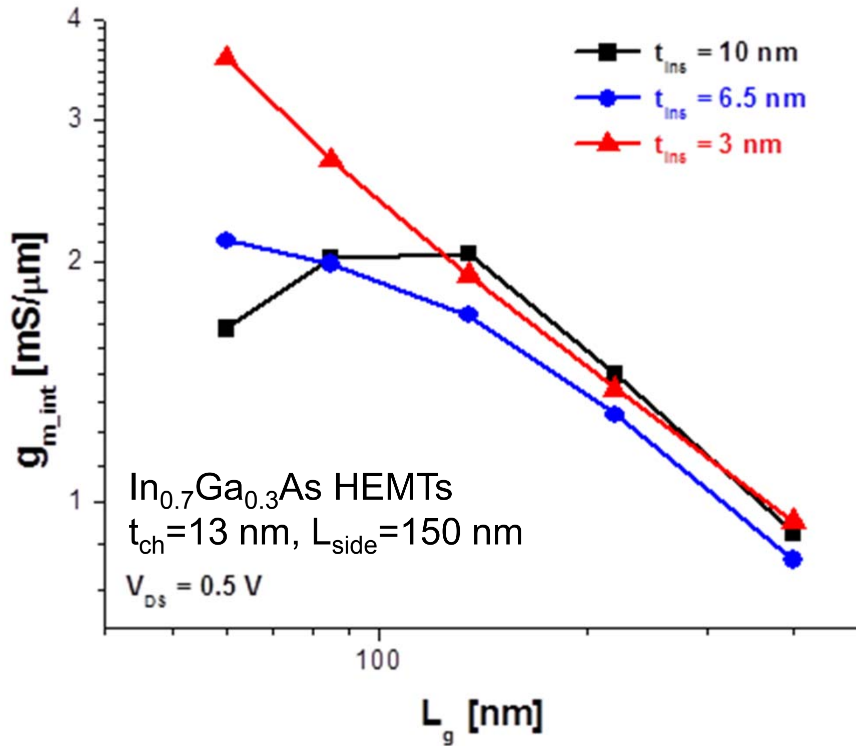
→ R_S, R_D ↑→ τ_{par} ↑

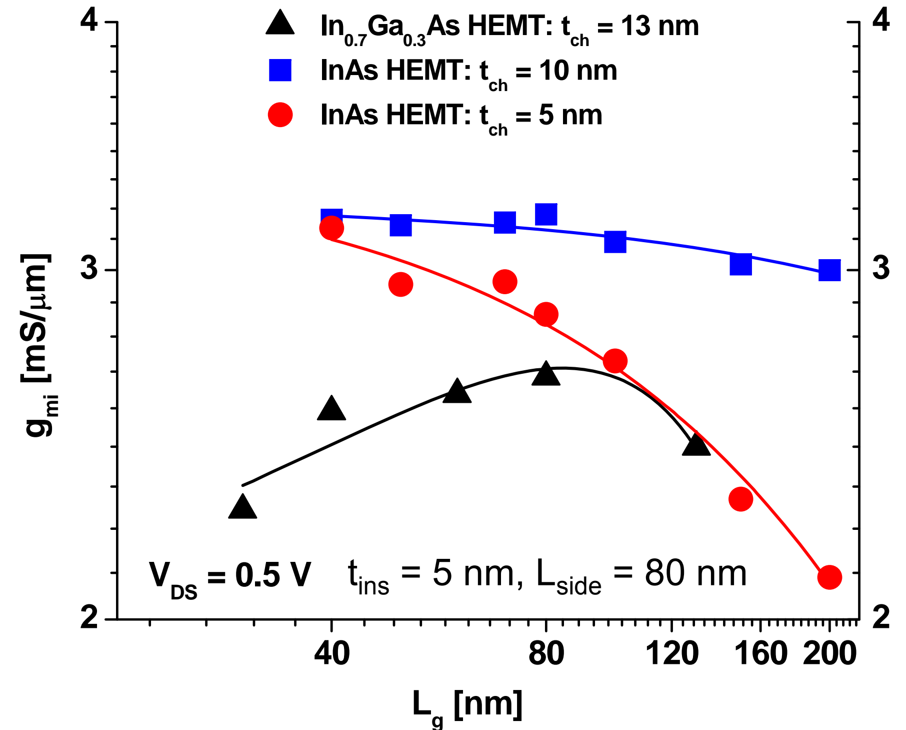
Kim, IPRM 2009



f_T tends to improve as t_{ch} ↓

c) L_g↓ without degrading g_{mi}





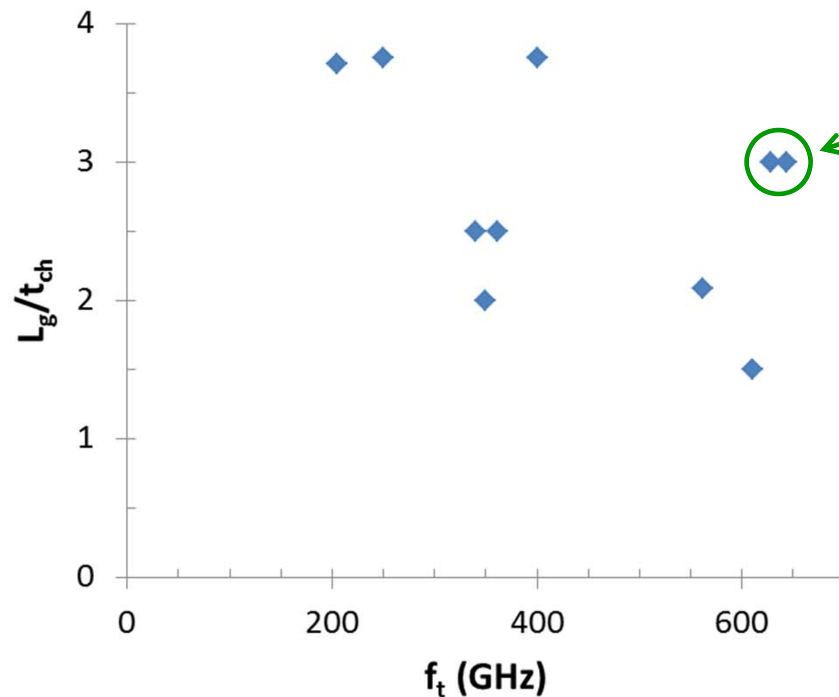
Kim, TED 2008

Kim, IPRM 2010

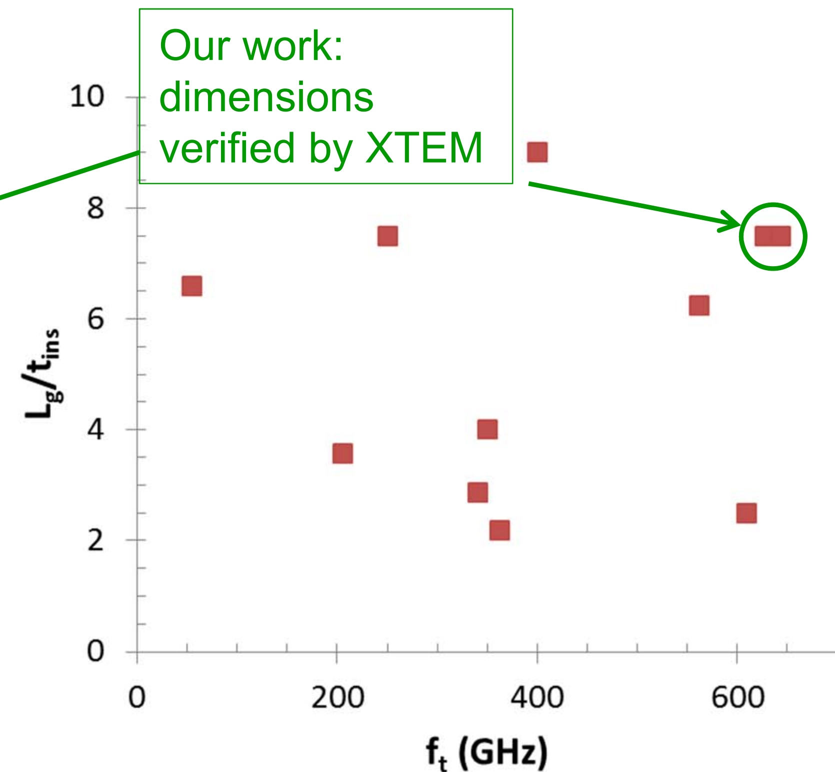
Harmonious scaling required: as L_g ↓ → t_{ch} ↓, t_{ins} ↓

Aspect ratio of record f_t devices

Channel aspect ratio: L_g/t_{ch}



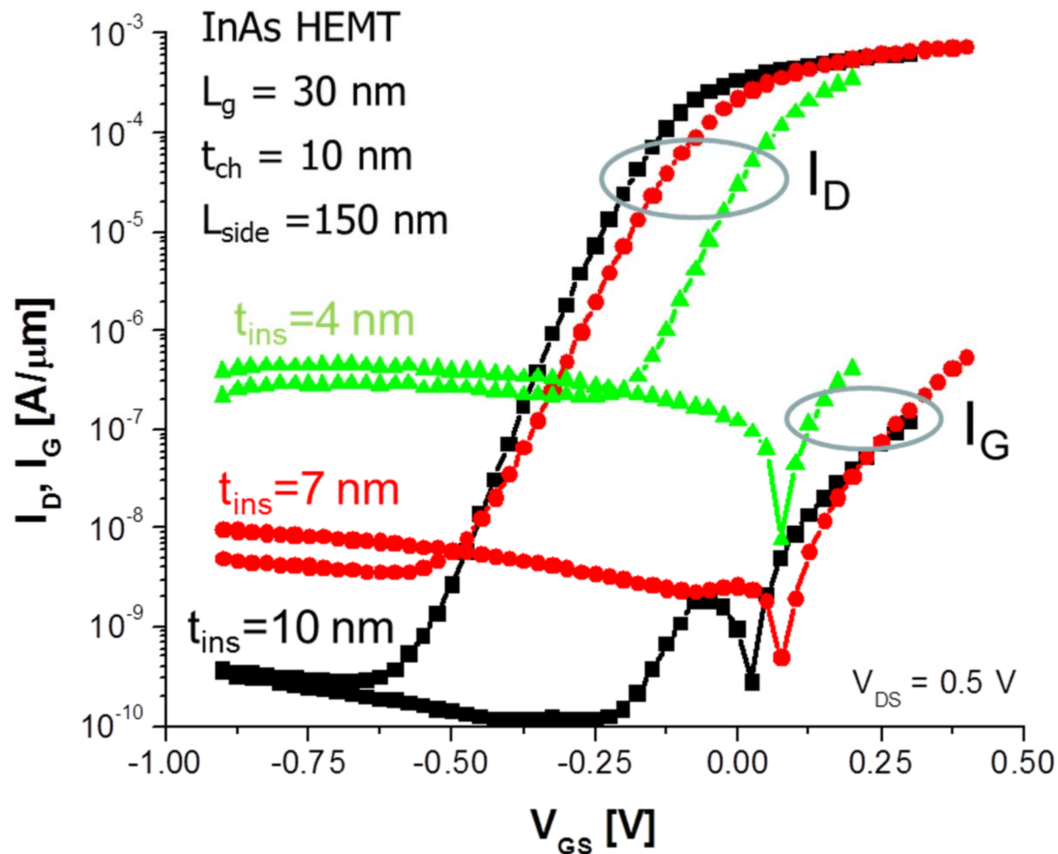
Insulator aspect ratio: L_g/t_{ins}

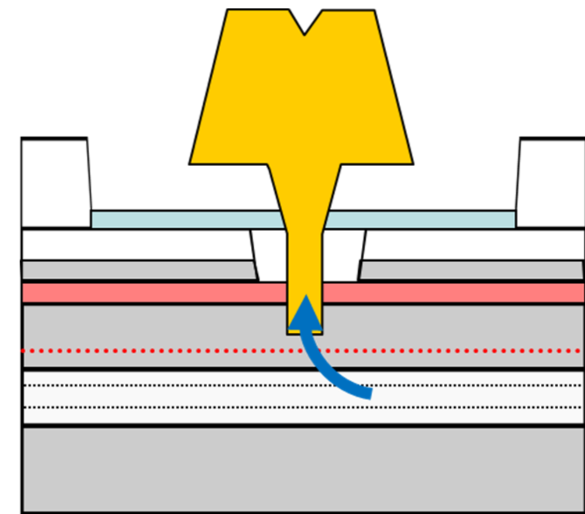


- Channel aspect ratio between 2 and 4
- Insulator aspect ratio between 2 and 8 (2 likely an underestimate)

5. Limits to HEMT scaling and future prospects

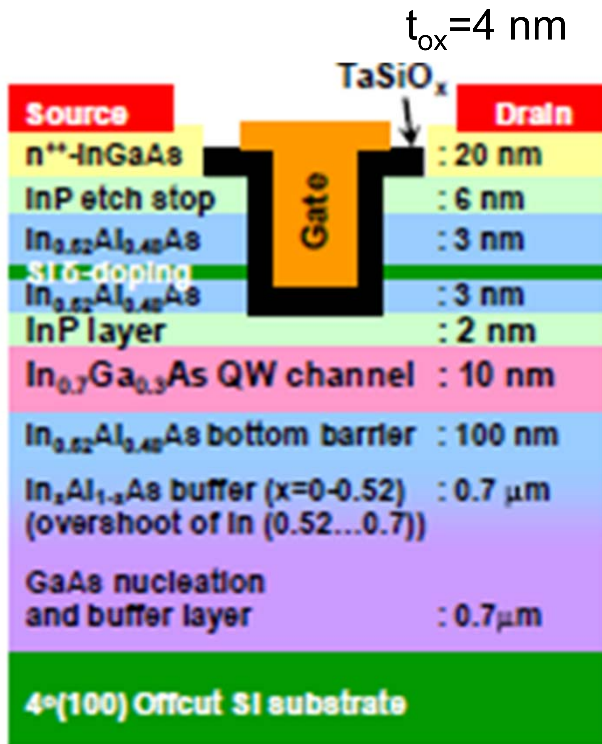
Barrier thickness scaling limited by I_G

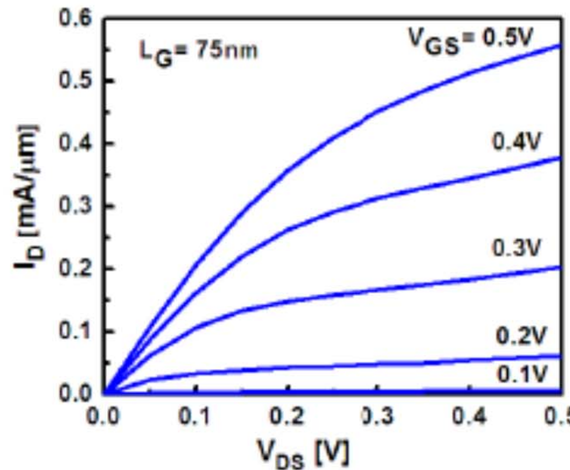


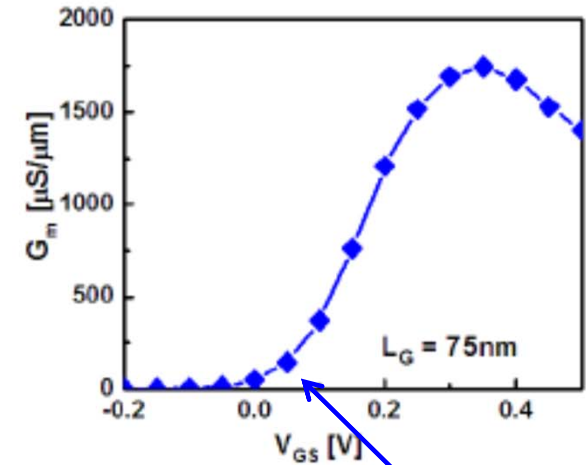


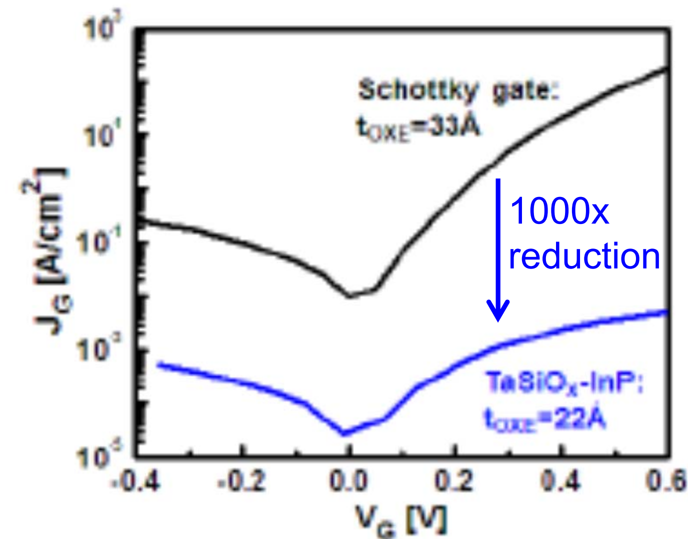
del Alamo, IPRM 2011

Alternative insulators









Radosavljevic, IEDM 2009

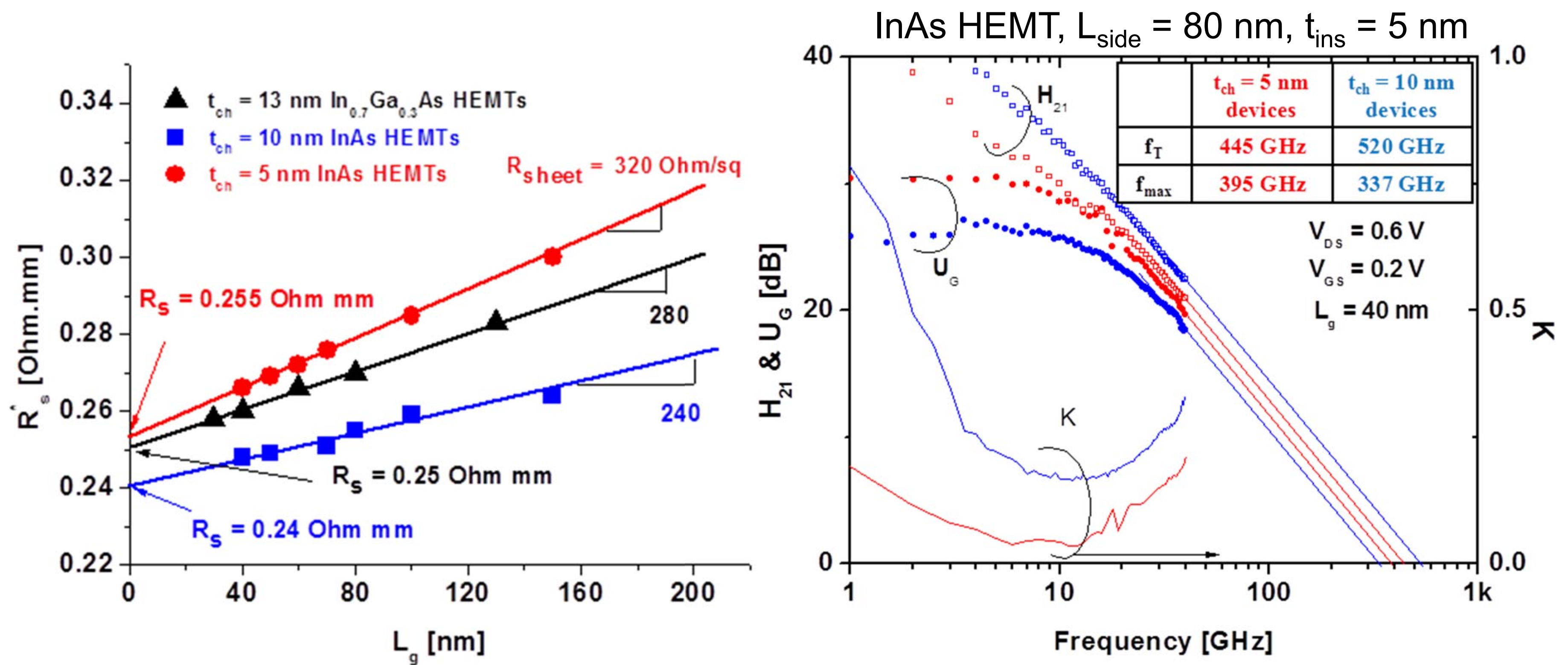
High-K dielectrics being pursued for III-V CMOS

→ huge opportunity for THz HEMT electronics!

Limits to HEMT scaling

Deep channel thickness scaling degrades performance:

→ R_S ↑ → f_T ↓



	t_{ch} = 5 nm devices	t_{ch} = 10 nm devices
f_T	445 GHz	520 GHz
f_{max}	395 GHz	337 GHz

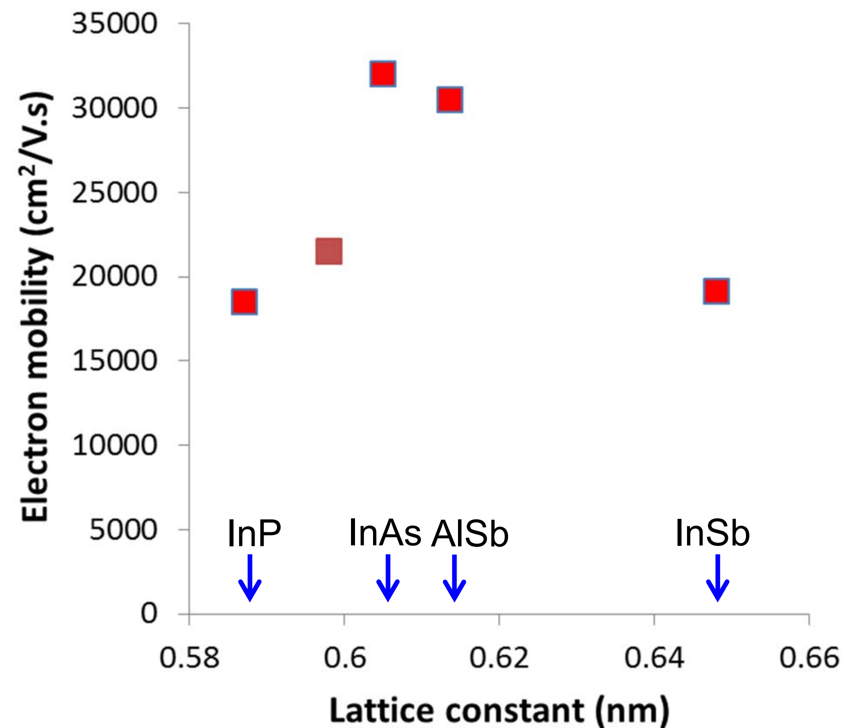
Noticeable mobility degradation: t_{ch}=10 nm → μ_e=13,500 cm^2/V.s

t_{ch}=5 nm → μ_e=9,950 cm^2/V.s

Kim, IPRM 2010

Channel strain engineering

InAs 300 K quantum-well mobility vs. lattice constant:



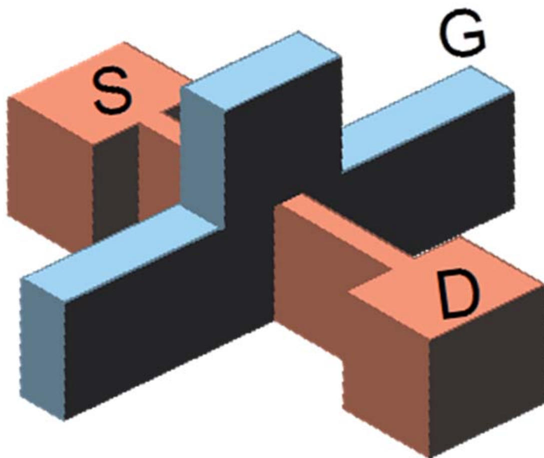
Independent control of channel strain and composition:

→ new possibilities for channel design

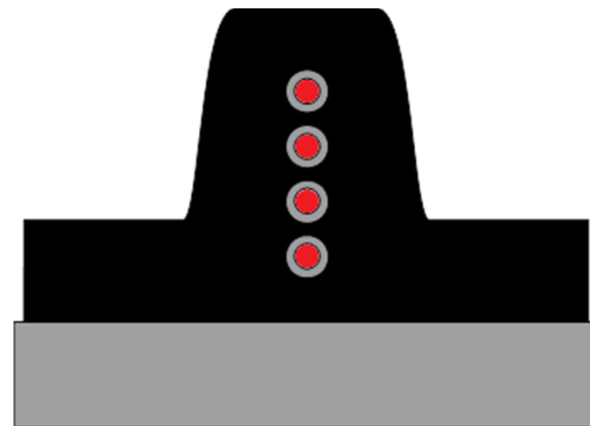
THz HEMTs: possible designs

Etched S/D QW-MOSFET

Regrown S/D QW-MOSFET



FinFET



Gate-all-around nanowire FET

Conclusion

- THz HEMTs just around the corner
- Expanding interest on III-V CMOS: huge opportunity for THz HEMT electronics

  → fast technology progress

  → new processes and tools

  → fundamental research on transport, etc.

  → Si as substrate for THz electronics