Injection Velocity in Thin-Channel InAs HEMTs

Tae-Woo Kim and Jesús A. del Alamo

Microsystems Technology Laboratories

MIT

Sponsors: Intel, FCRP-MSD

Fabrication: MTL, NSL, SEBL at MIT

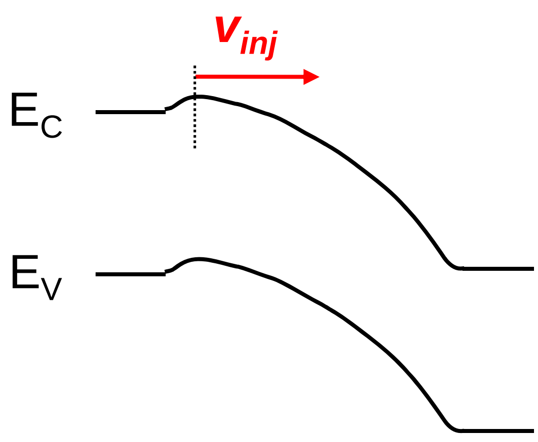
Acknowledgement: Dae-Hyun Kim (Teledyne Scientific)

IPRM

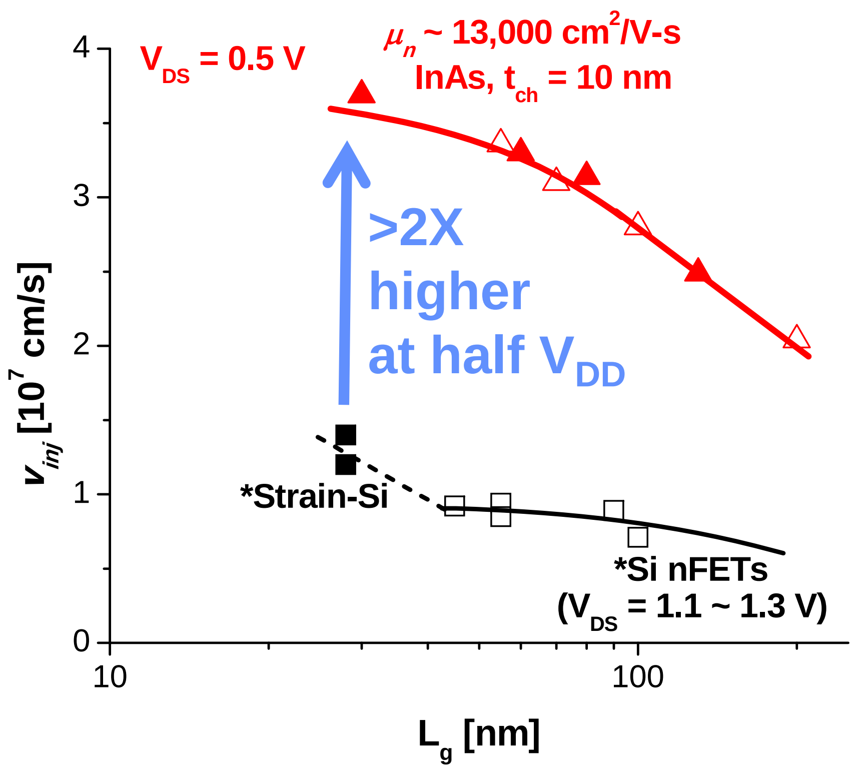
May 24th, 2011

Injection Velocity in III-V QW FETs

- Injection velocity: average velocity of electrons at virtual source
  - sets I_{ON} which determines switching speed
- Recent measurements of v_{inj} in InAs HEMTs:

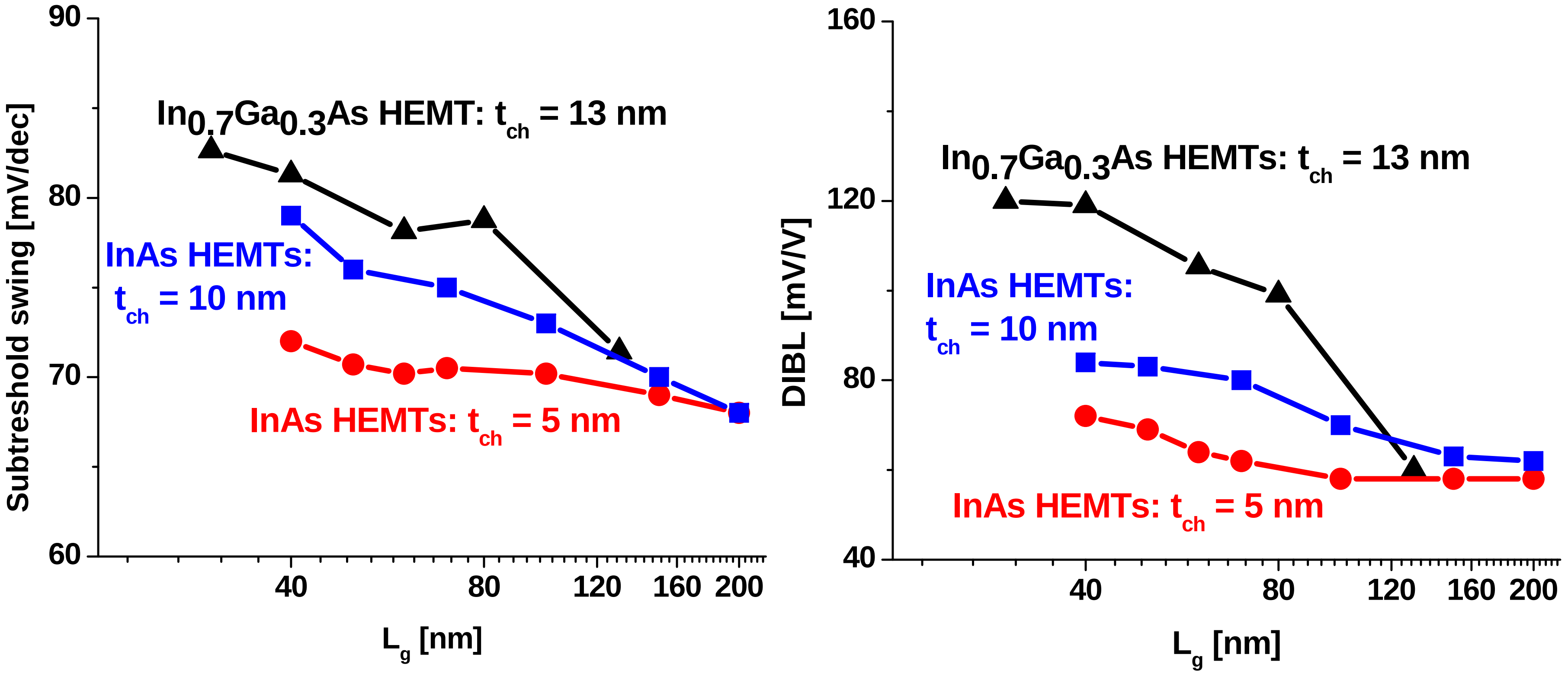


Kim, IEDM 2009



- v_{inj}(InAs) > $2v_{inj}$(Si) at less than half V_{DD}
- Derived v_{inj} values consistent with purely ballistic transport

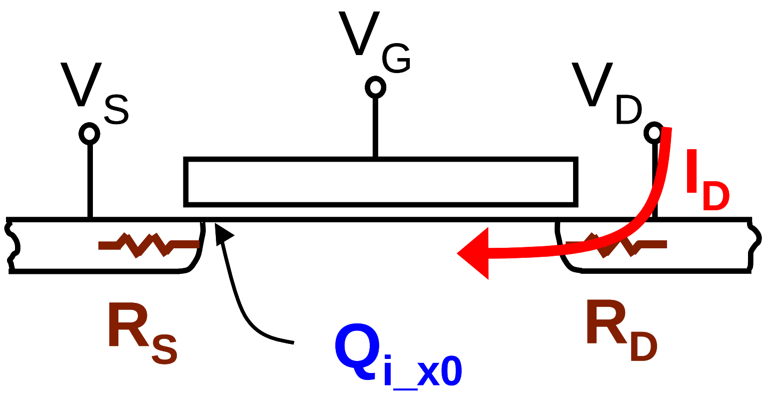
Role of channel thickness in QW-FET scalability

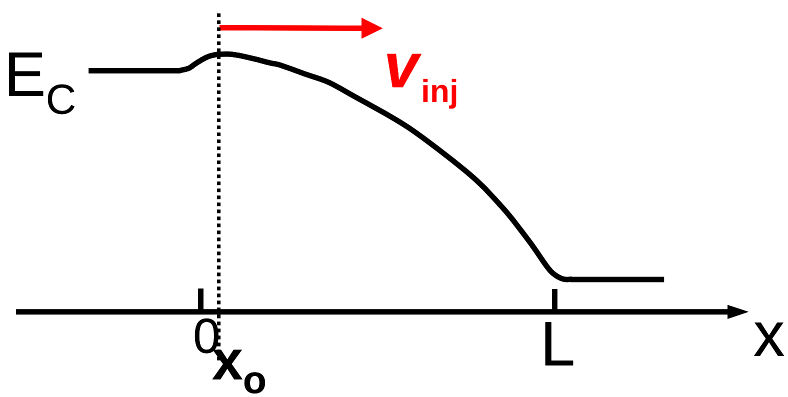


Kim, IPRM 2010

- Dramatic improvement in short-channel effects in thin-channel devices
- Concern: v_{inj} degradation in thin-channel devices?

Extraction methodology for v_{inj}





Kim, IEDM 2009

$$I_D = Q_{i\_x0} \times v_{inj} \Rightarrow v_{inj} = \frac{I_D}{Q_{i\_x0}}$$

- I_D: measured drain current
- Q_{i_x0}: sheet-charge density

$$Q_{i\_x0} = \int C_{gi}\, dV_{GS,i}$$

with C_{gi} @ V_{DS} = 10 mV

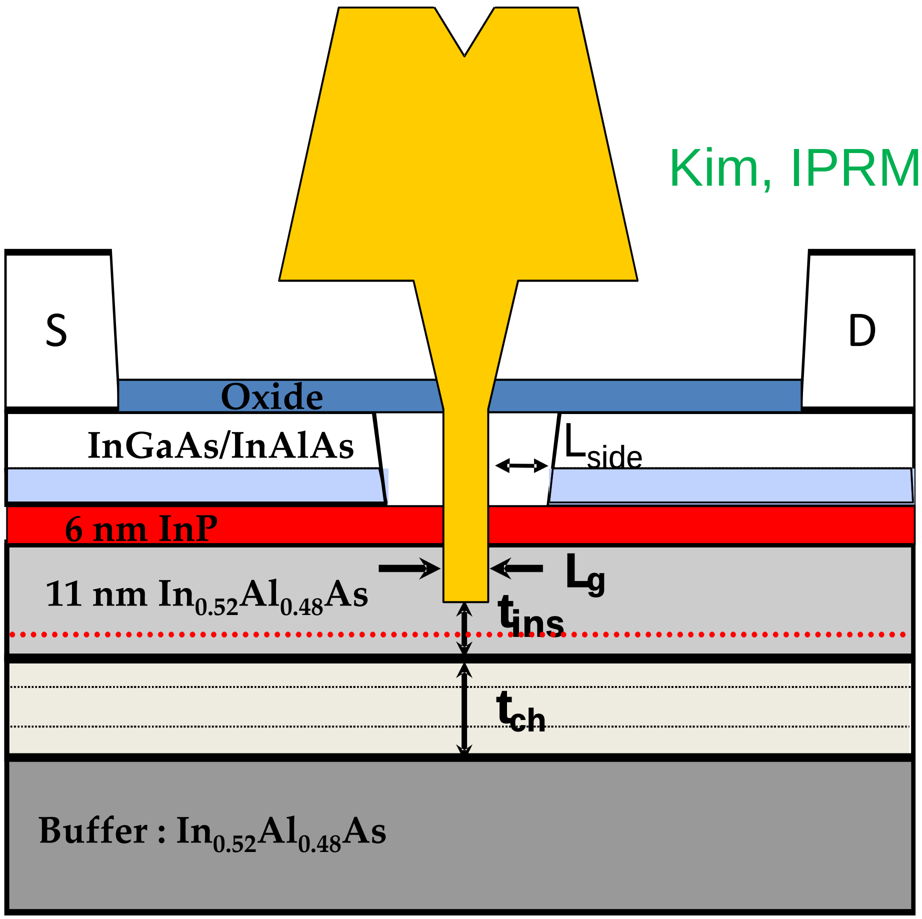
- C_{gi} extracted from S-parameters
- R_S and R_D correction:

$$V_{DSi} = V_{DS} - I_D \times (R_S + R_D)$$

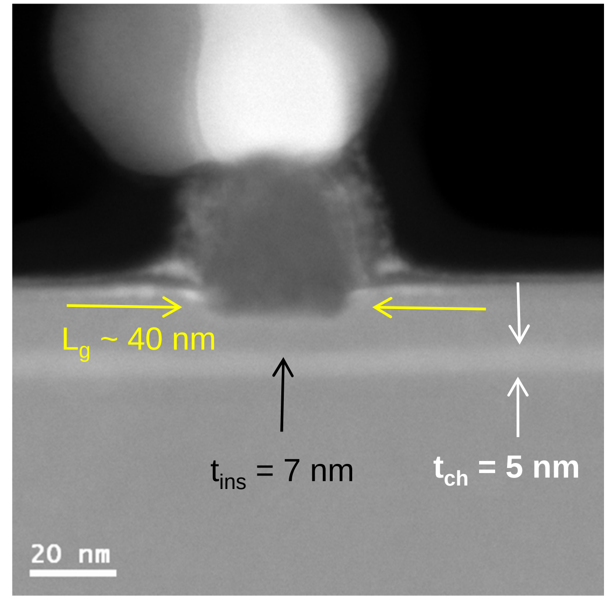
$$V_{GSi} = V_{GS} - I_D \times R_S$$

- V_T roll-off correction
- DIBL correction

Thin-channel InAs HEMTs



Kim, IPRM 2010



$In_{0.7}Ga_{0.3}As$: 1 nm
InAs: 2 nm
$In_{0.7}Ga_{0.3}As$: 2 nm
} t_{ch} = 5 nm

$\mu_{n,Hall}$ = 9,950 cm^2/V-sec

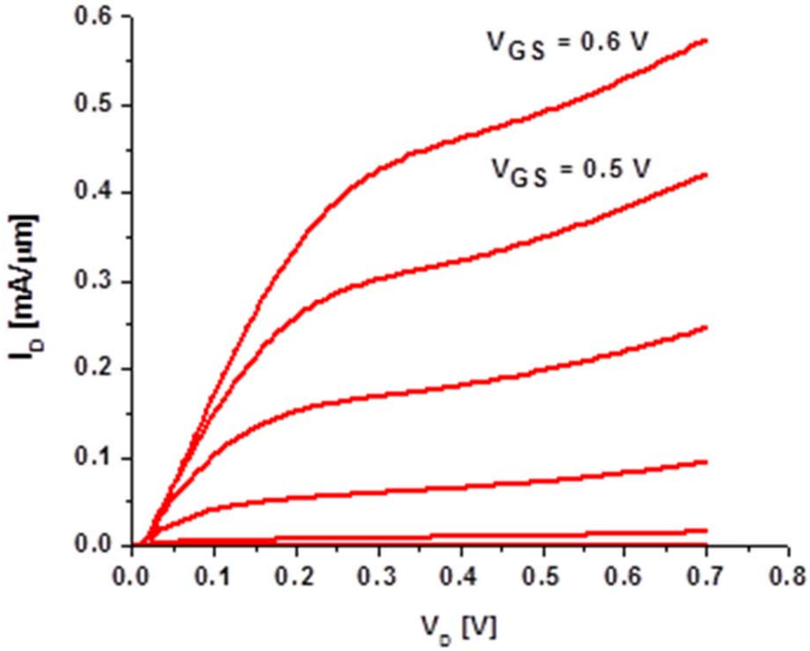
- Triple-step gate recess process
- Gate metal stack: Ti/Pt/Au
- L_g = 40 ~ 200 nm
- L_{side} = 80 nm, t_{ins} = 3, 7 nm

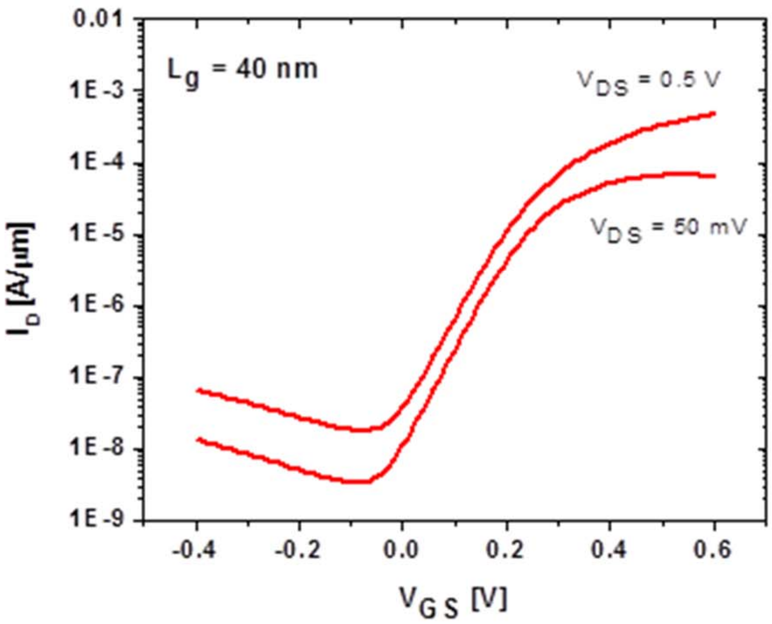
Reference:

- InAs HEMT with t_{ch} = 10 nm
- $\mu_{n,Hall}$ = 13,500 cm^2/V-sec

Kim, IEDM 2008

I-V Characteristics: L_g = 40 nm with t_{ins}=3 nm

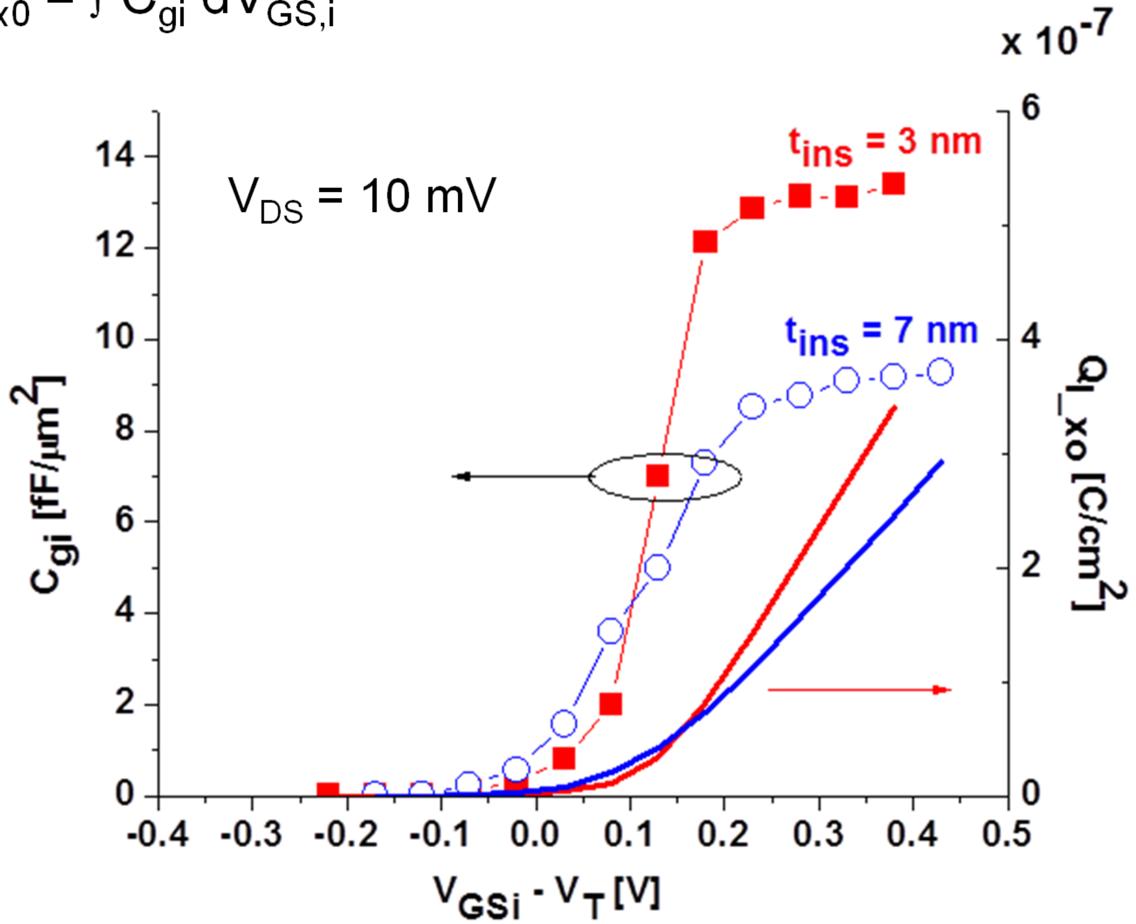




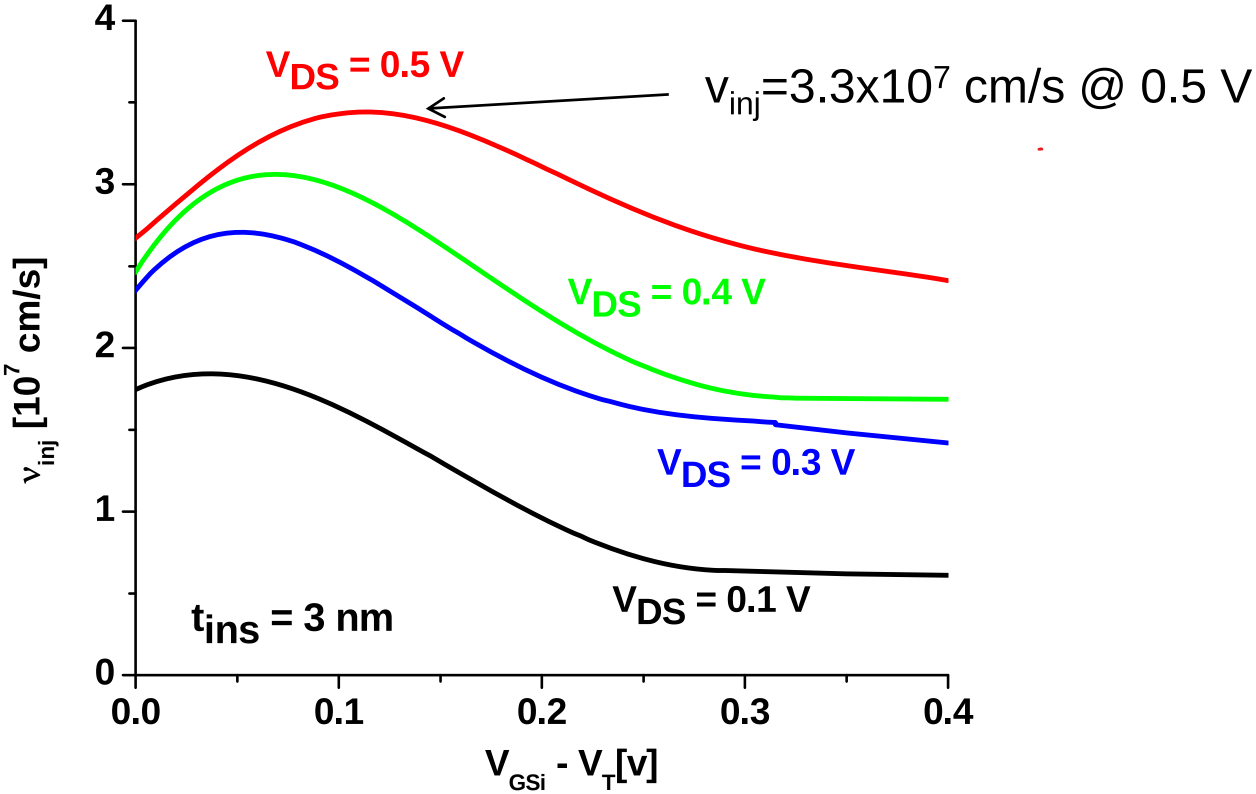
- V_T = 0.11 V, S = 65 mV/dec, DIBL = 50 mV/V
- g_m=1.6 mS/µm, R_S=275 Ohm-µm

Extraction of Q_{i_x0}

- C_{gi} extracted from S-parameters @ V_{DS} = 10 mV
- Parasitic capacitance removed
- $Q_{i\_x0} = \int C_{gi}\, dV_{GS,i}$



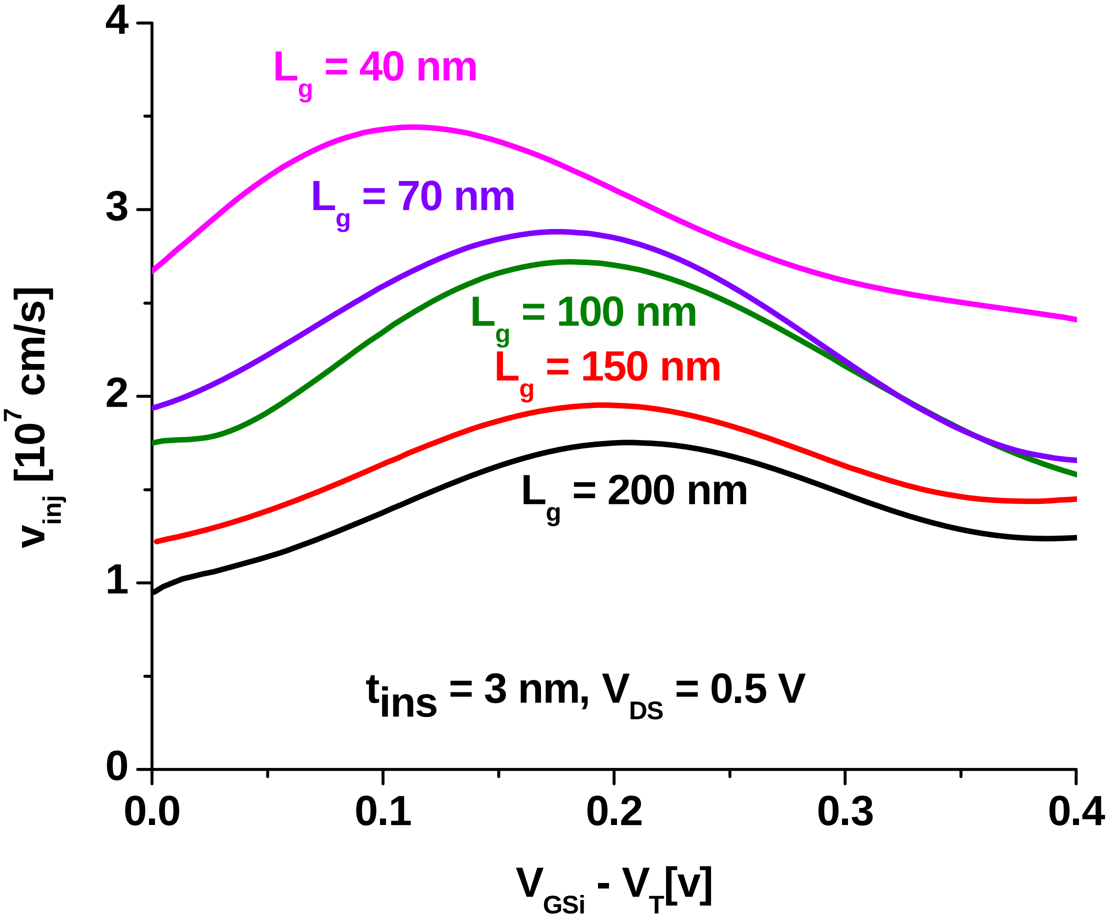
v_{inj} of L_g=40 nm t_{ins}=3 nm InAs HEMTs



- V_{DS} ↑ → v_{inj} ↑ (device driven into saturation)
- V_{GSi}-V_T ↑ → v_{inj} initially ↑ (because Q_{i_xo} ↑)

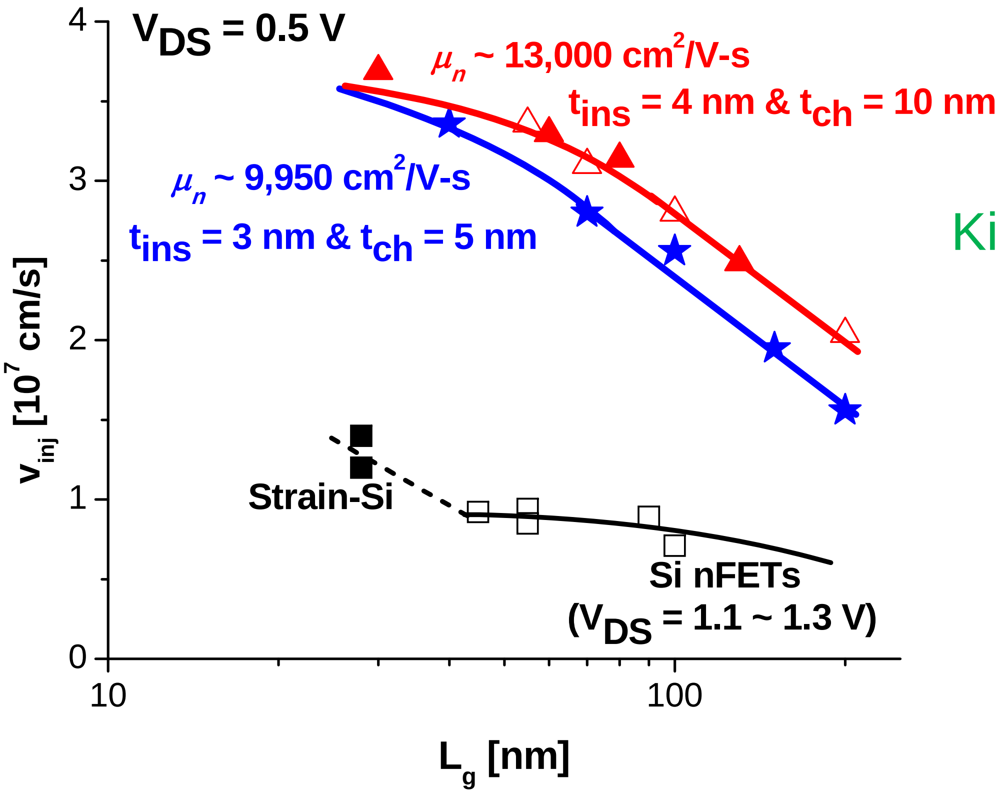
  → then v_{inj} ↓ (device driven into linear regime)

v_{inj} vs. L_g



$L_g \downarrow \rightarrow v_{inj} \uparrow$

v_{inj} - impact of channel thickness



Kim, IEDM 2009

In thin-channel devices:

- Long L_g: v_{inj} decreases right along with μ_e (~23%)
- Short L_g: v_{inj} relatively unaffected

→ consistent with ballistic transport

Conclusions

- Thin-channel InAs HEMTs with t_{ch}=5 nm:

  - Evidence of mobility degradation

  - Small degradation in injection velocity for short L_g FETs:

$$v_{inj} = 3.3 \times 10^7 \text{ cm/s at } L_g = 40 \text{ nm}$$

- Great scaling potential of thin-channel FETs

- Key question:

  - Can v_{inj} be preserved if severe μ degradation (~3000 cm^2/V.s)?