

## Logic Characteristics of 40 nm thin-channel InAs HEMTs

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### Abstract

We have experimentally investigated the trade-offs involved in thinning down the channel of III-V FETs with the ultimate goal of enhancing the electrostatic integrity and scalability of these devices. To do so, we have fabricated InAs HEMTs with a channel thickness of  $t_{ch} = 5$  nm and we have compared them against, InAs HEMTs with  $t_{ch} = 10$  nm. The fabricated thin-channel devices exhibit outstanding logic performance and scalability down to 40 nm in gate length.  $L_g = 40$  nm devices exhibit  $S = 72$  mV/dec, DIBL = 72 mV/V, and  $I_{ON}/I_{OFF} = 2.5 \times 10^4$ , all at  $V_{DS} = 0.5$  V. However, there are trade-offs of using a thin channel which manifest themselves in a higher source resistance, lower transconductance, and lower  $f_T$  when compared with InAs HEMTs with  $t_{ch} = 10$  nm.

### INTRODUCTION

As conventional Si CMOS scaling approaches the end of the roadmap, III-V based MOSFETs are being considered as an alternative technology to continue transistor size scaling [1-2]. In the quest to map the potential of III-Vs for future CMOS applications, the High Electron Mobility Transistor (HEMT) has emerged as a valuable model system to understand fundamental physical and technological issues. In fact, recently, excellent logic characteristics have been demonstrated in InAs HEMTs with gate length as small as 30 nm [3-4]. This is mainly a result of the outstanding electron transport properties of InAs and the use of a thin quantum well channel. Further scalability to  $L_g = 10$  nm dimension characteristic of a future III-V CMOS technology will require harmonious scaling of all relevant device dimensions including the channel thickness. A consequence of very thin channel is that carrier transport deteriorates, mainly as a result of increased carrier scattering [5]. This can detract from performance.

In order to understand the trade-offs involved in thinning the channel in sub-100 nm III-V FETs, we have experimentally investigated the characteristics of InAs HEMTs with a 5 nm thick channel. This is half the value of earlier device demonstrations from our group [4]. We show that a very thin channel design substantially improves short channel effects (SCEs) and output conductance ( $g_o$ ) characteristics but deteriorates its transport properties and access resistance. Future self-aligned gate (SAG) device architectures should be able to mitigate these problems.

### PROCESS TECHNOLOGY

Fig. 1 shows a schematic cross sectional view of the device

giving the details of the epitaxial layer structure. This heterostructure is essentially identical to that of our previous InAs HEMT designs [4] except that the channel consists of a multilayer structure with a 2 nm thick pure InAs core surrounded by a 1 nm  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  top cladding and a 2 nm  $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$  bottom cladding layer. In an epi wafer with an identical heterostructure except for a simpler 10 nm InGaAs capping layer with  $1 \times 10^{18}$  / $\text{cm}^3$  Si doping, the Hall mobility ( $\mu_{n,\text{Hall}}$ ) and carrier density ( $n_s$ ) were 9,950  $\text{cm}^2/\text{V}\cdot\text{s}$  and  $2.5 \times 10^{12}$  / $\text{cm}^3$ . This is about 30 % lower than the value obtained in a 10 nm thick channel InAs HEMT heterostructure with a 5 nm InAs core [6] and reveals the increased carrier scattering that comes with channel thickness scaling.

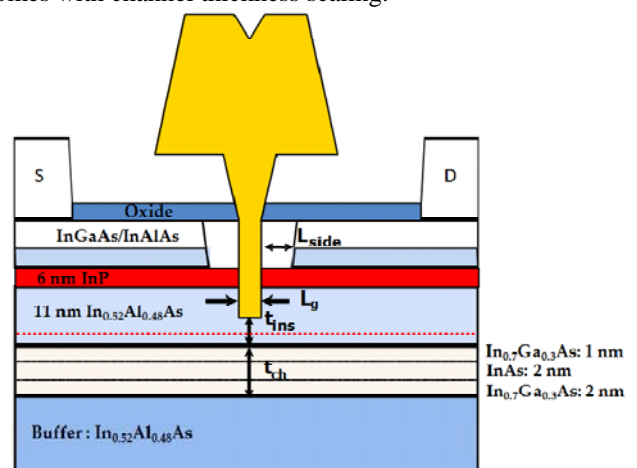


Fig. 1 Schematic of thin-channel InAs HEMT. The heterostructure features a 5 nm total channel thickness that includes a 2 nm InAs core channel layer.

Device fabrication closely follows our previous device demonstrations [6]. We used a three-step gate recess process that yielded an InAlAs barrier thickness in the intrinsic region,  $t_{\text{ins}}$ , of about 4 nm and a Ti/Pt/Au (20/20/300 nm) T-gate with gate-cap edge distance  $L_{\text{side}} = 80$  nm. We have fabricated devices with  $L_g$  values in the range of 40 to 200 nm.

For reference, we simultaneously fabricated devices on an InAs HEMT heterostructure with  $t_{\text{ch}} = 10$  nm that it is very similar to an epi wafer structure that we have processed earlier [6]. These devices have gone through an identical process and should therefore have closely matched dimensions.

### DC AND LOGIC CHARACTERISTICS

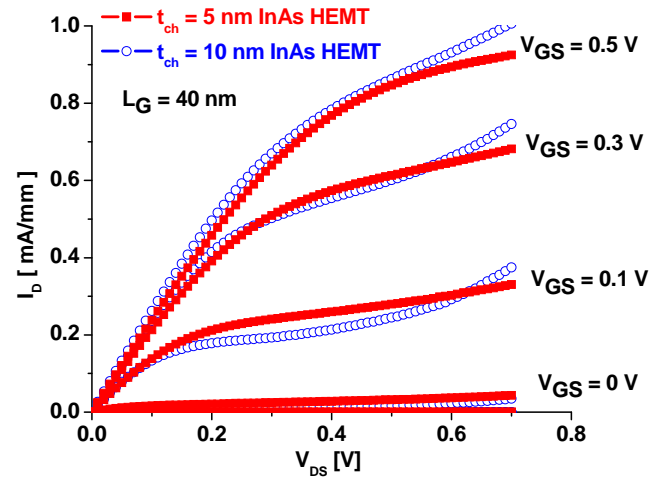
**Fig. 2** shows the output characteristics of 40 nm gate length InAs HEMTs on both heterostructures. Both devices exhibit excellent pinch-off and saturation characteristics up to  $V_{\text{DS}} = 0.7$  V. The threshold voltages of both devices are  $-0.22$  V at 1 mA/mm of  $I_{\text{D}}$  and  $V_{\text{DS}} = 0.5$  V. Interestingly, the thin channel device show much better output conductance. This is expected as a result of reduced impact ionization and  $V_{\text{T}}$  dependence on  $V_{\text{DS}}$  (DIBL, discussed below). These are both a product of a thin highly quantized channel. However, the thin-channel HEMTs exhibit slightly higher  $R_{\text{ON}}$ .

**Fig. 3** shows subthreshold and gate current characteristics of both 40 nm InAs HEMTs at  $V_{\text{DS}} = 50$  mV and 0.5 V. The thin-channel ( $t_{\text{ch}} = 5$  nm) device shows much shaper subthreshold swing and much less threshold voltage shift with  $V_{\text{DS}}$  (DIBL) than the thick-channel ( $t_{\text{ch}} = 10$  nm) device. For the  $t_{\text{ch}} = 5$  nm device, the subthreshold swing (S) is 72 mV/dec, the drain-induced-barrier-lowering (DIBL) is 72 mV/V, and the  $I_{\text{ON}}/I_{\text{OFF}}$  ratio is  $2.5 \times 10^4$ . These results compare favorably with those obtained on the  $t_{\text{ch}} = 10$  nm device which are 79 mV/dec, 84 mV/V, and  $9 \times 10^3$ , respectively.

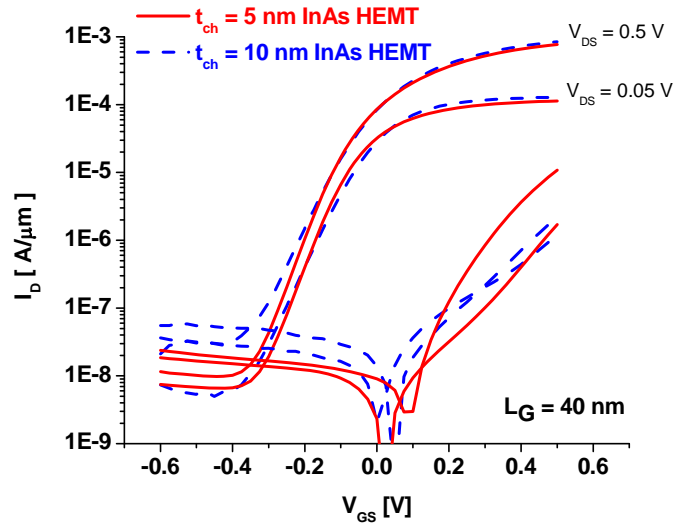
**Fig. 4** shows typical transconductance characteristics of both InAs HEMTs at  $V_{\text{DS}} = 0.5$  V. The 5 nm thick channel device exhibits a maximum transconductance of 1.65 S/mm, while the 10 nm channel HEMT shows 1.75 S/mm.

**Fig. 5** shows the subthreshold and gate leakage current characteristics of thin channel InAs HEMTs from  $L_g = 200$  nm to 40 nm at  $V_{\text{DS}} = 0.5$  V. There is a very small  $V_{\text{T}}$  shift of less than 34 mV as the gate length scales down from 200 to 40 nm. In contrast, the  $V_{\text{T}}$  shift of the 10 nm thick devices over the same gate length range is 55 mV.

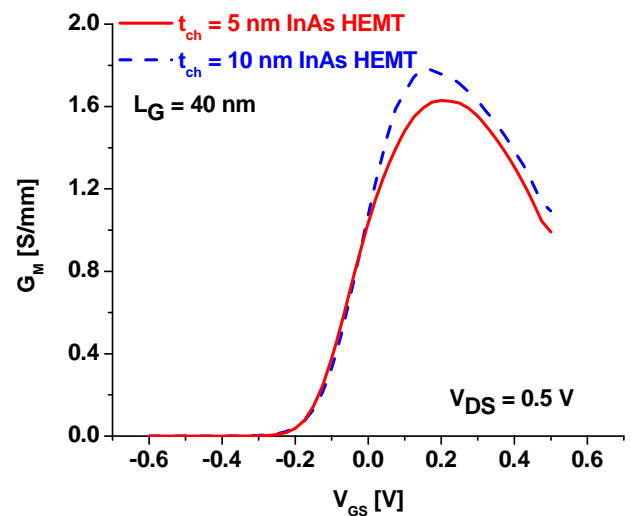
The superior scalability of the 5 nm devices is also manifested in the evolution of S and DIBL with  $L_g$  (**Fig. 6** and **Fig. 7**). These figures also include result from an earlier set of devices with a 13 nm InGaAs channel, and similar value of  $L_{\text{side}}$  and  $t_{\text{ins}}$  [3]. It is clear that thinning down the channel brings significant benefits in terms of improved electrostatic integrity and scalability.



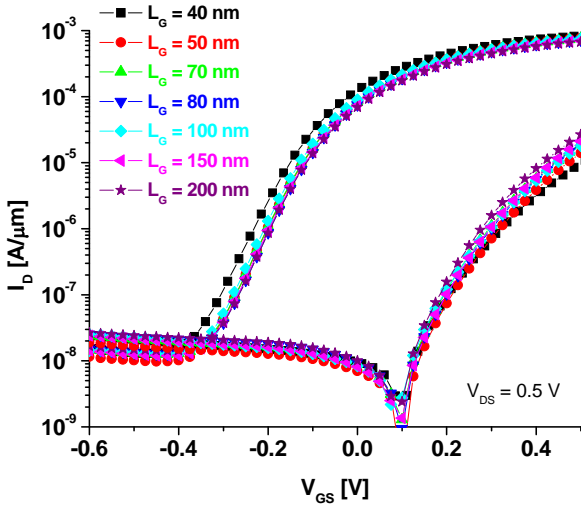
**Fig. 2** Output characteristics for both 40 nm gate length InAs HEMTs.



**Fig. 3** Subthreshold and gate leakage characteristics for both 40 nm gate length InAs HEMTs.



**Fig. 4** Transconductance characteristics for both 40 nm gate length InAs HEMTs.

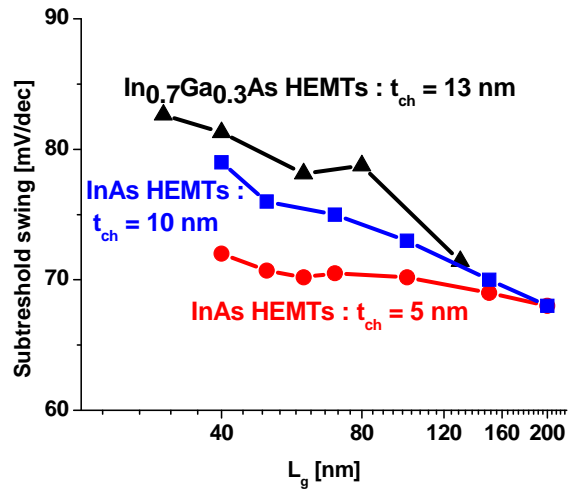


**Fig. 5** Subthreshold and  $I_G$  characteristics for 5 nm thick channel InAs HEMTs with different values of  $L_g$  at  $V_{DS} = 0.5$  V.

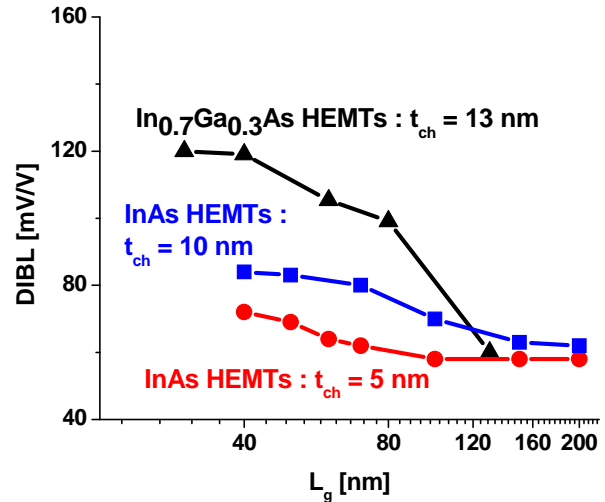
The increased  $R_{ON}$  observed in **Fig. 2** and the decreased transconductance observed in **Fig. 4** for the thin channel device also points out the trade-offs of the present approach. They essentially arise from enhanced scattering which translates into lower channel electron mobility. **Fig. 8** shows the evolution of the transconductance as a function of gate length at  $V_{DD} = 0.5$  V for the three types of devices. At all gate lengths, the present devices exhibit a lower extrinsic transconductance than the 10 nm thick channel InAs HEMTs but better than the 13 nm thick channel InGaAs HEMTs which show poor scalability.

To understand this result better, we have carried out measurements of the effective source resistance,  $R_S^*$ , using the gate current injection method [7]. As shown in **Fig. 9**,  $R_S^*$  can be extracted by linear extrapolation to zero  $L_g$ . The extracted  $R_S^*$  for thin channel devices is 0.255 Ohm•mm, in contrast with 0.24 Ohm•mm for the 10 nm thick channel devices and 0.25 Ohm•mm for the 13 nm thick channel devices. In addition, we found that devices with the 5 nm thick channel exhibit a higher sheet resistance (320 Ohm/sq) in the channel region when compared with 240 Ohm/sq for the 10 nm InAs HEMTs and 280 Ohm/sq of the 13 nm InGaAs HEMTs. Self-aligned gate (SAG) device architectures should be able to partially mitigate this problem.

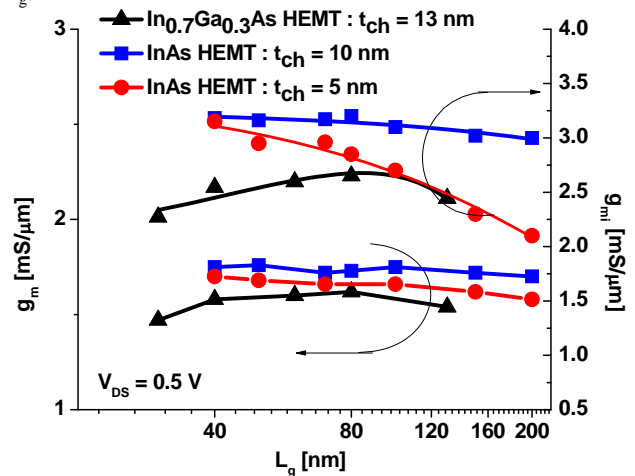
Using these measurements, we have extracted the intrinsic transconductance of our transistors. Our extraction accounts for the effects of output conductance ( $g_o$ ),  $R_S$ , and  $R_D$ . **Fig. 8** shows a reduced value of  $g_{mi}$  for the thin channel when compared with the 10 nm thick channel devices but better scalability. In fact, at  $L_g = 40$  nm, the intrinsic transconductance is about the same in both transistors. It seems reasonable to expect that for shorter gate lengths, the thin channel device will surpass the thicker designs in terms of intrinsic transconductance as it should continue to scale much better.



**Fig. 6** Subthreshold swing of InAs HEMTs with  $t_{ch} = 5$  nm and 10 nm as well as  $In_{0.7}Ga_{0.3}As$  HEMTs with  $t_{ch} = 13$  nm as a function of  $L_g$ .



**Fig. 7** DIBL of InAs HEMTs with  $t_{ch} = 5$  nm and 10 nm as well as  $In_{0.7}Ga_{0.3}As$  HEMTs with  $t_{ch} = 13$  nm as a function of  $L_g$ .



**Fig. 8** Intrinsic transconductance ( $g_{mi}$ ) and extrinsic transconductance ( $g_m$ ) as a function of gate length.

## MICROWAVE CHARACTERISTICS

Small-signal microwave performance was characterized from 0.5 to 40 GHz. On-wafer open and short patterns were used to subtract pad capacitances and inductances from the measured device S-parameters. **Fig. 10** plots current gain ( $H_{21}$ ) and unilateral gain ( $U_g$ ) as a function of frequency for the best bias conditions at  $V_{GS} = 0.2$  V and  $V_{DS} = 0.6$  V for  $L_g = 40$  nm thin and thick channel InAs HEMTs. Values of  $f_T = 445$  GHz and  $f_{max} = 395$  GHz have been obtained for the  $t_{ch} = 5$  nm device while values of  $f_T = 520$  GHz and  $f_{max} = 337$  GHz have been obtained for the  $t_{ch} = 10$  nm device. For the 5 nm channel device,  $f_T$  is lower but  $f_{max}$  is higher. Low  $f_T$  mainly comes from a high source resistance and a higher gate capacitance without any higher intrinsic transconductance which reflects a lower velocity. The higher  $f_{max}$  is due to the improved output conductance ( $g_o$ ) characteristics which arise from the reduced impact ionization and strong electron confinement. This is shown in **Fig. 11** which graphs the output conductance ( $g_o$ ) as a function of  $I_D$  for three different devices with  $L_g = 40$  nm. As  $I_D$  increases, 5 nm thick channel InAs HEMTs exhibit much better output conductance ( $g_o$ ) than the 10 nm thick InAs HEMTs.

## CONCLUSION

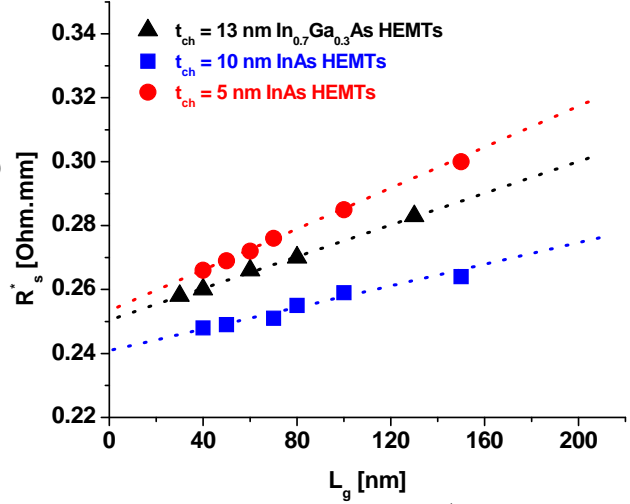
We have demonstrated 40 nm InAs HEMTs with a 5 nm thick channel. The devices show excellent short-channel effects and scalability although their performance suffers from an increased source resistance. In particular, 40 nm devices exhibits  $S = 72$  mV/dec, DIBL = 72 mV/V, and  $I_{ON}/I_{OFF} = 2.5 \times 10^4$ . These encouraging results stem from the combination of the outstanding transport properties of InAs and the tight electron confinement afforded by the thin channel. But there are trade-offs in the thin channel approaches which are related to degraded transport properties and access resistance. However, future self-aligned gate (SAG) device architectures should be able to mitigate these problems. This work suggests that future thin InAs channel MOSFETs have the potential for scaling to very small dimensions.

## REFERENCE

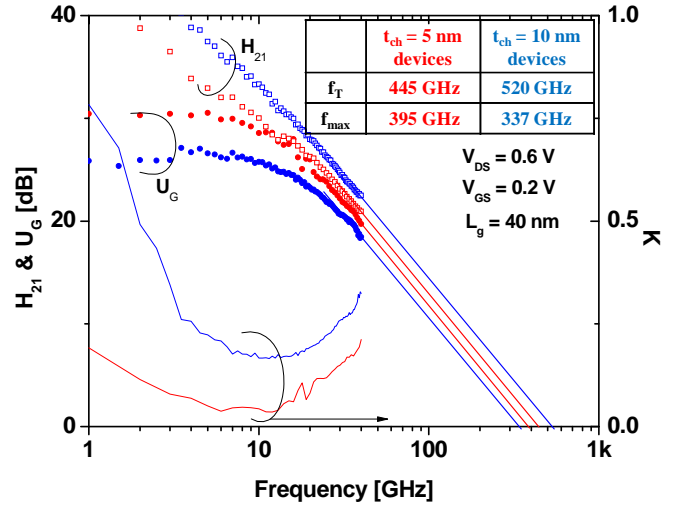
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## ACKNOWLEDGEMENTS

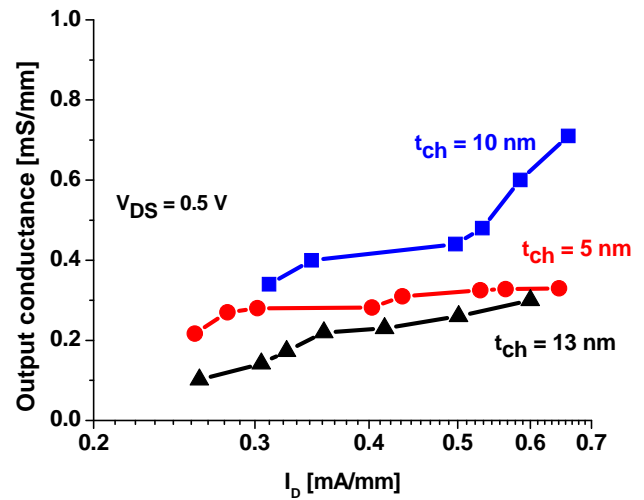
This work was sponsored by Intel Corporation and FCRP-MSD at MIT. Device fabrication took place at the facilities of the Microsystems Technology Laboratories (MTL), the Scanning Electron Beam Lithography (SEBL) and the Nano-Structures Laboratory (NSL) at MIT.



**Fig. 9** Effective source resistance  $R_s^*$  as a function of  $L_g$  obtained through the gate current injection technique.



**Fig. 10** Microwave characteristics of both types of 40 nm InAs HEMTs with  $t_{ch} = 5$  nm and  $t_{ch} = 10$  nm.



**Fig. 11** Output conductance ( $g_o$ ) characteristics as a function of  $I_D$  for three different  $L_g = 40$  nm devices at  $V_{DS} = 0.5$  V.