Impact of $\langle 110 \rangle$ uniaxial strain on n-channel In_{0.15}Ga_{0.85}As high electron mobility transistors

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This letter reports on a study of the impact of $\langle 110 \rangle$ uniaxial strain on the characteristics of InGaAs high electron mobility transistors (HEMT) by bending GaAs chips up to a strain level of 0.4%. Systematic changes in the threshold voltage and intrinsic transconductance were observed. These changes can be well predicted by Schrödinger–Poisson simulations of the one-dimensional electrostatics of the device that include the piezoelectric effect, Schottky barrier height change, and sub-band quantization change due to strain. The effect of $\langle 110 \rangle$ strain on the device electrostatics emerges as a dominant effect over that of transport in the studied InGaAs HEMTs. © 2009 American Institute of Physics. [doi:10.1063/1.3273028]

As InGaAs field-effect transistors (FETs) are receiving a great deal of attention as a potential post-Si CMOS logic technology,¹⁻⁴ channel strain engineering is being explored as a way to enhance their performance. In fact, recently, strain has been intentionally employed to enhance the electron mobility in InGaAs metal-oxide-semiconductor fieldeffect transistor by regrowing lattice-mismatched source and drain regions.⁵ Mechanical strain is often unintentionally introduced to InGaAs high electron mobility transistors (HEMTs) by various sources, such as lattice mismatch between channel and substrate, passivation dielectrics,⁶ and hydrogen absorption⁷ in the gate stack. The residual strain is found not only to shift the electrical properties of the device but also to impose serious reliability concerns.^{8,9} It is therefore of great importance to understand the fundamental effects of mechanical strain on device performance. This has yet to be done in a rigorous way. In the studies mentioned above, it is hard to exclusively attribute the observed changes in the device characteristics to strain because other physical aspects of the device structure also changed along the way.

In this letter, we report an experimental study of strain effects on InGaAs HEMTs by introducing mechanical strain through chip-bending experiments. Electrical measurements have been performed at different levels of uniaxial strain along the main crystallographic orientations. It is found that strain introduces significant changes to the electrostatics of InGaAs HEMTs that overwhelm any changes that might be introduced to the transport characteristics.

A chip-bending apparatus was fabricated that allows the application of uniaxial tensile or compressive strain to semiconductor chips with size down to $2 \times 4 \text{ mm}^2$. To avoid cracking, the InGaAs FET chips were mounted to a supporting aluminum plate. Devices are wire-bonded to metal pads that connect to a semiconductor parameter analyzer, to exclude any change of probing resistance during the bending experiments. The strain level was calibrated using a laser reflection method (Tencor Flx-2320) and strain gauges. The measurements were verified to be fully reversible when we apply or remove the strain, indicating no strain relaxation of any kind during the experiment.

Experimental n-channel double-heterojunction In_{0.15}Ga_{0.85}As HEMTs on [001] GaAs with 1 μ m long and 50 μ m wide gate were used.¹⁰ The channel direction points along the [$\bar{1}10$] direction. The inset in Fig. 1 shows the device cross section. Both tensile and compressive strain along the two (110) directions were applied to the device. During bending experiments, a complete set of electrical parameters, including transfer characteristics, output characteristics, source/drain resistance, and source-gate Schottky diode characteristics, were obtained by a benign characterization suite. Figure 1 shows an example of the impact of strain on the subthreshold characteristics for different level of strain along the [$\bar{1}10$] direction.

We chose to study the strain dependence of threshold voltage $(V_{\rm T})$ as a proxy for the electrostatics and the intrinsic transconductance $(g_{\rm mi})$ in the linear regime as a proxy for transport. Both $V_{\rm T}$ and $g_{\rm m}$ were determined at low drain-to-source voltage $(V_{\rm DS}=50 \text{ mV})$ to minimize heating effects and parasitic ohmic drops. $V_{\rm T}$ was defined as $V_{\rm GS}$ that yields $I_{\rm D}=1$ mA/mm. The intrinsic transconductance was extracted following the method in Ref. 11. Output conductance was obtained from the output characteristics. The source and



FIG. 1. (Color online) Measured subthreshold characteristics of devices as $[\bar{1}10]$ strain changes. Cross section of the devices is shown in the inset.

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FIG. 2. (Color online) Change of $V_{\rm T}$ as a function of $\langle 110 \rangle$ strain. Data are well explained by the model (dashed lines) that includes the piezoelectric effect and Schottky barrier height change.

drain resistances were extracted using the gate-current-injection method. $^{12} \ensuremath{$

Figure 2 shows the change of threshold voltage (ΔV_T) under both [$\overline{1}10$] and [110] strain. The strain along the two different $\langle 110 \rangle$ directions reverses the sign of ΔV_T . This is the unique signature of the piezoelectric effect, which occurs in polar materials. Particularly, when unequal amount of uniaxial strain along the two $\langle 110 \rangle$ directions is applied to a III-V heterostructure with [001] growth direction, a polarization field (P_z) is generated along the growth direction.⁶ The polarization field is related to the $\langle 110 \rangle$ uniaxial strain by

$$P_{z} = \frac{1}{2}e_{14}(\varepsilon_{[110]} - \varepsilon_{[\bar{1}10]}), \tag{1}$$

where e_{14} is the piezoelectric coefficient, $\varepsilon_{[110]}$ and $\varepsilon_{[\bar{1}10]}$ are the strain along [110] and [$\bar{1}10$], respectively. The polarization field superimposes on the gate-induced electric filed and leads to a $V_{\rm T}$ shift given by

$$\Delta V_{\rm T} = -\int_0^{\rm BC} \frac{P_z(z)}{\varepsilon(z)} dz,$$
(2)

where BC stands for the back channel-barrier interface, z is the distance from a point in the heterostructure to the gate contact along [001] direction, and $\varepsilon(z)$ is the dielectric constant along z.¹³ From Eqs. (1) and (2), it can be seen that alternating uniaxial strain from [$\overline{110}$] to [110] directions reverses the direction of P_z and consequently the sign of $\Delta V_{\rm T}$. The sign of $\Delta V_{\rm T}$ predicted by Eqs. (1) and (2) is consistent with the data in Fig. 2.

Interestingly, Eqs. (1) and (2) also predict that the absolute value of $\Delta V_{\rm T}$ should be the same for the two $\langle 110 \rangle$ directions. However, Fig. 2 shows that $|\Delta V_{\rm T}|$ under [$\bar{1}10$] strain is nearly 3× larger than that under [110] strain. This suggests that there is another mechanism in action here.

Previously, an asymmetric directional dependence was observed in both GaAs metal-semiconductor field-effect transistor (MESFETs) (Ref. 6) and InP HEMTs,⁷ but not fully understood. Asbeck⁶ suspected that in GaAs MESFETs subjected to dielectric passivation stress, this dependence came from spatial distribution of piezoelectric charge under the gate. In the study of hydrogen-induced piezoelectric effect in InGaAs/InP HEMTs, Blanchard⁷ speculated that proton penetration into the semiconductor caused a solid shift of



FIG. 3. (Color online) Change of Schottky barrier height as a function of strain for uniaxial strain parallel and perpendicular to the channel direction $[\bar{1}10]$. The slope of a linear fitting (continuous line) to the data determines the deformation potential (a_c) .

 $\Delta V_{\rm T}$ observed for [110], [110], and [010] directions. However, no clear evidence was further reported of these hypotheses in these two studies.

We postulate that the asymmetric directional dependence of $\Delta V_{\rm T}$ that we observe arises from strain-induced change in the Schottky barrier height ($\phi_{\rm B}$). Figure 3 shows $\Delta \phi_{\rm B}$ extracted using a thermionic-emission model for the I-V characteristics of the gate-source diode. Strain changes $\phi_{\rm B}$ without any directional dependence. This is to be expected. To the first order, $\Delta \phi_{\rm B}$ equals the change of conduction band edge energy of the barrier. This change is nondirectional and is linearly proportional to the hydrostatic component of applied strain.^{14,15} The coefficient, the hydrostatic deformation potential (a_c) , extracted from our measurements is -5.8 eV. This agrees with the recommended value of -6.8 eV in Ref. 16. Since $\Delta \phi_{\rm B}$ directly adds to $\Delta V_{\rm T}$, this nondirectional amount of change superimposes on the directional change due to the piezoelectric effect leading to the overall $\Delta V_{\rm T}$ pattern shown in Fig. 2.

By incorporating the piezoelectric and $\Delta \phi_{\rm B}$ effects into a one-dimensional Schrödinger–Poisson (SP) simulator, the two-dimensional electron gas (2DEG) charge concentration ($n_{\rm s}$) as a function of gate voltage can be calculated. Extracting $V_{\rm T}$ as the gate voltage when $n_{\rm s}$ equals to 10^{11} cm⁻², we found that the experimental data can be well explained by the simulation results (dashed lines in Fig. 2). The piezoelectric constants used in the simulation were e_{14} (GaAs)= -0.16 C/m², e_{14} (AlAs)=-0.225 C/m², and e_{14} (InAs)=-0.044 C/m^{2.15} A linear extrapolation was used for the e_{14} values for AlGaAs and InGaAs.

To investigate the impact of strain on transport, we extracted the linear regime intrinsic transconductance (g_{mi}) by carefully removing the impact of extrinsic resistances. It is important to do so because the extrinsic resistances are also affected by strain. To the first order, a well-extracted linear regime g_{mi} is independent on V_{GS} which we verified. Thus, the effect of strain-induced V_T change can be appropriately separated. Furthermore, we extracted g_{mi} at a certain gate overdrive ($V_{GS}=V_T+0.4$ V) to fully offset the effect of gatefield-induced QW profile change, even though this effect is minor. Figure 4 shows the extracted g_{mi} for both [110] and [$\overline{110}$] strain. Sign reversal and asymmetric Δg_{mi} pattern are seen for the two $\langle 110 \rangle$ directions.

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FIG. 4. (Color online) Relative change of intrinsic transconductance of InGaAs HEMT under $\langle 110 \rangle$ strain. Simulation results that account for the piezoelectric effect and changes in ΔE_c and quantization are shown by dashed lines. The inset shows the model of overall gate capacitance.

Theoretically, the change of $g_{\rm mi}$ consists of a combination of change in gate capacitance ($C_{\rm g}$) and electron mobility ($\mu_{\rm e}$). In the HEMT structure, $C_{\rm g}$ can be modeled as three capacitors connected in series: the insulator capacitor ($C_{\rm ins}$), the centroid capacitor ($C_{\rm cent}$), and the quantum capacitor ($C_{\rm Q}$) (Ref. 17) (inset in Fig. 4). The centroid capacitor comes from the fact that 2DEG in the QW is usually centered at a distance away from the barrier-channel interface. The quantum capacitor originates from the limited density-of-states in semiconductors.

Our SP simulation reveals that C_{cent} is changed significantly by uniaxial strain in a manner that again suggests a dominant role for the piezoelectric effect. This can be explained through the modifications that the strain-induced polarization field imposes on the QW profile. In essence, the centroid of 2DEG moves either closer to or farther from the gate, depending on the direction of the polarization field. In addition, a nondirectional component of ΔC_{cent} arises from the change in band discontinuity (ΔE_c) at the barrier-channel interface and its impact on sub-band quantization. The SP simulation shows that the $\Delta C_{\rm cent}/C_{\rm cent}$ can be as high as -14% with 0.4% strain. The $\Delta C_Q/C_Q$ due to effective mass change¹⁸ is estimated to be in the order of -3.5% with 0.4% strain. The capacitance of C_{ins} is set by the barrier thickness. Considering that C_Q is around 2× larger than C_{cent} in our HEMT, the change of C_{g} is dominated by the change in C_{cent} . SP simulation results of the overall $\Delta C_{\rm g}/C_{\rm g}$ with polarization field incorporated is shown by the dashed lines in Fig. 4. In the SP model, the gate capacitance is determined by the differential increase of n_s over V_g at $V_g = V_T + 0.4$ V. Interestingly, the impact of uniaxial strain on C_{g} nearly fully accounts for all the observed change in $g_{\rm mi}$.

The agreement between model and experiments obtained in Fig. 4 suggests that strain does not affect μ_e significantly. Theoretically, μ_e should increase with tensile strain and decrease with compressive strain due to conduction band warping.¹⁸ This is precisely contrary to what is observed in our experiments in the nondirectional component of Δg_{mi} . Consistent with our experimental results, the reported experimental Hall mobility change for electrons in GaAs due to strain is not significant, the value is in the ±1% range for strain up to -0.4%.¹⁹ Thus, we conclude that the observed Δg_{mi} in our experiments is dominated by the change in C_{cent} . Under higher strain, the change of C_{cent} will tend to saturate as the 2DEG moves close to the QW sidewalls. Also, the mobility in InGaAs under high tensile stress could significantly increase.¹⁸ Under these conditions, it is possible for the strain-induced changes in mobility to dominate the changes in transconductance. In deeply scaled devices, the piezoelectric effect is expected to be mitigated, as the barrier thickness is reduced or the barrier is replaced by nonpiezoelectric dielectrics.

In summary, we have studied uniaxial strain effects on n-type InGaAs HEMTs through chip-bending experiments. We have found that $\langle 110 \rangle$ uniaxial strain affects the electrostatics of InGaAs HEMTs through a combination of piezo-electric effect, Schottky barrier height change, and quantum well profile change. These effects are much more significant than any impact of strain on mobility. Understanding these effects is important for implementing strain engineering in III-V FETs.

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