# Modeling Frequency Response of 65 nm CMOS RF Power Devices

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## ABSTRACT

This paper presents a model for the frequency response of 65 nm RF power CMOS devices as a function of device width. We find that the cut-off frequency ($f_T$) and maximum oscillation frequency ($f_{max}$) decrease with increasing device width. Small-signal equivalent circuit extractions reveal that the main reason for the degradation in $f_T$ and $f_{max}$ is the presence of non-scalable parasitic resistances in the gate and drain of wide devices. Simplified expressions for $f_T$ and $f_{max}$ that include these parasitic effects have been derived and shown to be very accurate.

## I. INTRODUCTION

The remarkable improvement in the frequency response of silicon CMOS devices in recent years has motivated their use in millimeter-wave power applications. Specific applications in the millimeter-wave regime include high capacity wireless LAN, short-range high data-rate wireless personal area networks, and collision avoidance radar for automobiles [1, 2]. Using silicon CMOS for these applications allows for higher levels of integration and lower cost. Also, special circuits for improving efficiency and linearity of power amplifiers can be easily integrated into CMOS.

The main concern with using CMOS at millimeter-wave frequencies is its inability to yield high efficiency power amplifiers with power levels over 10 mW in the 60-80 GHz regime. Previous research in our group on the power performance of 65 nm CMOS has shown that the peak output power drops to below 20 mW at 18 GHz [3]. It was also shown that the output power and peak power-added efficiency are strongly correlated to $f_{max}$ [3]. Hence the decrease in output power at high frequencies can be attributed mainly to a decrease in $f_{max}$ in wide devices.

In this paper, we investigate the reasons for the degradation in $f_{max}$ with device width. We first present measured data for $f_T$ and $f_{max}$ as a function of device width. Small-signal equivalent circuits are then extracted from the measured s-parameters to identify the reason for the degradation in $f_{max}$ of wide devices. Finally, analytical expressions for $f_T$ and $f_{max}$ that include width relevant elements are derived in terms of small-signal parameters.

## II. TECHNOLOGY

The devices used in this study are standard foundry 65 nm CMOS transistors from IBM [4]. Each device consists of $N_C$ identical unit cells, each with 24 fingers ($N_F$) of 2 μm finger width ($W_F$). All devices have a gate length of 50 nm and total gate widths ranging from 96 μm to 16,128 μm. S-parameter measurements from 0.5 GHz to 40 GHz were performed using an Agilent 8510C. Unless otherwise indicated, all s-parameter measurements were done at $V_{DD}$=1 V and a constant drain current density.

## III. MEASUREMENTS

Fig. 1 shows the de-embedded $f_T$ and $f_{max}$ as a function of total device width at $I_D$=25 mA/mm and $I_D$=200 mA/mm. The s-parameter data was de-embedded using on-wafer open and short de-embedding structures that were custom designed for each device. We find that $f_T$ is relatively constant with width for low current densities, but decreases with width at the higher current densities. On the other hand, $f_{max}$ decreases with device width at all widths under both bias conditions, although the decrease is more prominent at higher current densities. At $V_{DD}$=1 V and $I_D$=100 mA/mm, $f_T$ decreases from 142 GHz to 110 GHz and $f_{max}$ decreases from 190 GHz to 90 GHz as the device width is increased from 96 μm to 1536 μm.

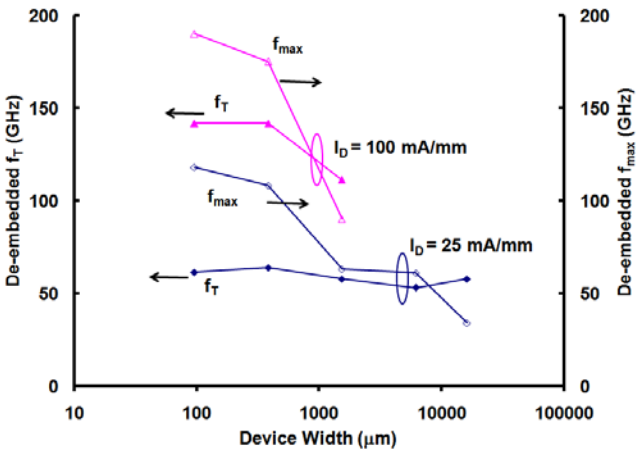


Fig. 1: De-embedded $f_T$ and $f_{max}$, measured at $I_D$=25 mA/mm and at $I_D$=100 mA/mm, as a function of total device width

## IV. SMALL-SIGNAL EQUIVALENT CIRCUIT

To understand the reasons for the degradation of $f_{max}$ in wide devices, we extracted the small-signal equivalent circuit for our devices from s-parameter measurement data. The topology of our model is shown in Fig. 2. The circuit includes parasitic resistances in the gate ($R_G$), source ($R_S$) and drain ($R_D$), transconductance ($g_m$), output resistance ($r_o$), intrinsic gate-source ($C_{gs}$) and gate-drain ($C_{gd}$) capacitances, substrate resistance ($R_{sx}$), and parasitic capacitances from the body to gate ($C_{gb}$), source ($C_{sb}$) and drain ($C_{db}$).

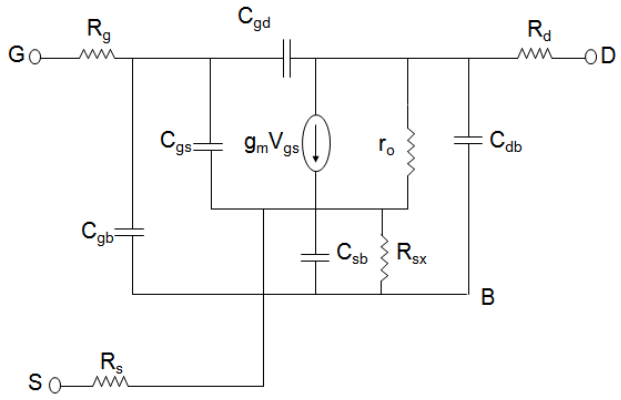


Fig. 2: Small-signal equivalent circuit of a MOSFET including parasitic resistances and the substrate network.

S-parameter measurements from 0.5 to 40 GHz were made on each device at $V_{GS}$=$V_{DS}$=0 V and at $V_{DS}$=1 V, $I_D$=100 mA/mm. The parasitic resistances are extracted from the $V_{GS}$=$V_{DS}$=0 V s-parameter data as [5]:

$$R_G = real(Z_{11} - Z_{12})$$
$$R_S = real(Z_{12})$$
$$R_D = real(Z_{22} - Z_{12})$$

The extracted parasitic resistances are subtracted from the z-parameter data measured at $V_{DS}$=1 V, $I_D$=100 mA/mm to give the intrinsic y-parameters. The rest of the equivalent circuit parameters can then be extracted from the intrinsic y-parameters as [5]:

$$g_m = real(Y_{21}) \qquad C_{gs} = \frac{imag(Y_{11}+Y_{12})}{\omega}$$
$$r_o = \frac{1}{real(Y_{22})} \qquad C_{gd} = -\frac{imag(Y_{12})}{\omega}$$
$$R_{sx} = \frac{real(Y_{22}+Y_{12})}{(imag(Y_{22}+Y_{12}))^2} \qquad C_{db} = C_{sb} = \frac{imag(Y_{22}+Y_{12})}{\omega}$$

The value of $C_{gb}$ can then be determined by fitting the equivalent circuit model to the measured s-parameter data in Agilent ADS.

The equivalent circuit parameters extracted for a device of total width 96 μm (2 unit cells of 48 μm width) at $V_{DS}$=1V, $I_D$=100 mA/mm are as follows:
$R_G$=2.5 Ω, $R_S$=2 Ω, $R_D$=3.25 Ω, $g_m$=0.107 S, $r_o$=83 Ω, $R_{sx}$=75 Ω, $C_{gs}$=56 fF, $C_{gd}$=34 fF, $C_{db}$=$C_{sb}$=120 fF, $C_{gb}$=3.8 fF.

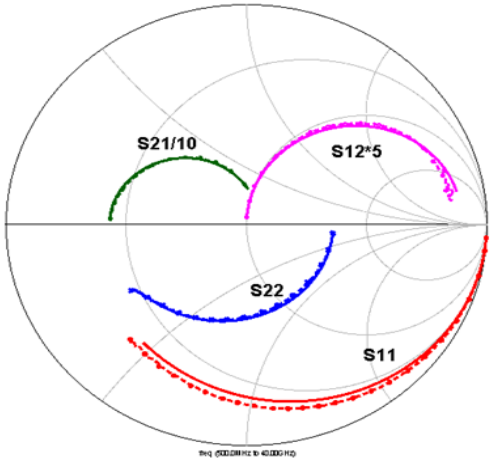


Fig. 3: Measured and Modeled s-parameters at $V_{DD}$=1 V, $I_D$=100 mA/mm. Measured data is in symbols and the model is the solid line. W=2x48 μm.

Fig. 3 shows the comparison of measured and modeled s-parameters at $V_{DS}$=1 V, $I_D$=100 mA/mm for the 96 μm wide device. The model shows excellent agreement with the measured data over the entire frequency range.

Fig. 4 plots the modeled and measured short-circuit current gain ($h_{21}$) and the unilateral power gain (U) for the same device. It is clear that the model does an admirable job at predicting not only the $f_T$ and $f_{max}$ of the device, but also $h_{21}$ and U over the entire frequency range.

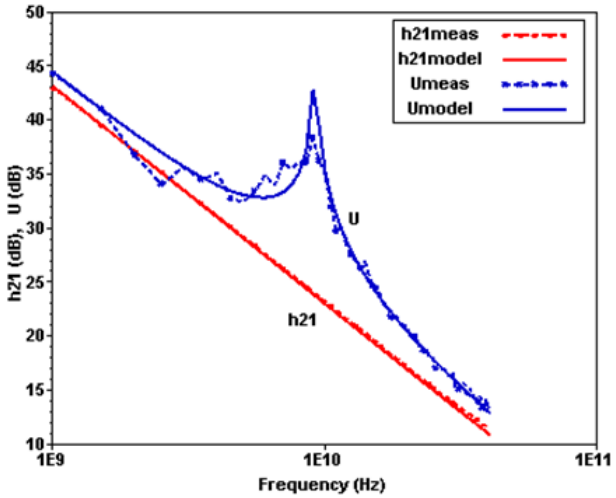


Fig. 4: Short circuit current gain and unilateral power gain as a function of frequency. W=2x48 μm, $V_{DD}$=1 V, $I_D$=100 mA/mm

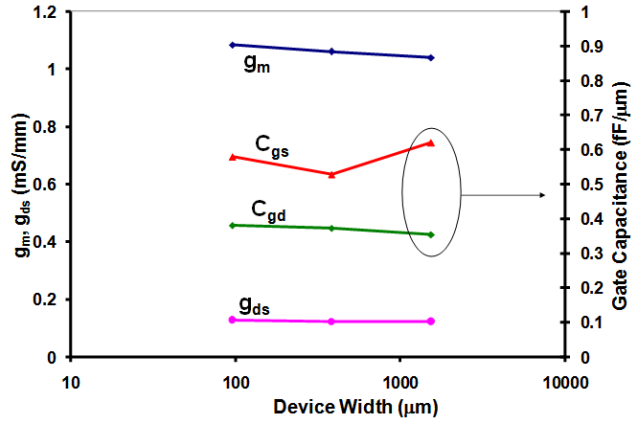


Fig. 5: Normalized intrinsic parameters ($g_m$, $g_{ds}$, $C_{gs}$, $C_{gd}$) as a function of device width. $V_{DD}$=1 V, $I_D$=100 mA/mm.

Small-signal equivalent circuit parameters were extracted for devices with total width ranging from 96 µm to 1536 µm. The $g_m$, $g_{ds}$, $C_{gs}$ and $C_{gd}$, normalized to device width, are shown as a function of device width in Fig. 5. All these extracted intrinsic parameters are relatively constant with device width.

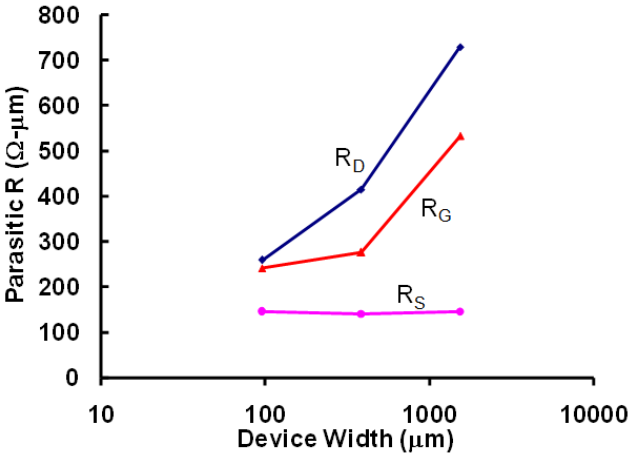


Fig. 6: Normalized parasitic resistances vs. device width. Parasitic resistances are extracted from s-parameters measured at $V_{DD}$=1 V, $I_D$=100 mA/mm.

Fig. 6 shows the normalized parasitic resistances across device width. $R_S$ is constant across width, but $R_G$ and $R_D$ increase with increasing width. Normalized $R_G$ increases by 120% and normalized $R_D$ increases by 180% as the device width is increased from 96 um to 1536 um. As mentioned before, the device width in our transistors is increased by wiring multiple unit cells in parallel. Thus, it makes sense that the parasitic gate and drain resistances are higher in the wide devices because of the additional wiring required to connect the unit cells in parallel.

To examine the effect of the various small-signal parameters on $f_T$ and $f_{max}$, a sensitivity analysis was carried out in ADS. The results are shown in Table 1. It is clear that $f_T$ shows no dependence on $R_G$ and a small dependence on $R_D$ (13% decrease in $f_T$ for a 100% increase in $R_D$). However, $f_{max}$ shows a much stronger dependence on both $R_G$ and $R_D$ (24% degrade in $f_{max}$ with 100% increase in either $R_G$ or $R_D$). Also note that $f_T$ and $f_{max}$ are relatively insensitive (less than 5% change) to the substrate parameters, $R_{sx}$, $C_{db}$, $C_{sb}$, and $C_{gb}$.

| | $f_T$ | % change in $f_T$ | $f_{max}$ | % change in $f_{max}$ |
|---|---|---|---|---|
| Measured | 142 | | 190 | |
| Modeled | 142 | | 179.5 | |
| 2x $R_G$ | 142 | 0 | 136.5 | -24 |
| 2x $R_D$ | 124 | -12.7 | 135 | -24.8 |
| 2x $R_S$ | 132 | -7 | 195 | 8.6 |
| 0.5x $g_m$ | 79 | -44.4 | 115 | -35.9 |
| 0.5x $r_o$ | 135.5 | -4.6 | 158.5 | -11.7 |
| 2x $C_{gs}$ | 95.5 | -32.7 | 151 | -15.9 |
| 2x $C_{gd}$ | 99 | -30.3 | 98.5 | -45.1 |
| 2x $R_{sx}$ | 143 | 0.7 | 178.5 | -0.6 |
| 2x $C_{sb}$ | 143.5 | 1.1 | 179.5 | 0 |
| 2x $C_{db}$ | 140.5 | -1.1 | 169.5 | -5.6 |
| 2x $C_{gb}$ | 137 | -3.5 | 178 | -0.8 |

Table 1: Sensitivity of $f_T$ and $f_{max}$ to the various small-signal equivalent circuit parameters. W=96 µm, $V_{DD}$=1 V, $I_D$=100 mA/mm.

When the values of $R_G$ and $R_D$ alone are increased (according to the values in Fig. 6) keeping all other parameters constant, the modeled $f_T$ decreases from 142 GHz to 112 GHz while the modeled $f_{max}$ decreases from 180 GHz to 95 GHz. In Fig. 1 we showed that the measured $f_T$ decreases from 142 GHz to 110 GHz and measured $f_{max}$ decreases from 190 GHz to 90 GHz as the device width increases from 96 µm to 1536 µm. Hence it can be concluded that the main reason for the degradation in $f_T$ for the wide devices is an increase in parasitic $R_D$ and the reason for degradation in $f_{max}$ is the increase in parasitic $R_G$ and $R_D$. The degradation in $f_{max}$ leads to a corresponding decrease in the output power and PAE in the wide devices.

## IV. ANALYTICAL MODEL FOR $f_T$ and $f_{max}$

A complete y-parameter analysis of the small-signal equivalent circuit shown in Fig. 2 was carried out in an effort to obtain simple analytical expressions for $f_T$ and $f_{max}$ that correctly account for the width scaling of the relevant elements. The substrate parameters, $R_{sx}$, $C_{db}$, $C_{sb}$, and $C_{gb}$ were not considered in this analysis because they have negligible impact on $f_T$ or $f_{max}$ (Table 1).

In the absence of these elements, and ignoring $\omega^2$ and higher order terms, the y-parameters can be approximated by:

$$Y_{11} \approx \frac{j\omega C_{gs}(1+g_{ds}(R_D+R_S))+j\omega C_{gd}(1+(g_m+g_{ds})(R_D+R_S))}{D}$$

$$Y_{12} \approx \frac{-j\omega C_{gs}(g_{ds}R_S)-j\omega C_{gd}(1+(g_m+g_{ds})R_S)}{D}$$

$$Y_{21} \approx \frac{g_m-j\omega C_{gs}(g_{ds}R_S)-j\omega C_{gd}(1+(g_m+g_{ds})R_S)}{D}$$

$$Y_{22} \approx \frac{g_{ds}+j\omega C_{gs}(g_{ds}(R_G+R_S))+j\omega C_{gd}(1+(g_m+g_{ds})(R_G+R_S))}{D}$$

*where*

$$D = 1+g_m R_S+g_{ds}(R_D+R_S+R_G R_S+R_G R_D+R_D R_S)+j\omega C_{gs}(R_G+R_S+g_{ds}(R_G R_S+R_G R_D+R_D R_S))+j\omega C_{gd}(R_G+R_D+g_{ds}(R_G R_S+R_G R_D+R_D R_S))$$

The short-circuit current gain, $h_{21}$, and the unilateral gain, U, can be expressed in terms of y-parameters as

$$h_{21} = \frac{Y_{21}}{Y_{12}}$$

$$U = \frac{|Y_{12}-Y_{21}|^2}{4[\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22})-\mathrm{Re}(Y_{12})\mathrm{Re}(Y_{21})]}$$

Approximate expressions for $f_T$ [6] and $f_{max}$ can be then be derived as

$$f_T \approx \frac{g_m}{2\pi\left[C_{gs}(1+\frac{R_D+R_S}{r_o})+C_{gd}(1+(R_D+R_S)(g_m+\frac{1}{r_o}))\right]}$$

$$f_{max} \approx \frac{g_m\sqrt{1+g_m R_S+g_{ds}(R_D+R_S)}}{4\pi[C_{gs}^2(R_G+R_S)g_{ds}(1+g_m R_S)+C_{gd}^2((R_G+R_D)(g_m+g_{ds})+(g_m+g_{ds})^2(2R_G R_S+R_G R_D+2R_S R_D))+C_{gs}C_{gd}(R_G(g_m+2g_{ds})+g_m g_{ds}(5R_G R_S+3R_G R_D+2R_S R_D)+g_m^2 R_G R_S)]}$$

The above expressions allow technologists and circuit designers to easily determine the frequency metrics for a given device design. The traditional derivations for U and $f_{max}$ [7] only consider the effect of $R_G$. We have also included the effect of $R_S$ and $R_D$ to improve the accuracy of the calculated $f_T$ and $f_{max}$.

Fig. 7 shows the measured data for $f_T$ and $f_{max}$ along with the values calculated using the above expressions. The calculated values show excellent agreement with the measured data over the entire range of device widths studied in this work.

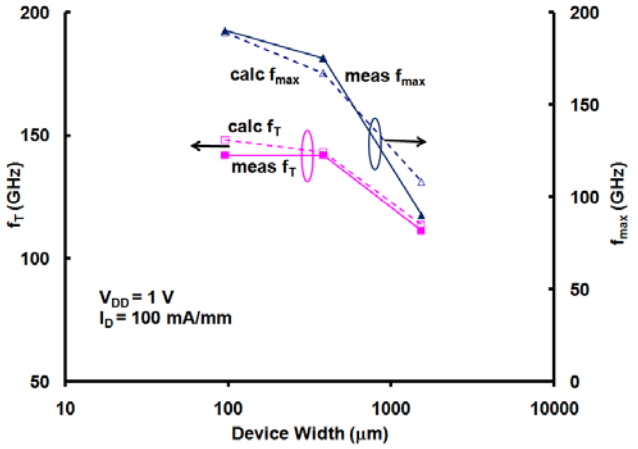


Fig. 7: Measured and calculated $f_T$ and $f_{max}$ as a function of device width. Measured data in solid symbols and lines and calculated data in open symbols and dashed lines.

## V. CONCLUSION

We have studied the frequency response of 65 nm CMOS devices. We find that, at $V_{DD}$=1 V and $I_D$=100 mA/mm, $f_T$ decreases from 140 GHz to 110 GHz and $f_{max}$ decreases from 190 GHz to 90 GHz as the device width is increased from 96 μm to 1536 μm. Small-signal equivalent circuit parameter extractions across device width show that the main reason for $f_T$ and $f_{max}$ degradation is the increase in parasitic gate and drain resistances with width because of the presence of non-scalable parasitics in wide devices. Thus, the key to enabling CMOS for millimeter-wave applications is a parasitic-aware approach when designing wide devices.

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