III-V's: From THz to CMOS

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CMOS scaling is the cornerstone of the electronics and information revolution. The increasing difficulty in extracting more performance out of scaled Si CMOS threatens to bring Moore's Law to a halt. At its heart, the problem is the increasing relative parasitic capacitance of the transistor as it scales down in size coupled with an insufficient additional current capable of driving it. In recent years, the use of increasing amounts of mechanical strain has extended the life of Si. The benefits of strain appear to have been exhausted. Further progress requires the use of a new channel material with much improved transport properties. This is where III-Vs come in.

III-Vs are known for their unique suitability for high frequency communications applications. III-V-based ICs have been inserted in many mission-critical systems where they perform with excellent reliability. The potential of III-Vs for logic has become evident in the last few years. The High-Electron Mobility Transistor (HEMT), in itself a device with THz potential, has revealed excellent logic characteristics down to very small dimensions. III-V MOSFETs utilizing high-K gate dielectrics have been demonstrated and they exhibit promising characteristics.

This talk will summarize recent progress at MIT in our quest to map out the potential of III-V compound semiconductors for logic and identify issues of relevance to future III-V logic MOSFETs. In our research, the HEMT has become an invaluable "model device." The HEMT is in its own right a FET with a "medium-k" gate barrier and outstanding transport characteristics. Due to gate leakage current, the HEMT is not expected to scale down to the dimensions that are required in future logic. Nevertheless, the HEMT constitutes an excellent test bed to study design concepts and device physics of relevance to any future III-V transistor design. In addition, the HEMT is a model device that allows us to start developing and calibrating today the device simulators that will be required in the future.

In this effort, we have developed a low-parasitic InAlAs/InGaAs HEMT technology with gate lengths down to 30 nm. This has enabled us to carry out a scaling study where we have examined the role of four dimensions that are critical to high-frequency and logic performance: gate length, barrier thickness, channel thickness, and side recess length. Out of this, a harmonious device design has emerged with low parasitics and very high electrostatic integrity at the 30 nm gate length regime based on a 10 nm thick channel containing a pure InAs subchannel. We have demonstrated transistors with a record f_T of 628 GHz, and enhancement-mode devices with a combination of f_T and f_{max} in excess of 600 GHz operating at 0.5 V. In addition, the logic characteristics of 30 nm InGaAs HEMTs, in terms of intrinsic delay and short-channel effects, rival those obtained on state-of-the-art Si MOSFETs of equivalent gate lengths. Underlying the potential of InGaAs as a channel material is our extraction of the electron injection velocity at the virtual source in our devices. Values in excess of $3x10^7$ cm/s are obtained for 30-40 nm gate length devices operating at V_{DS}=0.5 V. This is twice as high as strained Si and well in excess of the requirements of the International Technology Roadmap for Semiconductors for the 15 nm node.

A future logic III-V device will require the use of a high-K gate dielectric with very low leakage. Developing this is one of the great challenges ahead of us. These challenges will be summarized in this talk and device architecture options for a future III-V CMOS will be discussed.

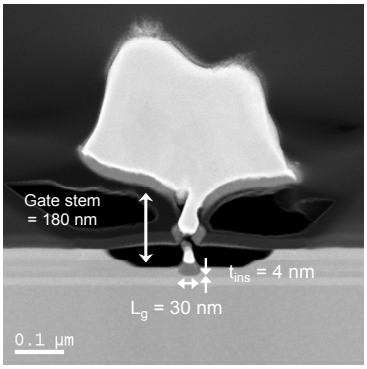

Fig. 1: TEM cross section of 30 nm InAlAs/InGaAs HEMT fabricated by two-step recess and Pt drive-in. The channel includes a 5 nm pure InAs subchannel.

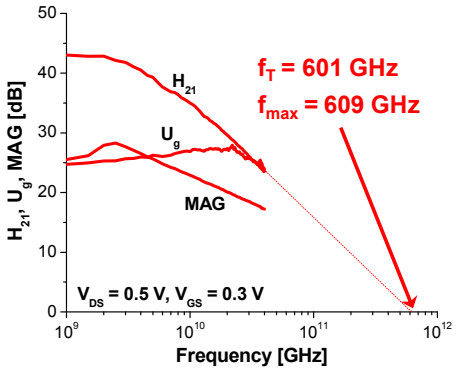

Fig. 2: f_T and f_{max} of 30 nm InGaAs HEMT. This is the first report of a transistor that exhibits both f_t and f_{max} in excess of 600 GHz. Both are obtained at the same bias point.

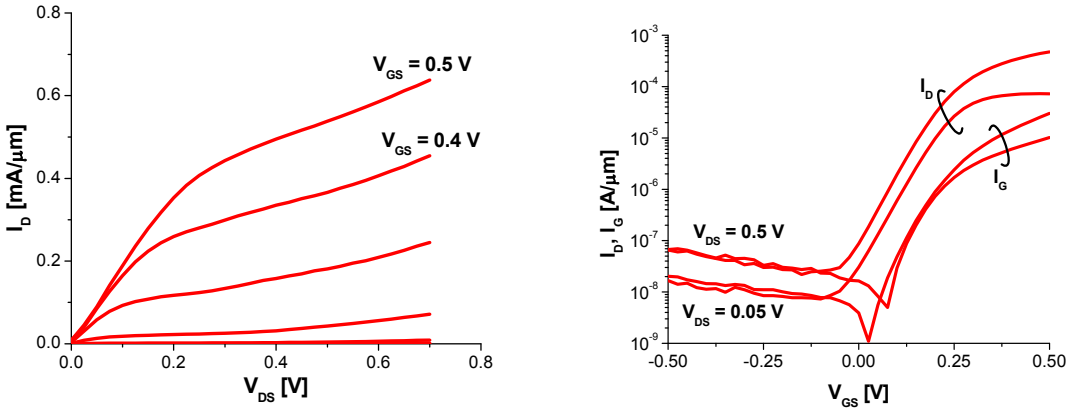

Fig. 3: Output characteristics (left) and subthreshold characteristics (right) of enhancement-mode 30 nm InGaAs HEMT by Pt drive in.

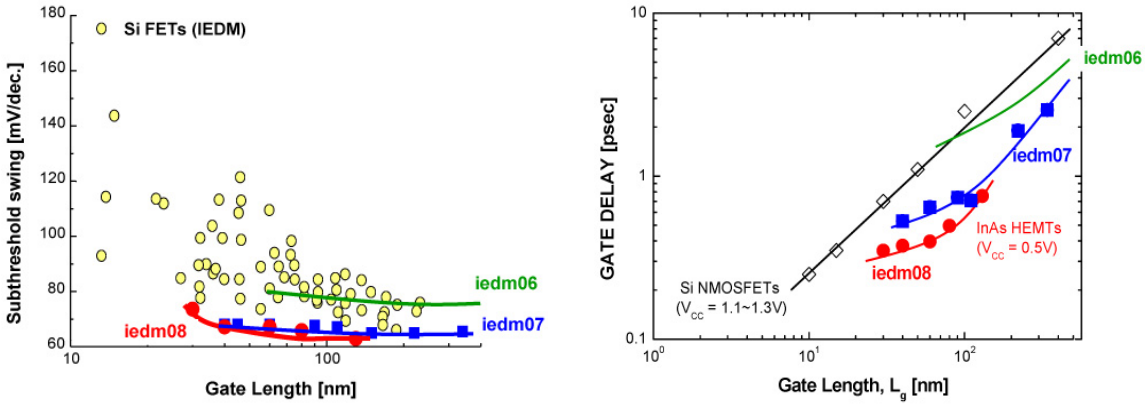

Fig. 4 Benchmarking of three generations of InGaAs HEMTs made at MIT against state-of-the-art Si MOSFETs. On the left is subthreshold swing as a measure of short-channel effects. On the right is intrinsic gate delay as a measure of logic performance. The references refer to the work of the authors presented at the International Electron Devices Meeting in the last few years.