RF Power Performance of an LDMOSFET on High-Resistivity SOI

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***Abstract*—This paper describes the RF power performance of an LDMOSFET technology on high-resistivity silicon-on-insulator wafers. The technology has an on-state breakdown voltage of greater than 10 V, and an off-state breakdown voltage of greater than 20 V. This device technology is shown to have excellent RF power characteristics at frequencies from 1.9 to 5.8 GHz. At 1.9 GHz, a peak power-added efficiency (PAE) of 63% was achieved with an output power of up to 520 mW from a single RF power cell. At 5.8 GHz, a peak PAE of 35% was achieved with an output power of up to 125 mW from a single RF power cell.**

***Index Terms*—LDMOSFET, RF power amplifier, silicon-on-insulator (SOI).**

I. Introduction

THIN-FILM silicon-on-insulator (SOI) is a promising technology platform for highly integrated, high-performance RF circuits. It has several advantages over bulk silicon for these applications; perhaps most importantly it enables the use of a high resistivity silicon substrate. High resistivity ($> 1\,\mathrm{k}{-}\Omega{\cdot}\mathrm{cm}$) silicon reduces substrate RF power loss, conferring considerable benefits to the active and passive elements of an RF system [1]. High resistivity bulk silicon offers the same RF performance advantages as high resistivity SOI, but is believed to pose reliability and yield problems [2], [3]. Thin-film SOI fabricated with a standard Czochralski top silicon and a high-resistivity handle wafer enables the combination of high performance RF circuits with digital logic and memory on the same chip. This solution gains the advantages of the high resistivity substrate for the RF sections without incurring potential reliability or yield problems with the digital sections.

LDMOSFETs on thin-film high-resistivity SOI are promising for highly integrated RF power amplifier applications. Potential uses are wide ranging; they include cellular telephones, wireless LANs, fixed wireless applications, and the radiation hardened applications for which SOI has well known advantages. Prior work has demonstrated the capability of RF LDMOSFETs on high-resistivity SOI to operate with excellent performance at frequencies up to 5.8 GHz [4]. However, that work has a few limitations. First, the demonstrated output power was limited: The previous output power limit for SOI is less than 150 mW.

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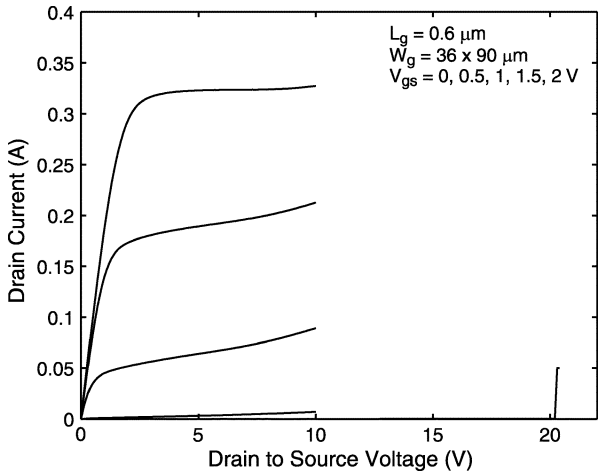

Fig. 1. Output characteristics of an RF power LDMOSFET cell on high resistivity SOI. The on-state breakdown voltage of the cell is greater than 10 V and the off-state breakdown voltage of the cell is greater than 20 V.

Second, the previous work in [4] achieved a high f_t range by utilizing a scaled gate length, a thin gate oxide, and a short drift region, all of which reduce the breakdown voltage. This limits output power and hurts amplifier reliability and robustness. In this letter, we describe an RF power LDMOSFET on high resistivity SOI with high breakdown voltage, high efficiency, output power levels unprecedented for SOI, and operating at frequencies up to 5.8 GHz.

II. Device Fabrication

The fabrication process of the devices in this letter was described in [5] and [6]. These devices were made on bonded SOI wafers with a 160-nm top silicon thickness and a 360-nm buried oxide thickness. The top layer was Czochralski silicon with a resistivity of 10–20 $\Omega \cdot$ cm, and the handle wafer was float-zone silicon with a resistivity of 2000 $\Omega \cdot$ cm. An under source body contact was used to connect the body to the source, preventing turn on of the parasitic source/body/drain bipolar transistor, and enabling high breakdown voltage [7]. The gate length was 0.6 μm, the drift region length was 0.5 μm, and the gate oxide thickness was 20 nm. A metal/polysilicon Damascene gate with a gate sheet resistance of 0.2 Ω/sq [5] was used to provide the low gate resistance required for the large gate finger widths necessary for high output power levels.

III. Results and Discussion

The dc output characteristics of a single RF power cell are shown in Fig. 1. The cell has 36 fingers with a 90-μm gate

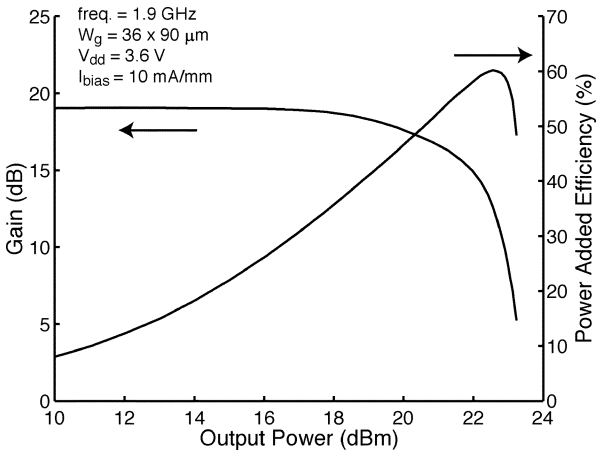

Fig. 2. Load–pull characteristics of a 36×90 μm RF power cell at 1.9 GHz. Input and output matching networks were set to maximize the PAE. The measurements were done using an ATN load-pull system.

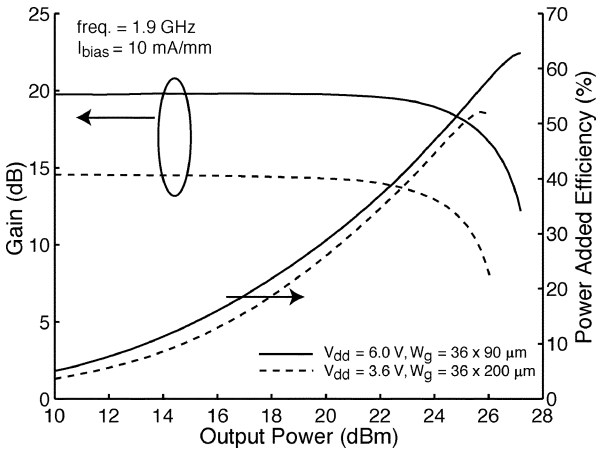

Fig. 3. Output power of an RF power cell can be increased by increasing the supply voltage or increasing the finger width. Using a 90-μm finger width and increasing the supply voltage to 6 V raises the output power for a single cell to 520 mW, and also increases both the peak PAE and small-signal gain. Using a 3.6-V power supply and increasing the finger width to 200 μm raises the output power to 370 mW, but decreases the peak PAE and the small-signal gain.

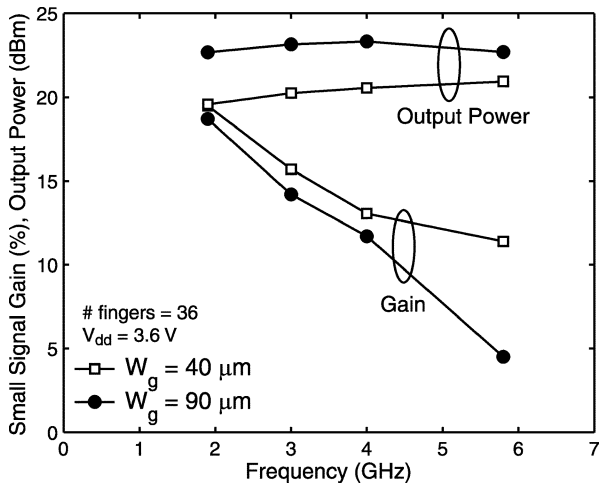

Fig. 4. Use of 40-μm fingers decreases the output power (as compared to the use of 90-μm fingers), but increases the small-signal gain, especially at frequencies greater than 4 GHz. In these measurements, the bias current density was between 10 and 50 mA/mm, and was set at each frequency to maximize PAE.

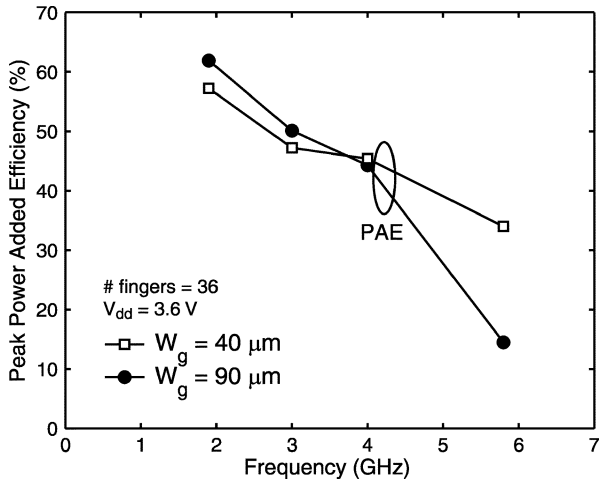

Fig. 5. Finger width of the RF power cell can be optimized for operation at frequencies between 1.9 and 5.8 GHz. The 90-μm fingers produce the highest peak PAE below 4 GHz, but 40-μm fingers are better at 5.8 GHz.

finger width for a 3.2-mm total gate width. On-state breakdown is greater than 10 V and off-state breakdown voltage is greater than 20 V.

This device technology exhibits excellent nonlinear and linear RF power performance. The on-wafer RF power characteristics of a 36×90 μm RF power cell are shown in Fig. 2 at a supply voltage of 3.6 V and a frequency of 1.9 GHz. The bias current was 10 mA/mm and the input and output matching networks were set to maximize PAE. Under these conditions, the RF power cell had a small-signal gain of 18 dB, a peak PAE of 60% and an output power at a peak PAE of 180 mW. When matched to simultaneously achieve high PAE and also high linearity, the same RF power cell had a PAE of 35% at an ACPR (using the W-CDMA 3GPP specification) of -38 dBc and 50 mW of output power at $V_{\rm dd} = 3.6$ V.

This device technology can produce greater output power levels by using a higher supply voltage or through optimization of the RF power cell layout. As shown in Fig. 3, increasing the supply voltage to 6 V raises the output power to 520 mW and increases the small-signal gain to 19.5 dB and the peak PAE to 63%. Increasing the gate finger width to 200 μm increases the output power to 370 mW at $V_{\rm dd} = 3.6$V. However, the small-signal gain is reduced to 15 dB by the increased gate resistance of the longer gate fingers, and therefore the peak PAE is decreased to 52%.

Figs. 4 and 5 demonstrate that this device technology is suitable for use at frequencies between 1.9 and 5.8 GHz, and that the correct selection of the gate finger width is necessary to achieve optimum performance at a particular frequency. These figures show the small-signal gain, output power, and peak PAE versus frequency for RF power cells with 36 fingers and a finger width of 40 or 90 μm. The input power level and input and output matching networks were set for maximum PAE at each measurement point. At all frequencies, the gain of the cell with 40 μm fingers is greater because the gate resistance is lower, while the

output power of the cell with 90 μm fingers is higher because it drives more current. The PAE of the cell with 90 μm fingers is superior at frequencies below 4 GHz because the gate and drain measurement pads have less of an impact on the larger width cell. However, the PAE of the 90 μm finger cell drops precipitously above 4 GHz due to higher gate resistance and greatly lower gain. Therefore the PAE of the cell with narrower fingers is superior above 4 GHz. The use of 40 μm fingers extends the frequency range of the technology to 5.8 GHz, where it has a 11 dB small signal gain, a 35% peak PAE, and an output power of 125 mW.

IV. Conclusion

This letter describes the RF power characteristics of an LDMOSFET technology on high-resistivity SOI. At 1.9 GHz and $V_{\rm dd} = 3.6$ V, a peak PAE of 63% was achieved with an output power level of 180 mW from a single RF power cell. Using wide fingers or increased supply voltage enables higher output power: 520 mW was demonstrated from a single cell. The use of narrow fingers extends the frequency limit of the technology to 5.8 GHz. At this frequency, output power of 125 mW at a peak PAE of 35% was achieved. This letter demonstrates the feasibility of high-resistivity SOI for future highly integrated RF power systems at 5 GHz and beyond.

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