Si CMOS
for RF Power Applications

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MIT

Workshop on Advanced Technologies for Next Generation of RFIC
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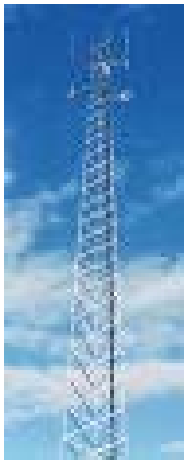
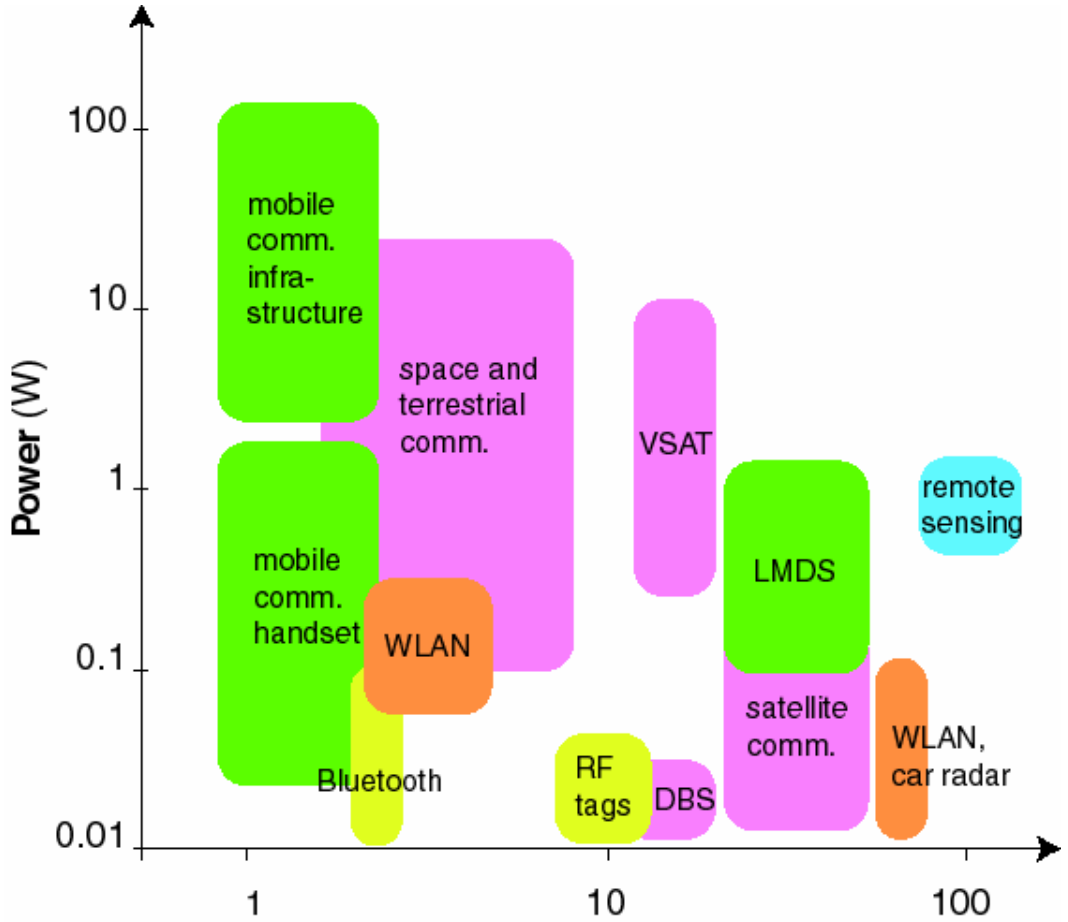
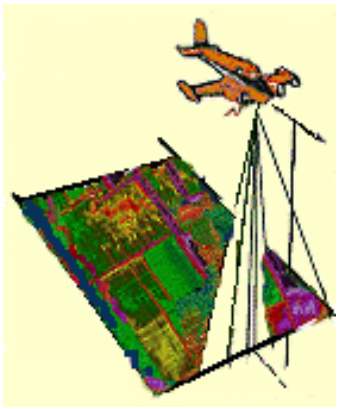
Sponsors: DARPA, IBM, SRC

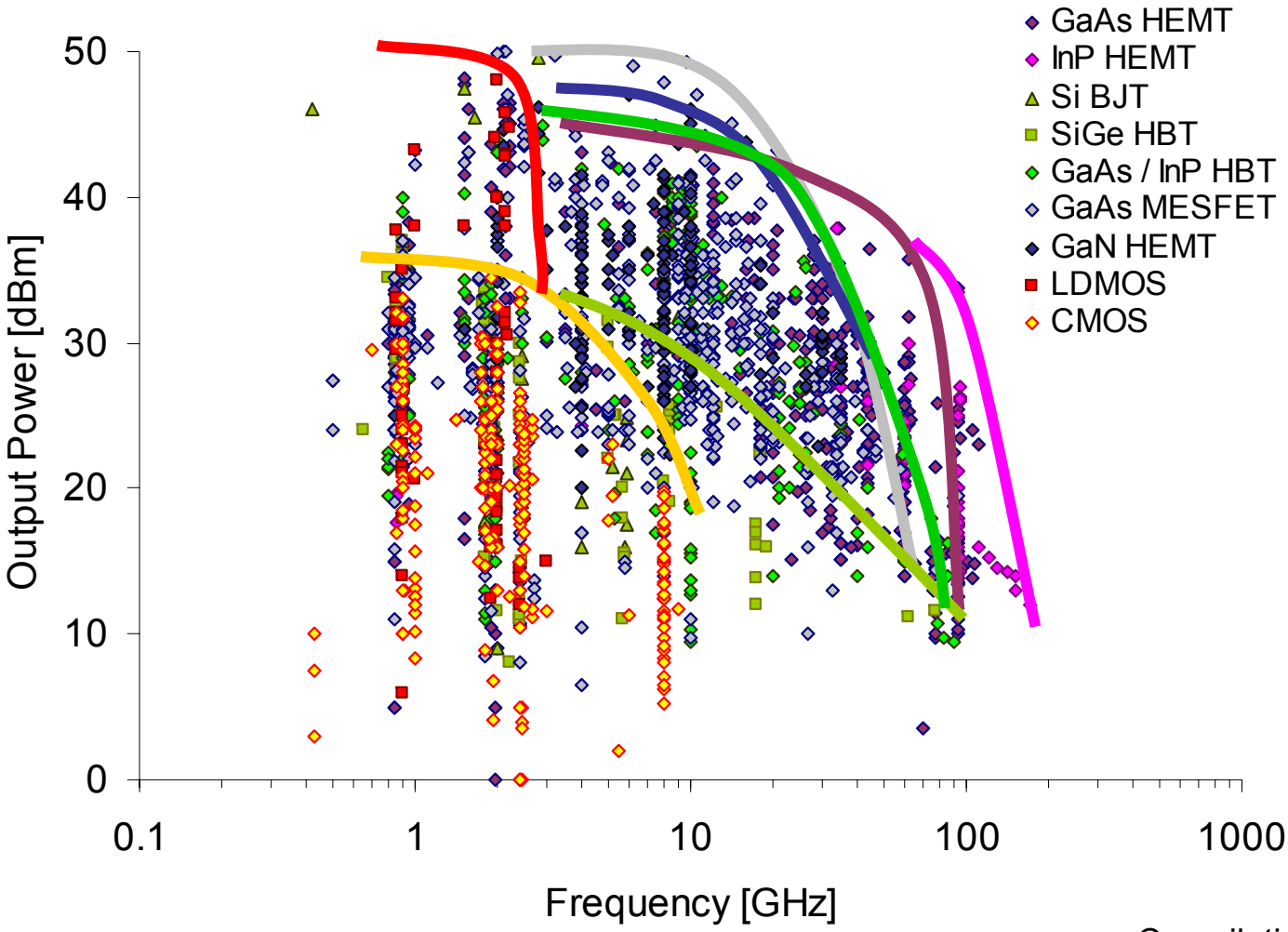
RF power applications





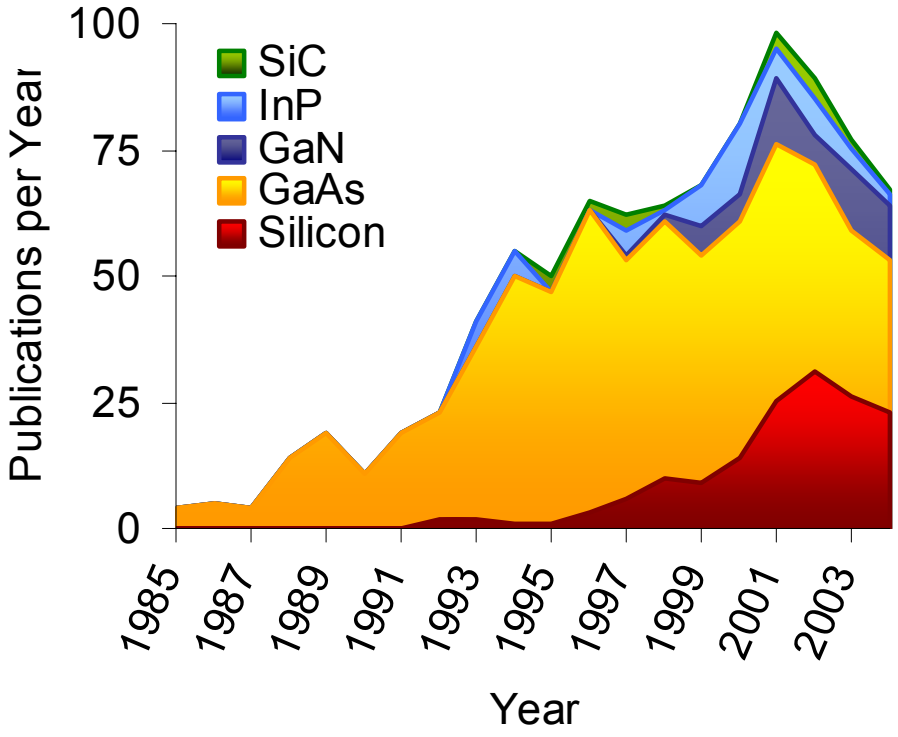


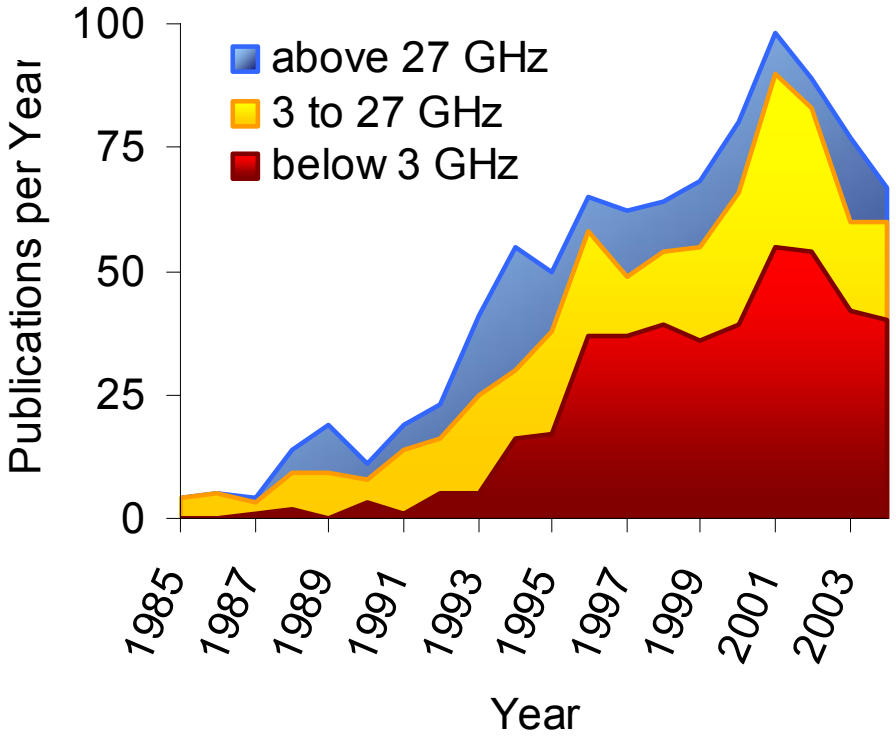
Power vs. frequency



Compilation of research papers from IEEE Xplore by J. Scholvin

Research activity by material and frequency





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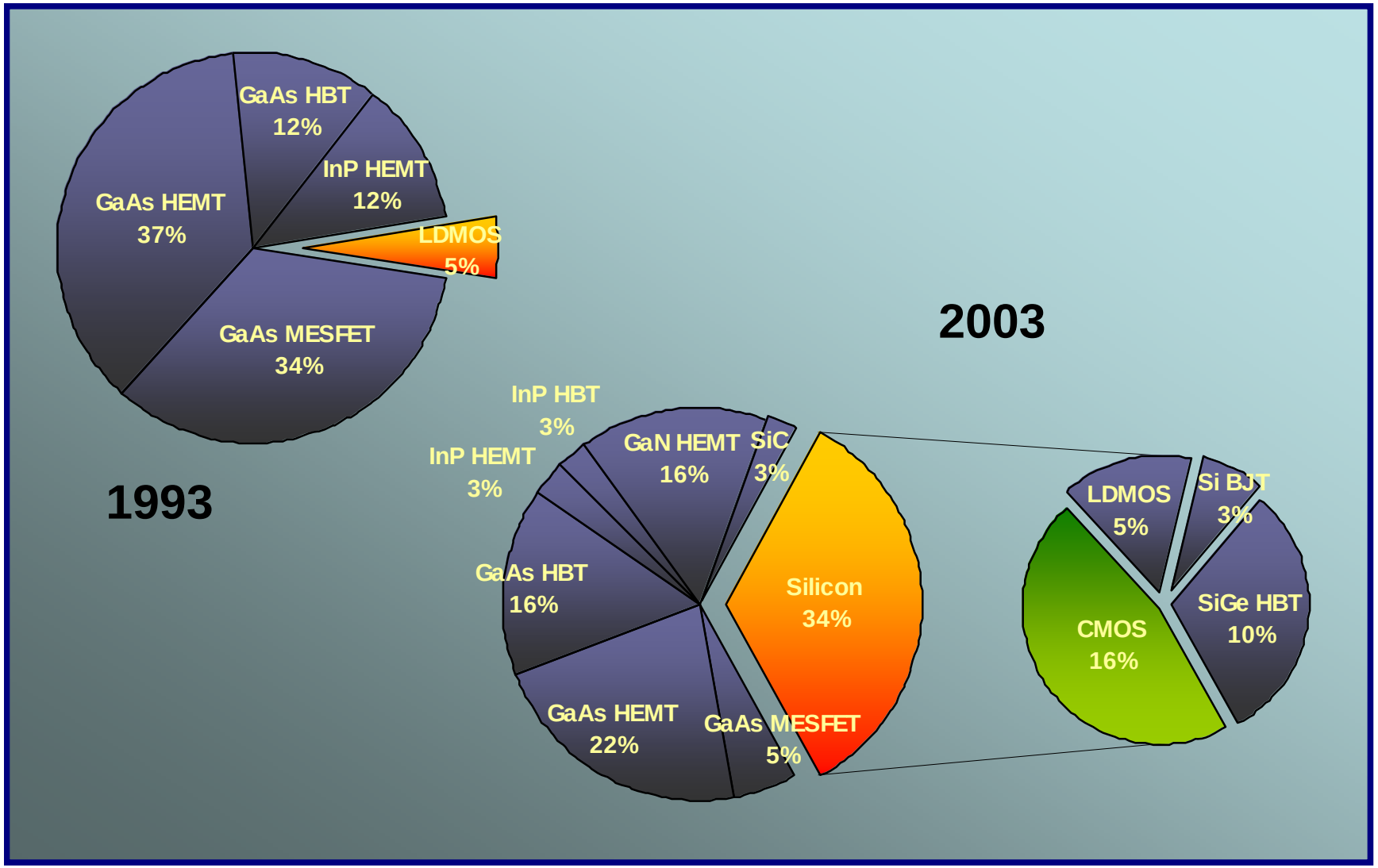
RF power technologies: 1993 vs. 2003



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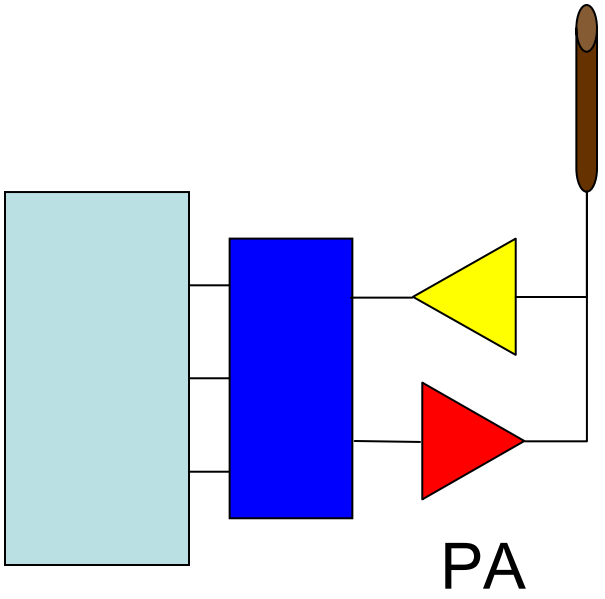
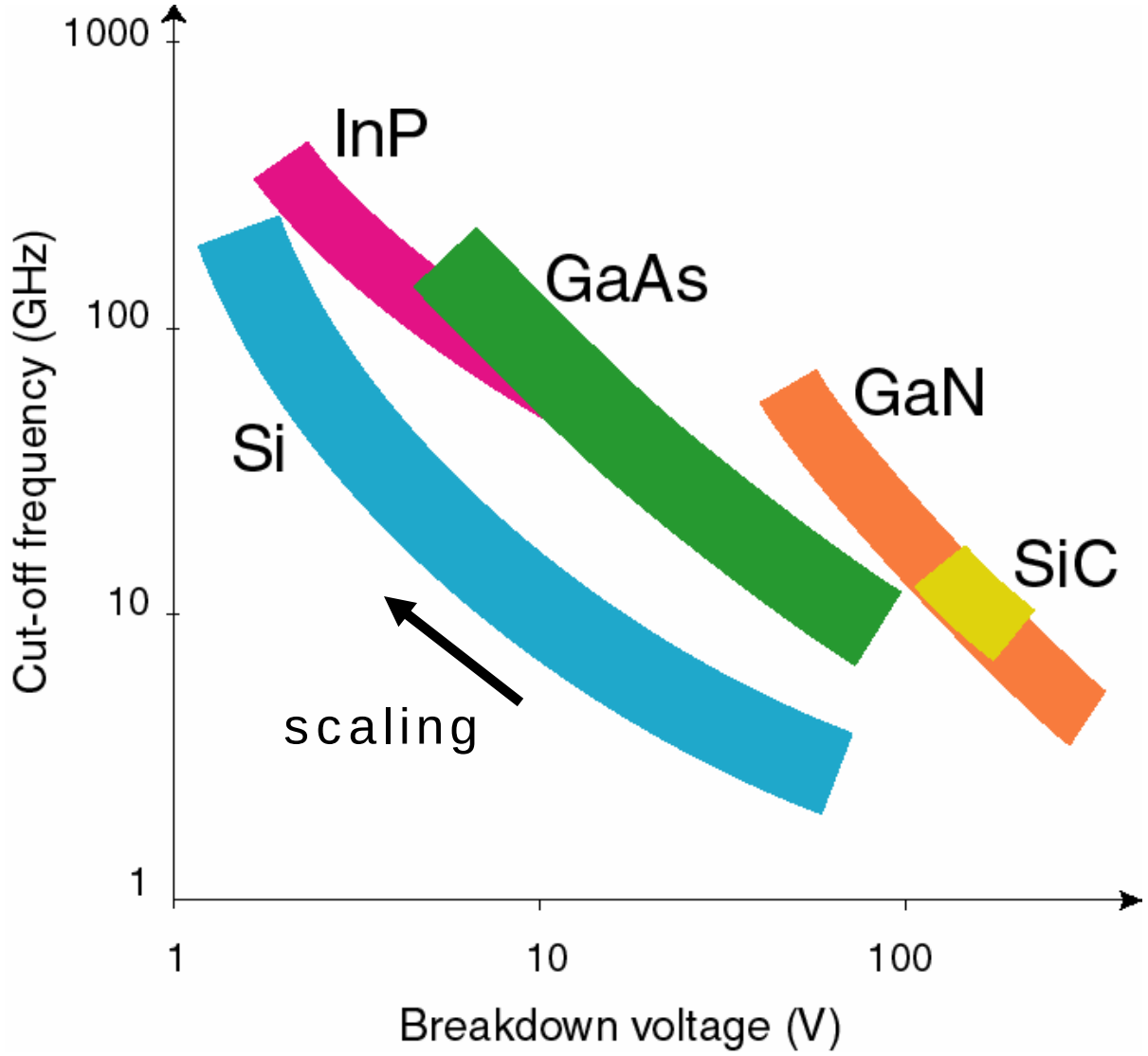
RF Power Figures of Merit

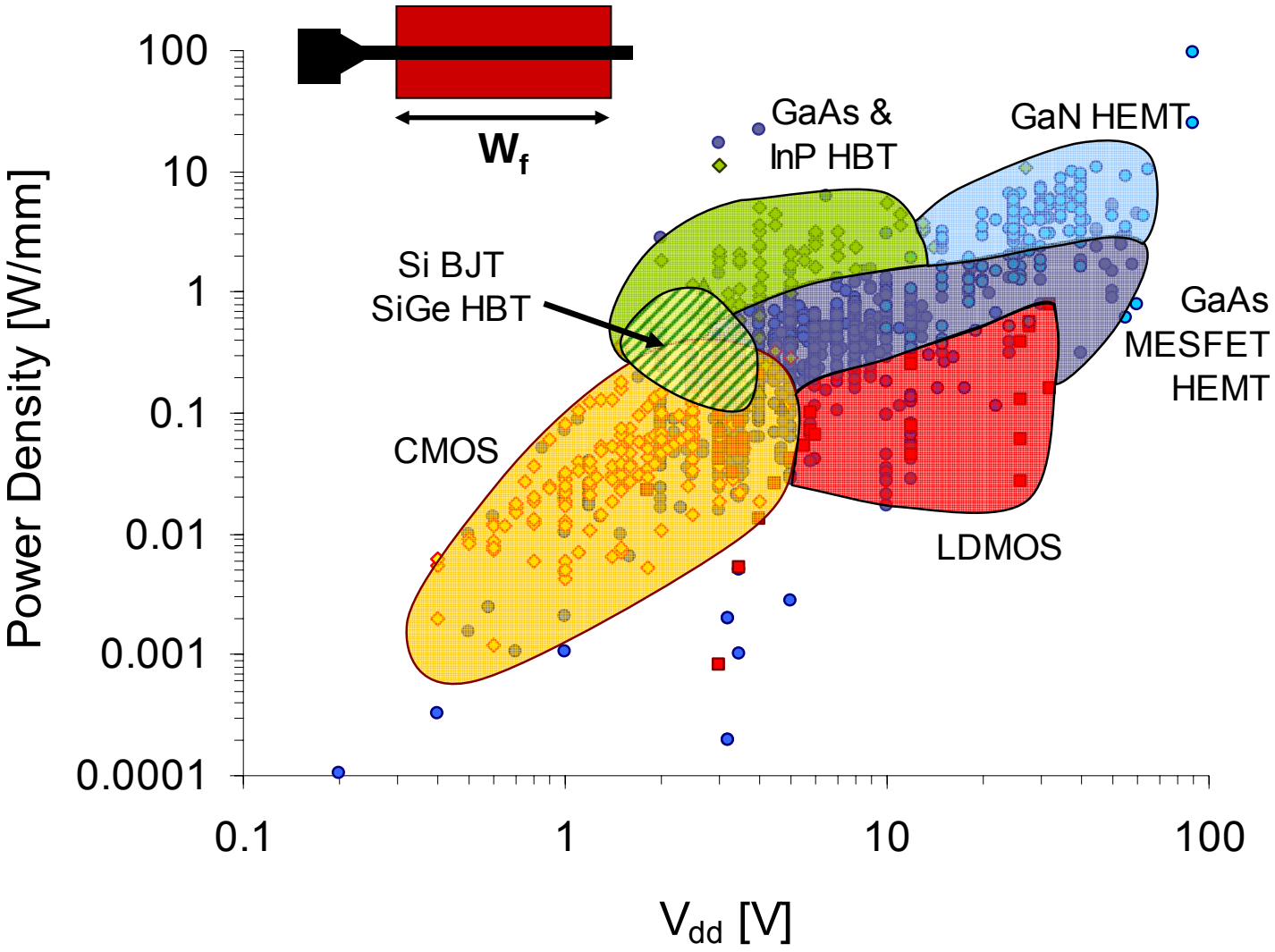


- PA specs:
  - Frequency
  - Power
  - Gain
  - Linearity
  - Voltage
  - Reliability
  - Power efficiency
  - Cost

Fundamental trade-off between voltage and frequency



Key to power: supply voltage



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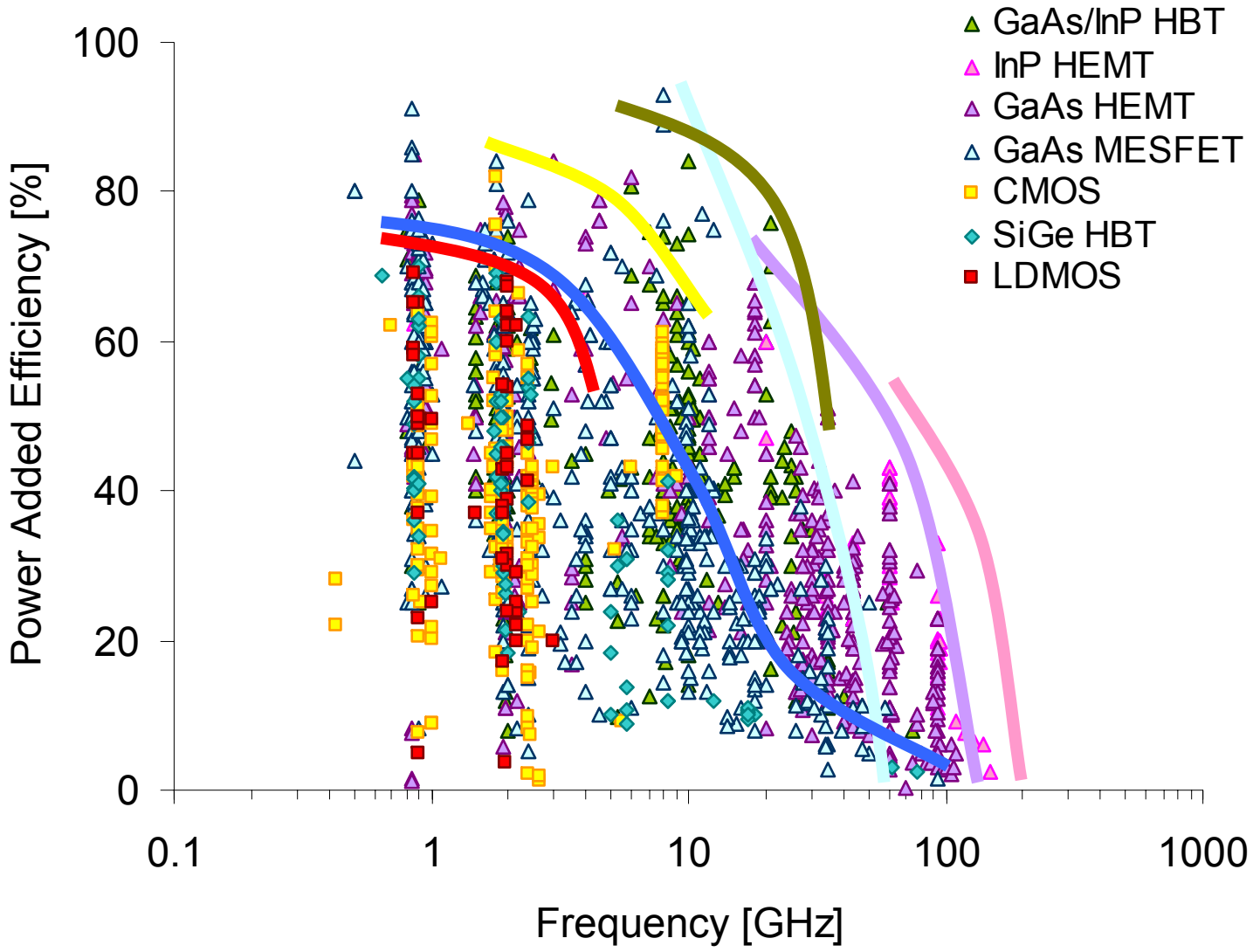
Key to frequency: efficiency



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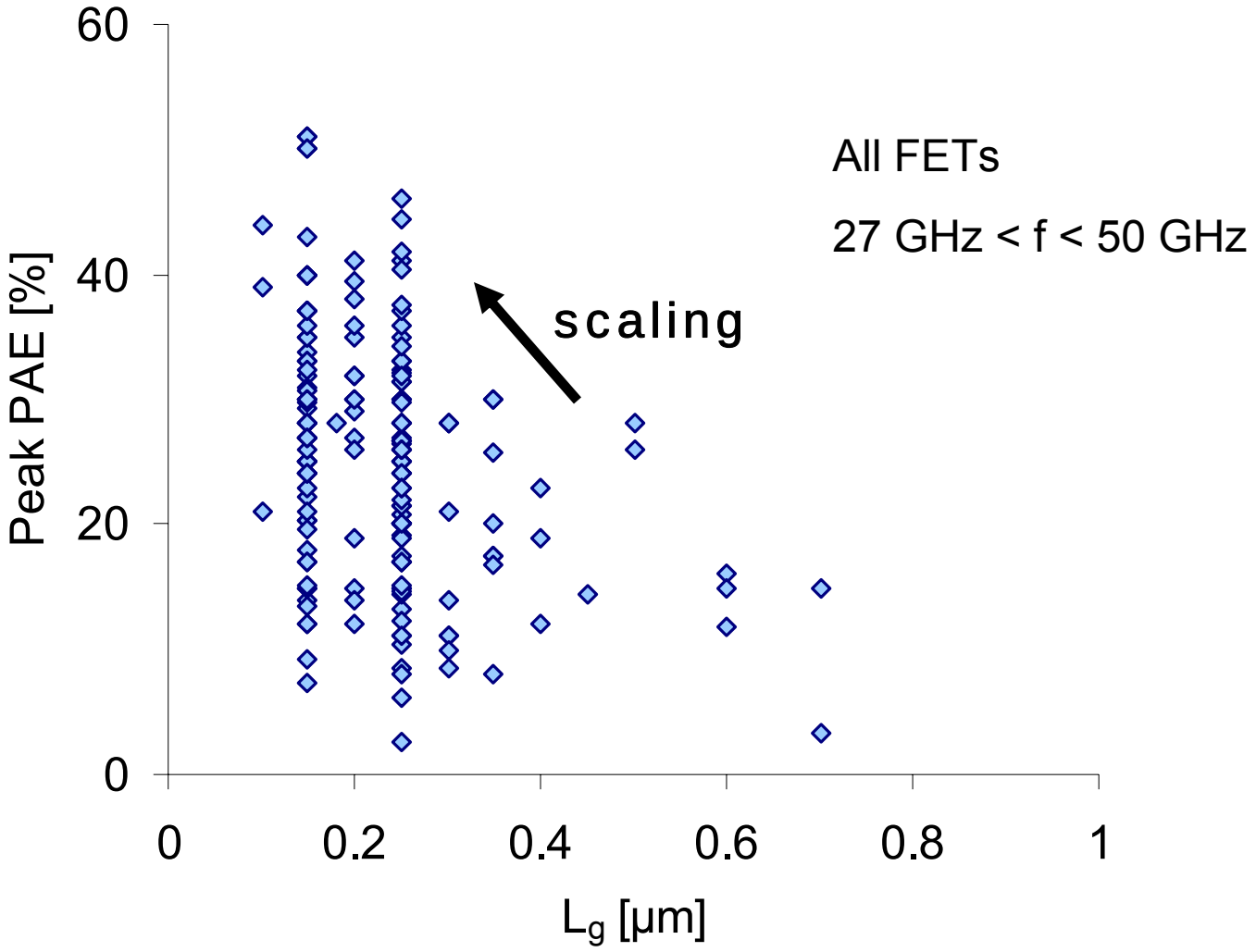
The benefits of scaling



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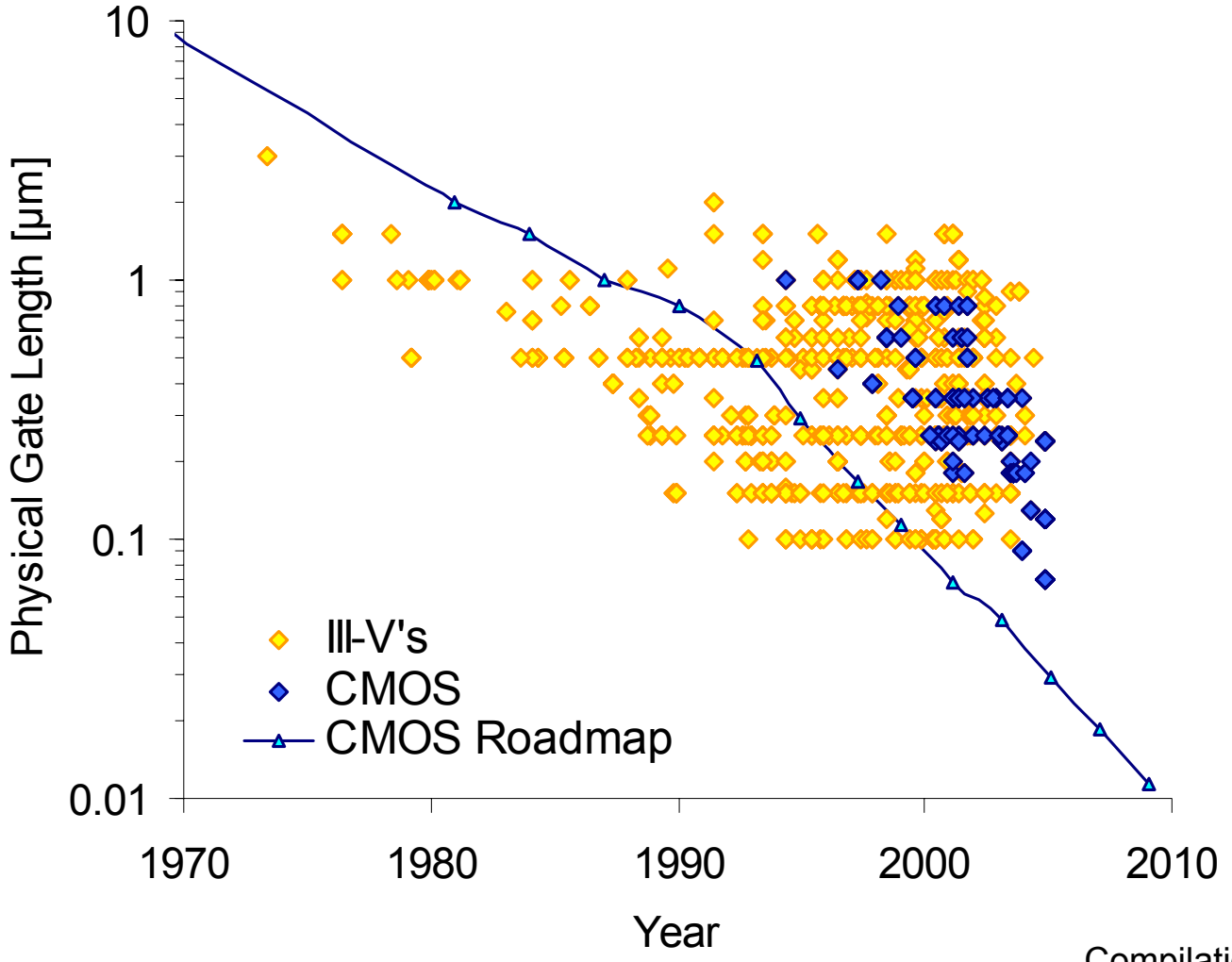
Gate length scaling in III-V FETs and CMOS



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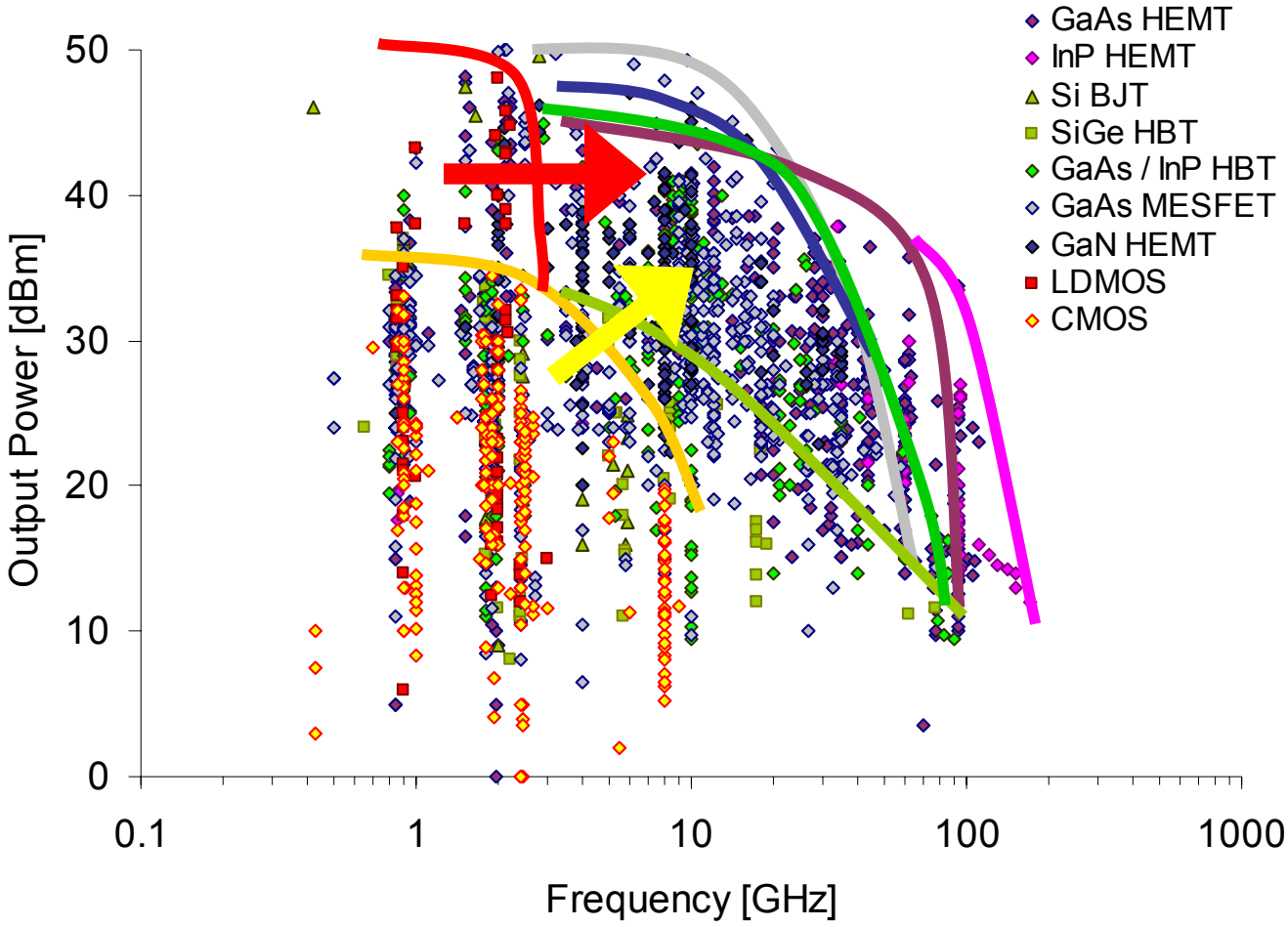
Si CMOS: a disruptive technology for RF power?

Si MOSFETs for RF power

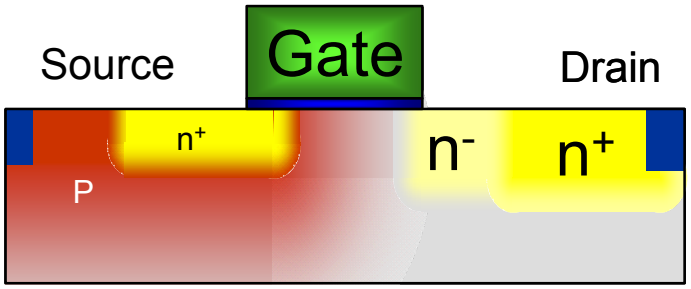


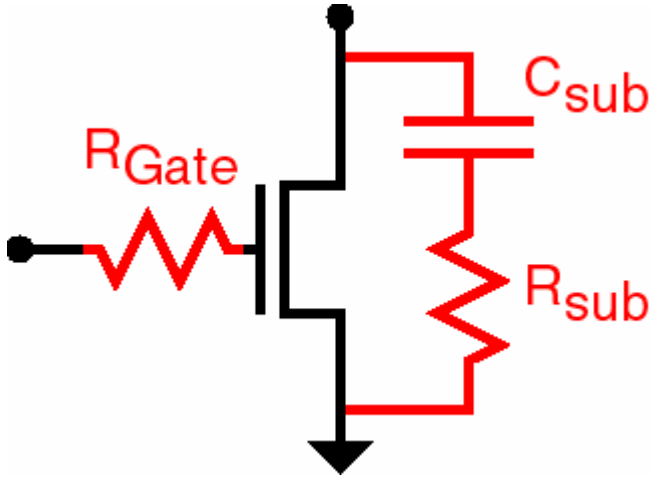
1. Extending LDMOS beyond 2 GHz
2. RF power suitability of deeply scaled CMOS

1. Extending LDMOS beyond 2 GHz

(PhD Thesis of J. Fiorenza)

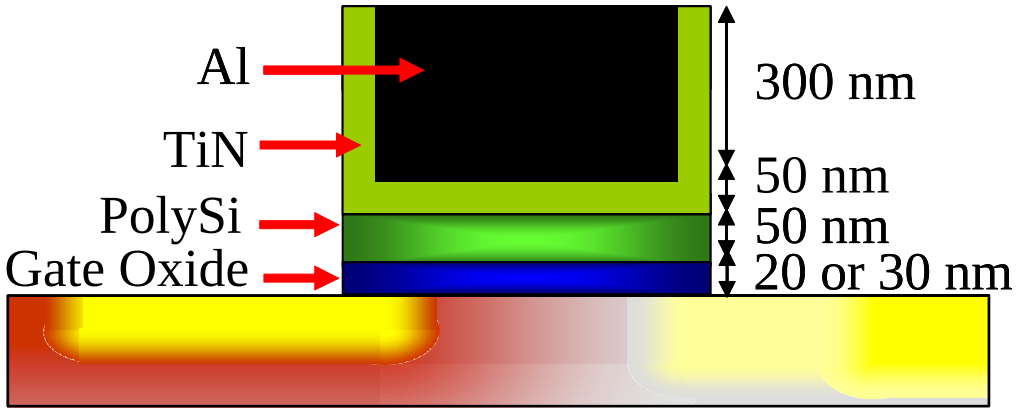
LDMOSFET: Lightly-doped Drain MOSFET





- Two critical sources of RF Loss:
  - Gate resistance loss: reduces power gain
  - Substrate loss: reduces power efficiency

Low-loss gate:
Metal/Poly-Si damascene gate

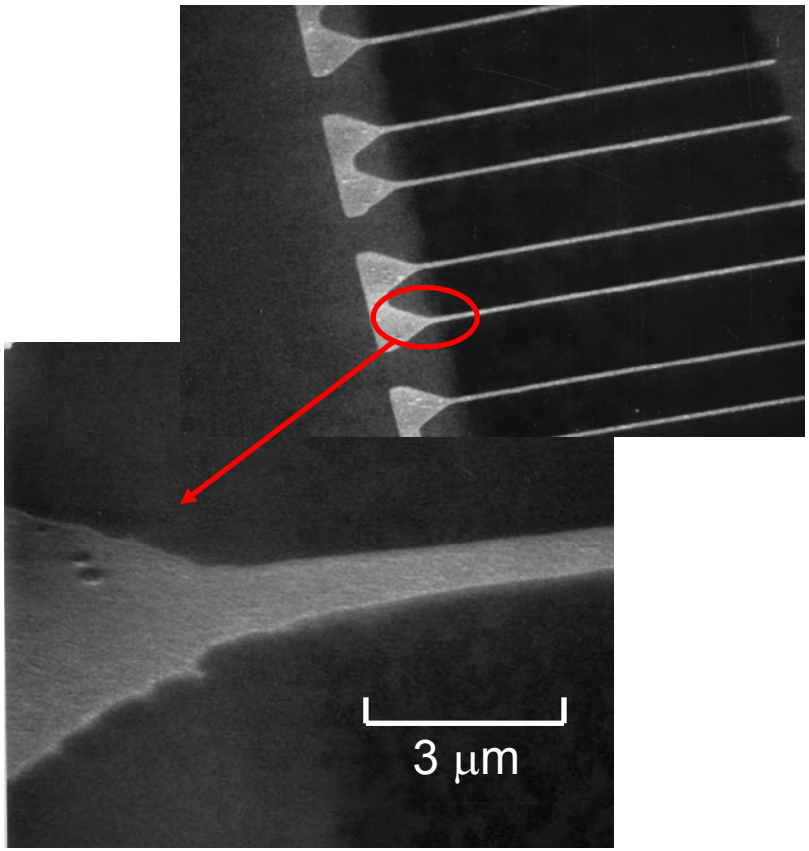


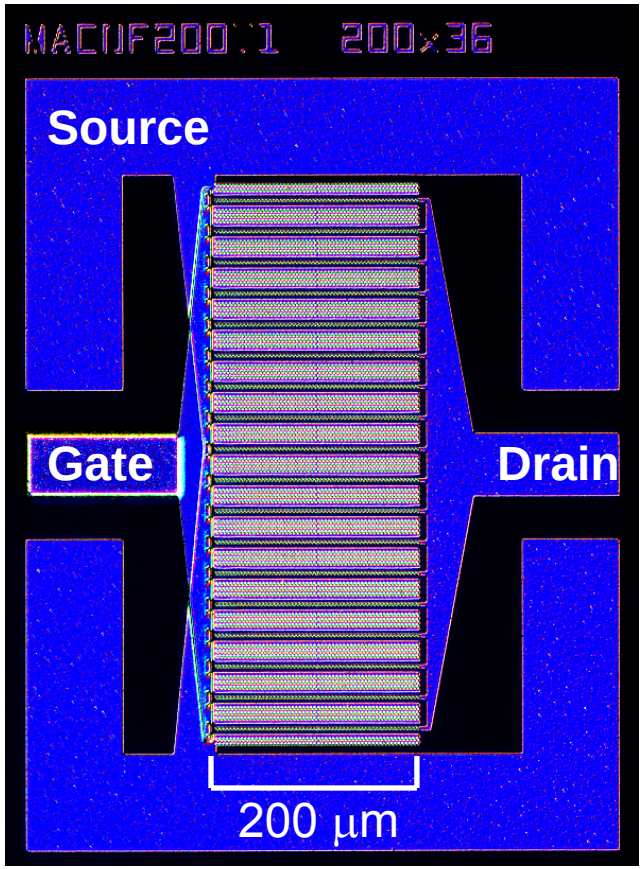
Advantages:

- Implemented in the back end of process
- Allows the use of Al or Cu: very low gate resistance
- Self-aligned: no increase in overlap capacitance
- Gate oxide undisturbed

Achieved: 0.2 ohm/sqr (>10 for polySi, ~1 for silic'd gate)

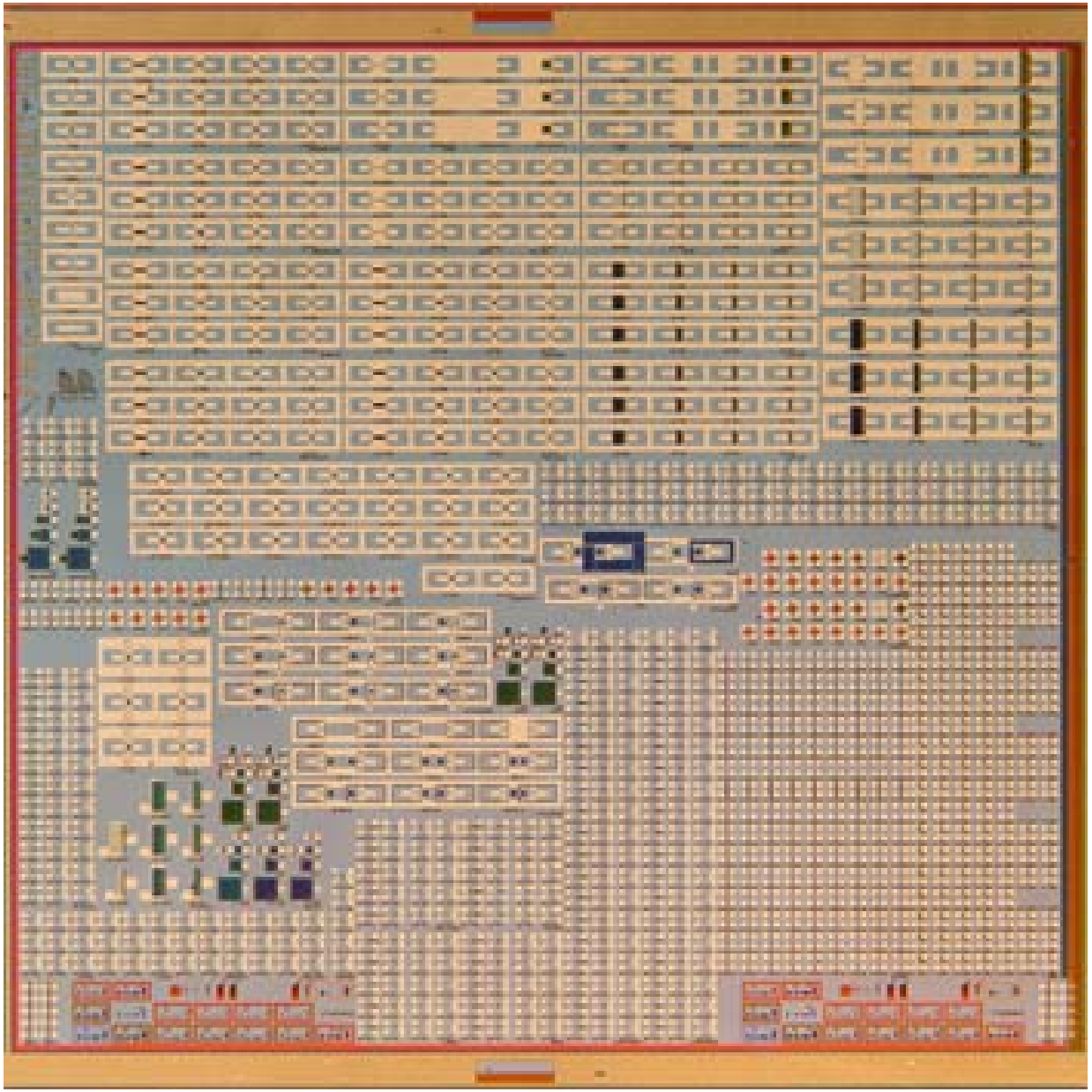
Metal/Poly-Si Damascene Gate





L_g = 0.6 μm f_t ~ 15 GHz BV_{off} > 18 V

Test chip



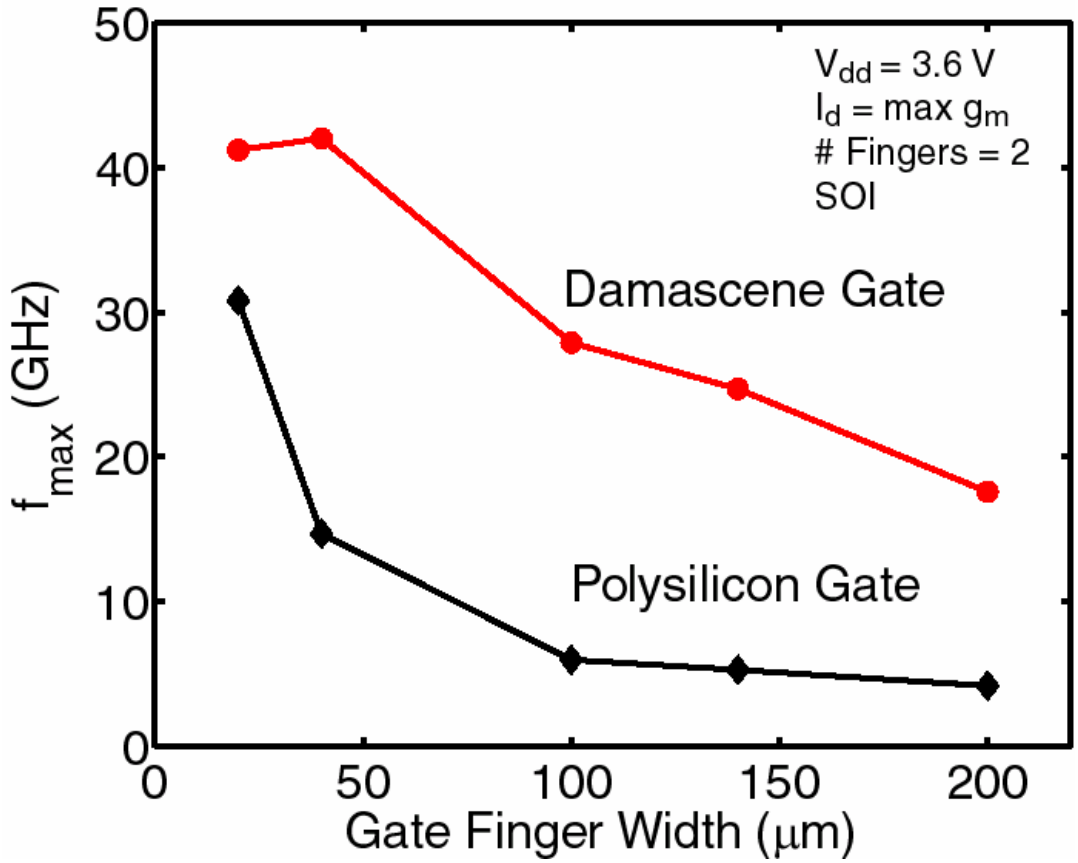
0.6 μm minimum L_g

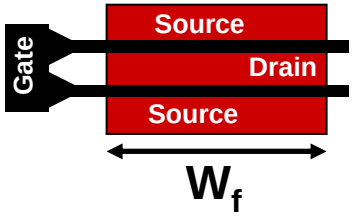
10 mask levels

2 levels of metal

Fabricated at MIT

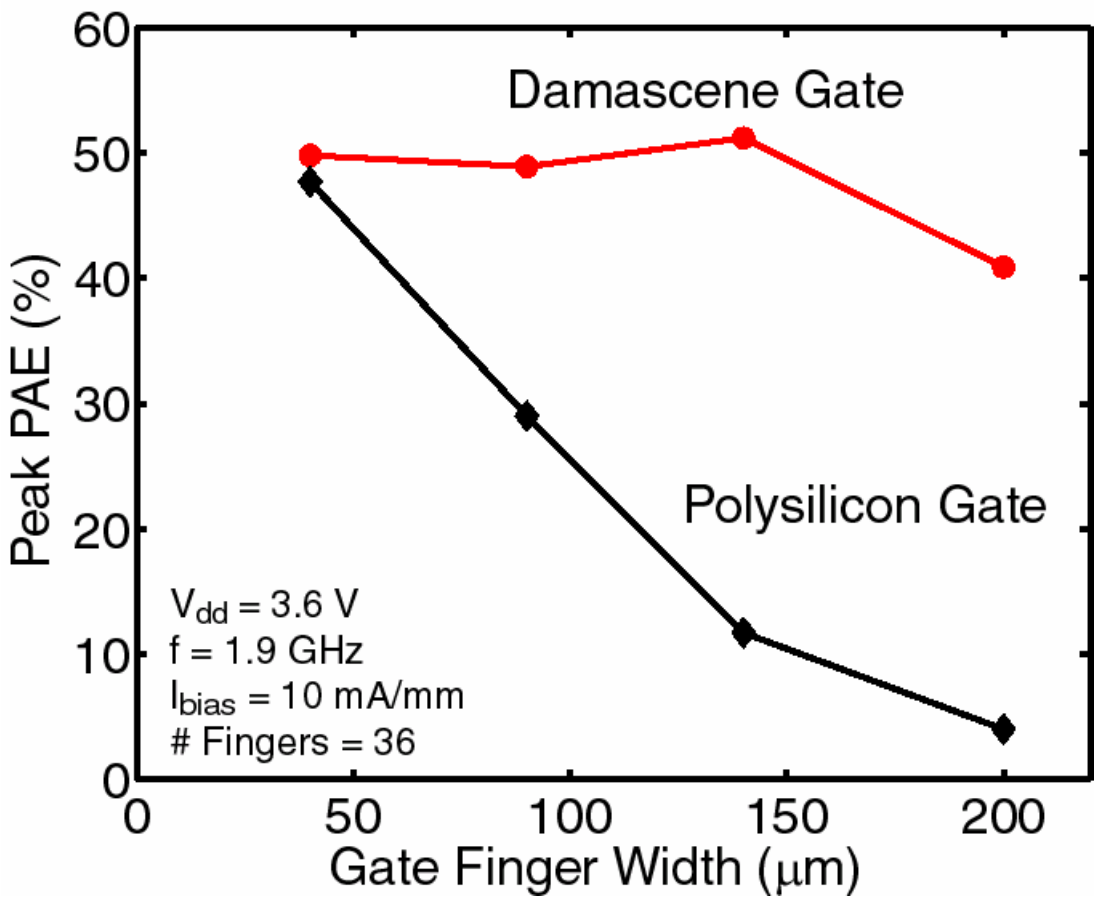
Benefit of low gate resistance: small signal

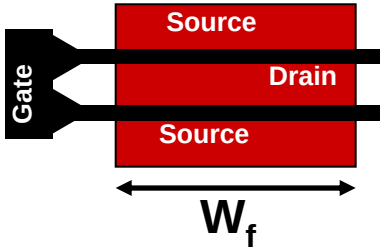




Damascene gate increases f_{max}, enables wide gate fingers

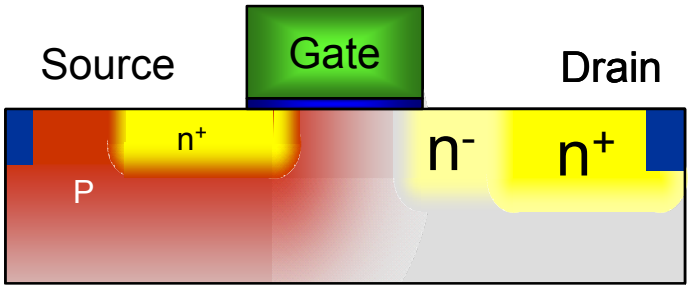
Benefit of low gate resistance: large signal



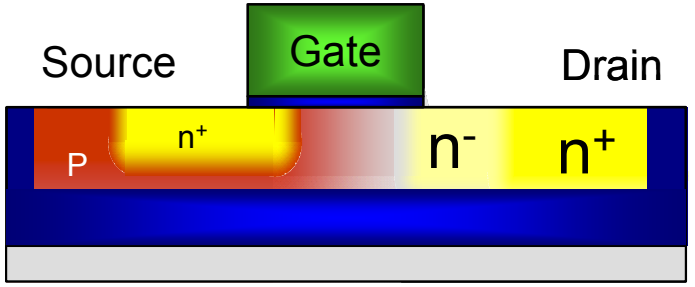


High PAE with gate finger width up to 140 μm

Low-loss substrates: SOI and high-resistivity Si



Bulk Si



Thin-film SOI

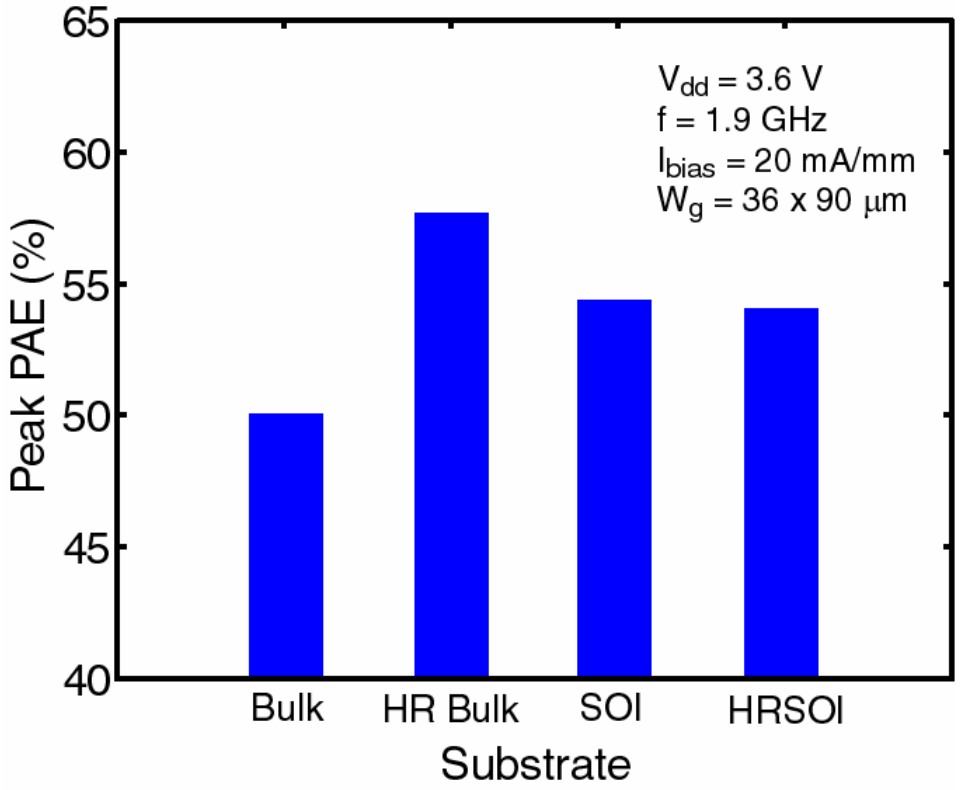
Substrate:

- Regular Si
- High-resistivity Si

Handle wafer:

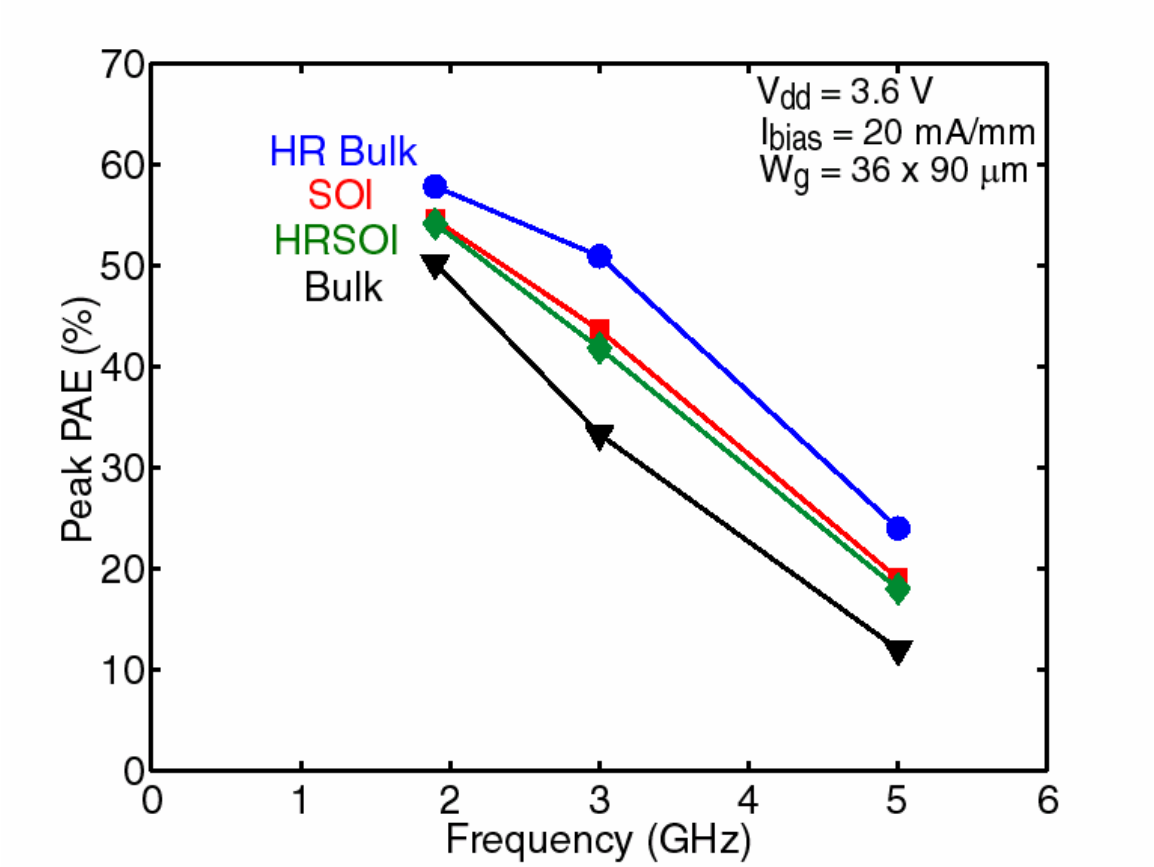
- Regular Si
- High-resistivity Si

Impact of substrate



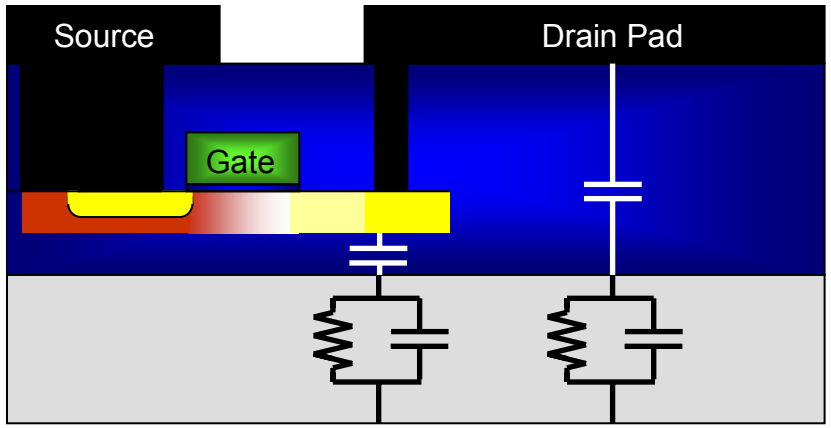
- SOI improves PAE
- High-resistivity silicon improves PAE on bulk
- High-resistivity silicon does not improve PAE on SOI

Beyond 2 GHz

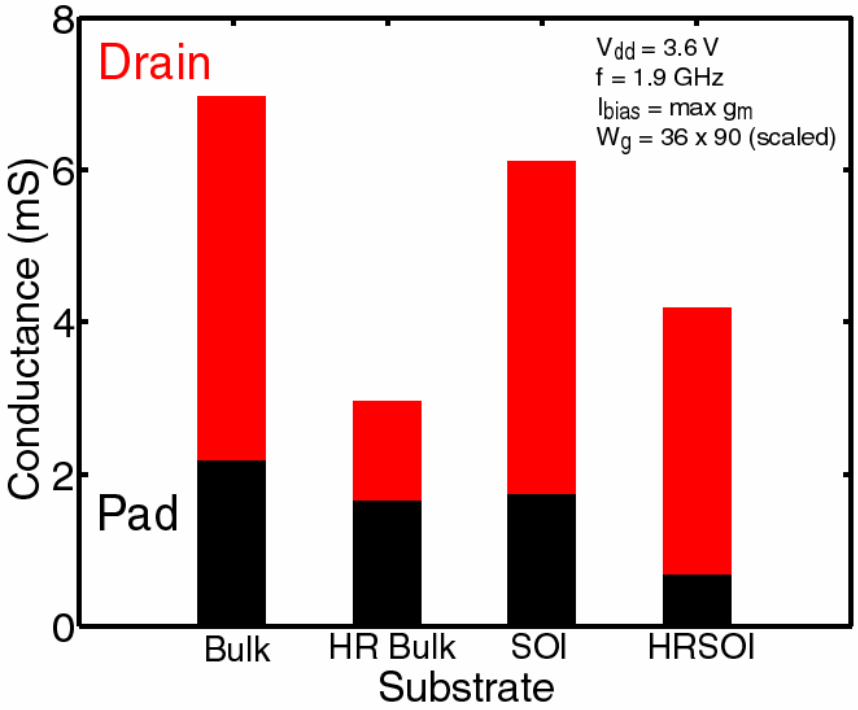


Low-loss substrate very important at high frequencies

Analysis of substrate loss

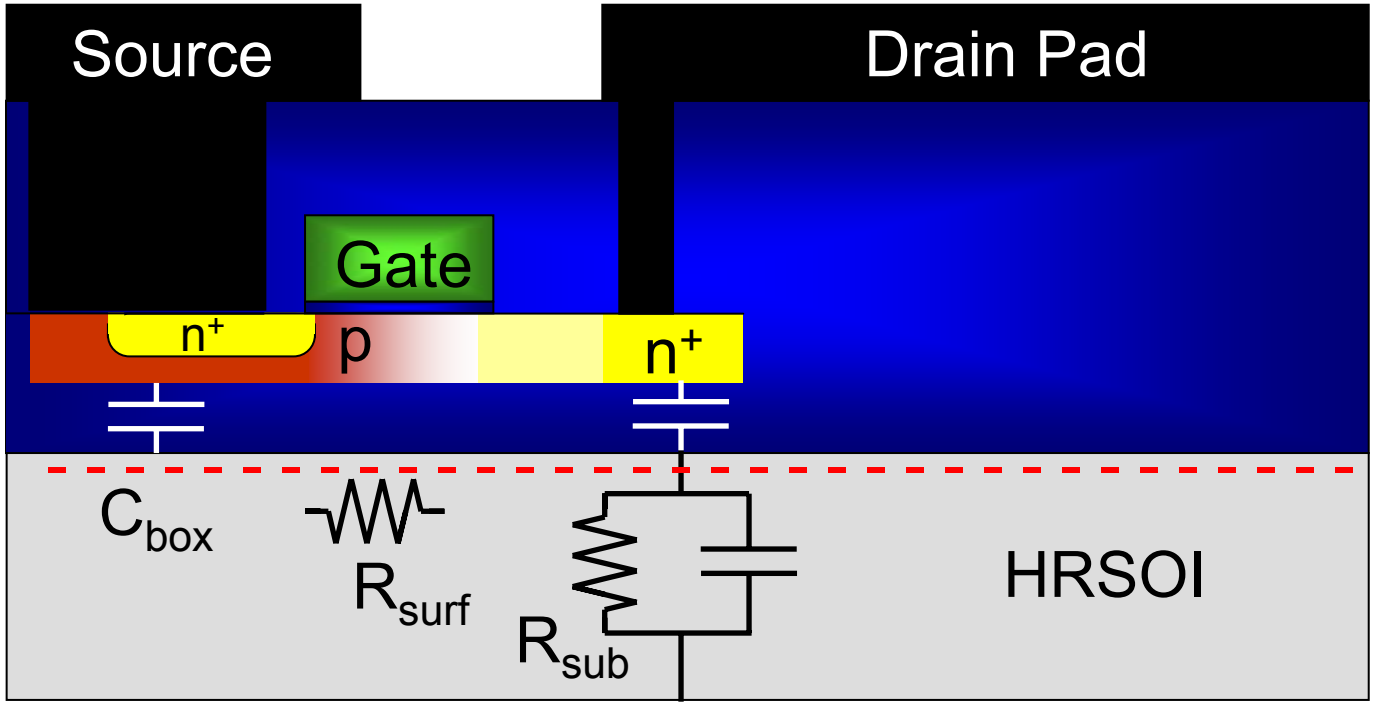


Drain Loss Pad Loss



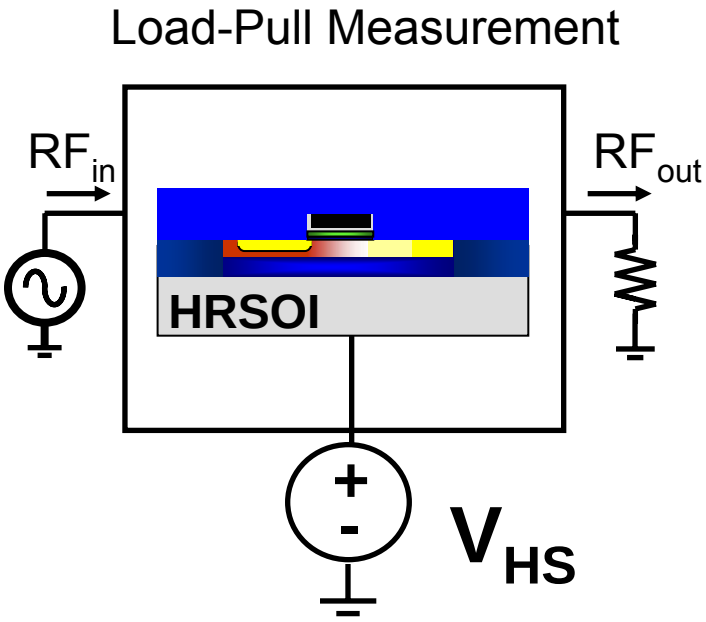
- Pad Loss:
  - SOI effective
  - HR effective on bulk Si and SOI
- Drain Loss:
  - SOI somehow effective
  - HR very effective on bulk Si, only moderately on SOI

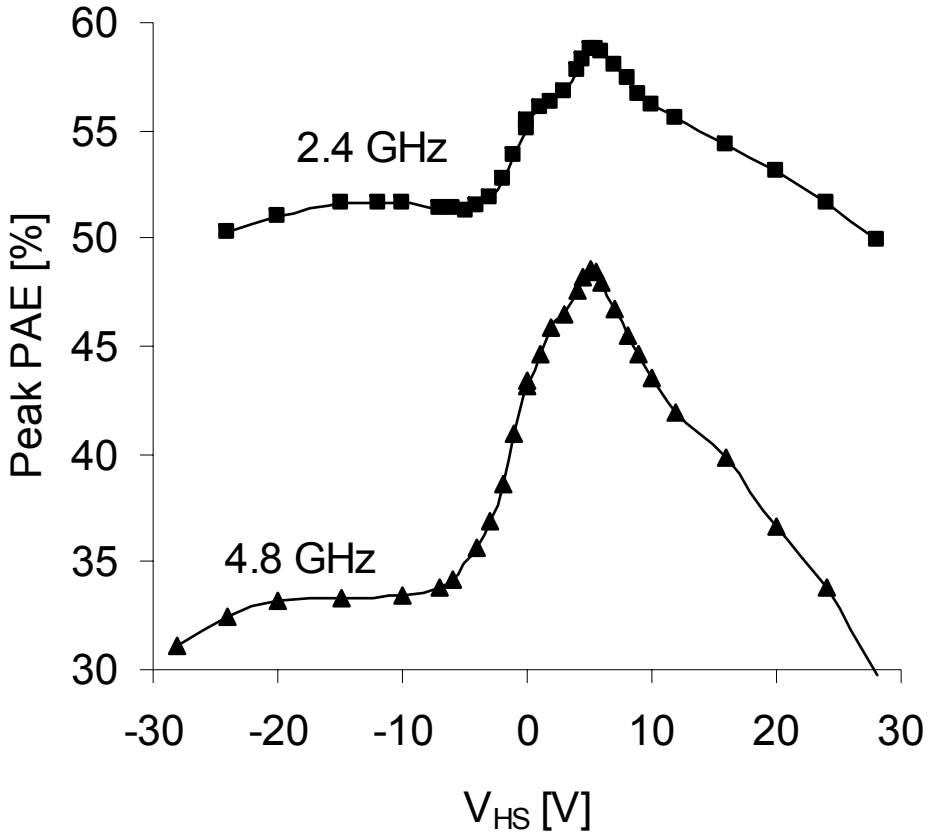
Why is HRSOI Ineffective?



Surface inversion increases drain loss on HRSOI

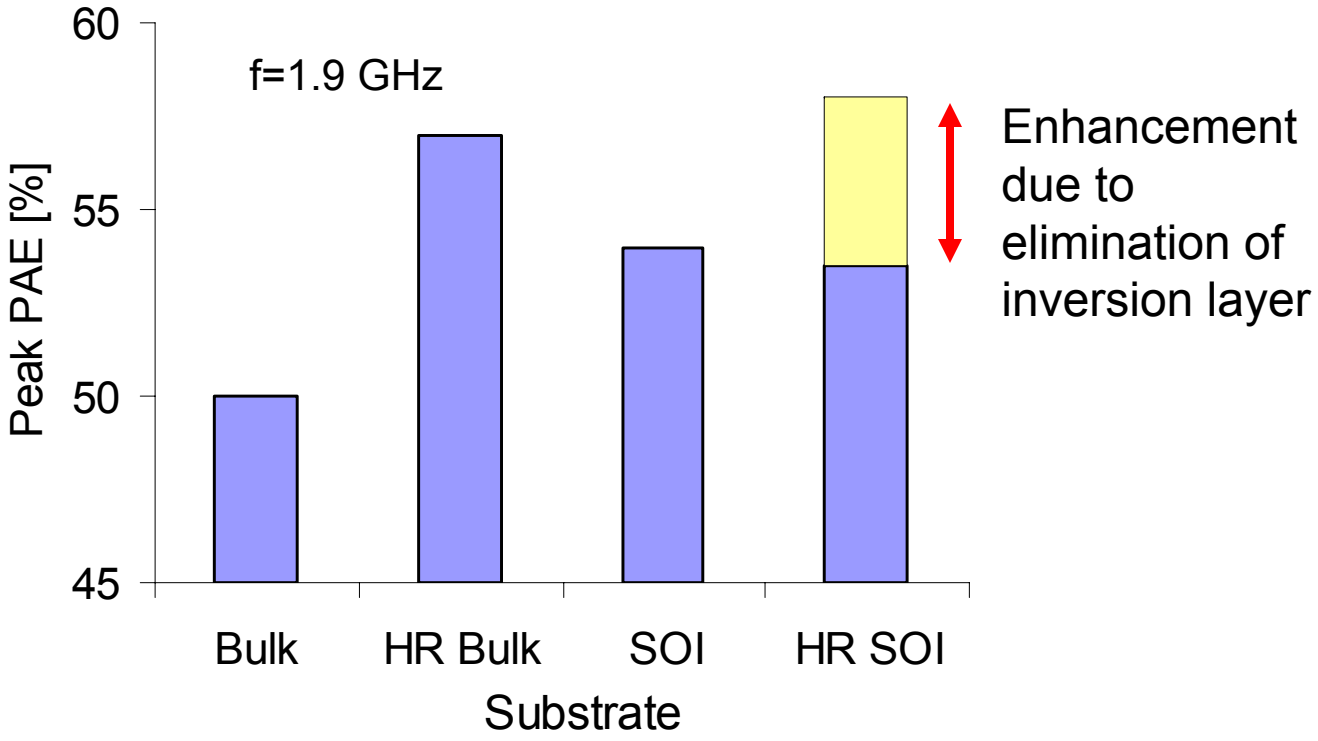
Effect of substrate inversion in HRSOI-LDMOS





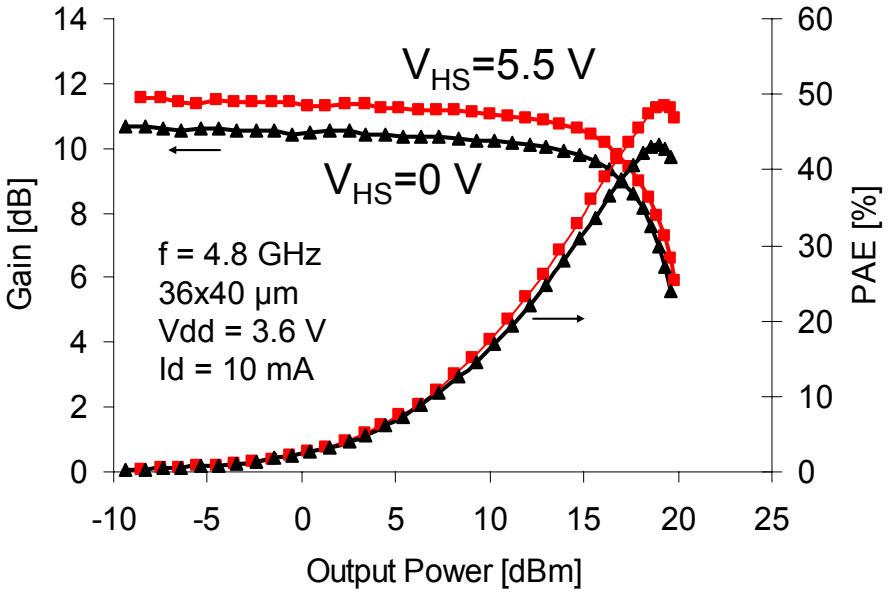
- Eliminating substrate inversion improves PAE
- Most prominent at high frequencies

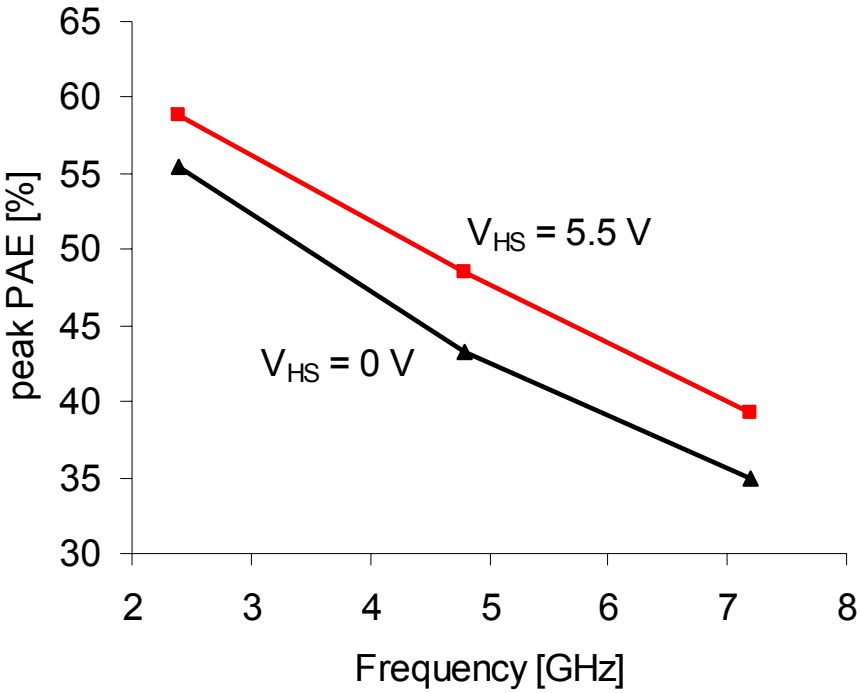
Impact of inversion layer elimination



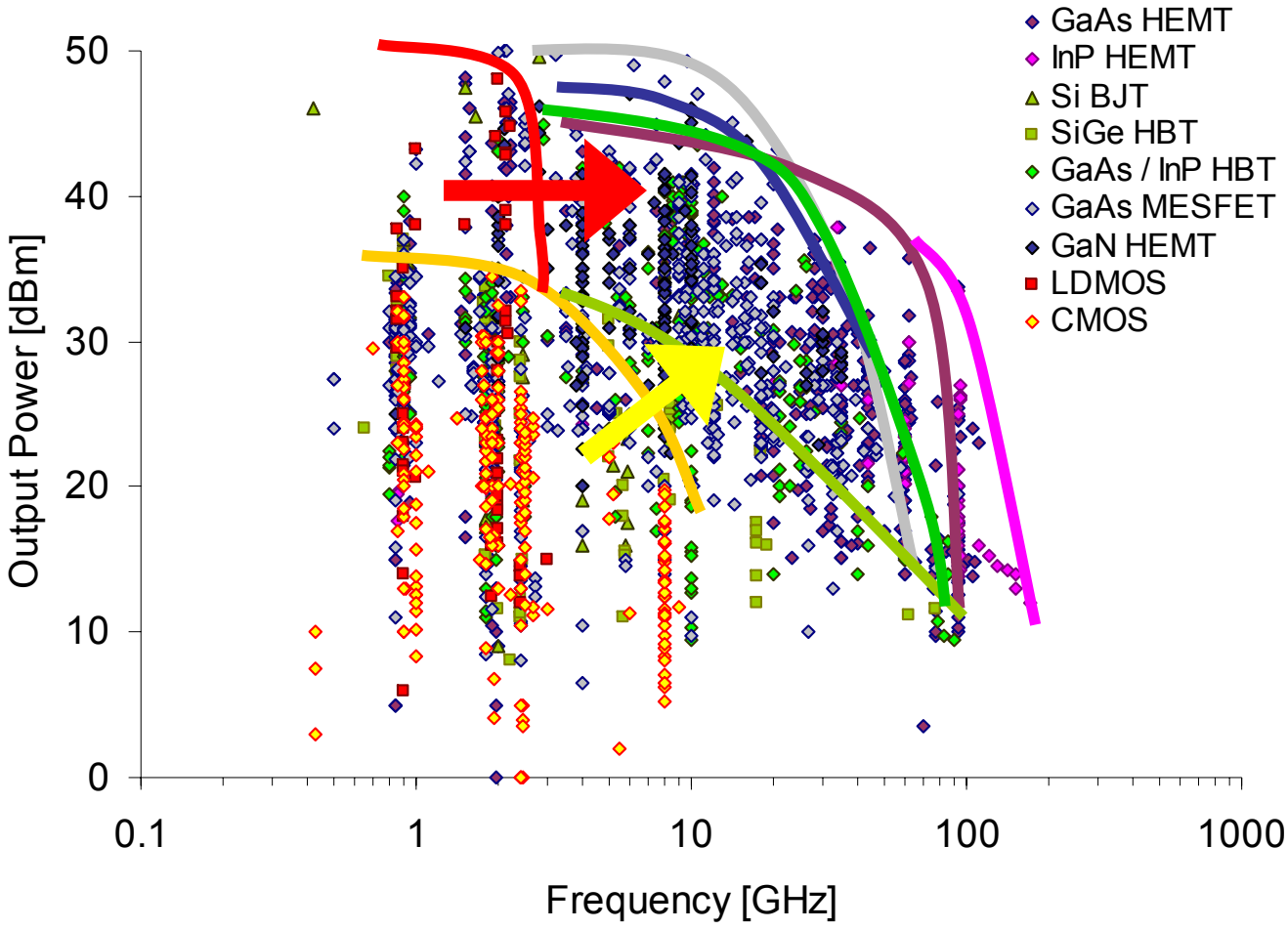
Impact of inversion layer elimination

- Eliminating substrate surface effects improves performance:
  - Particularly prominent in LDMOS due to large drain area
  - Both linear and saturated performance
  - Most prominent at high frequencies





Si MOSFETs for RF power



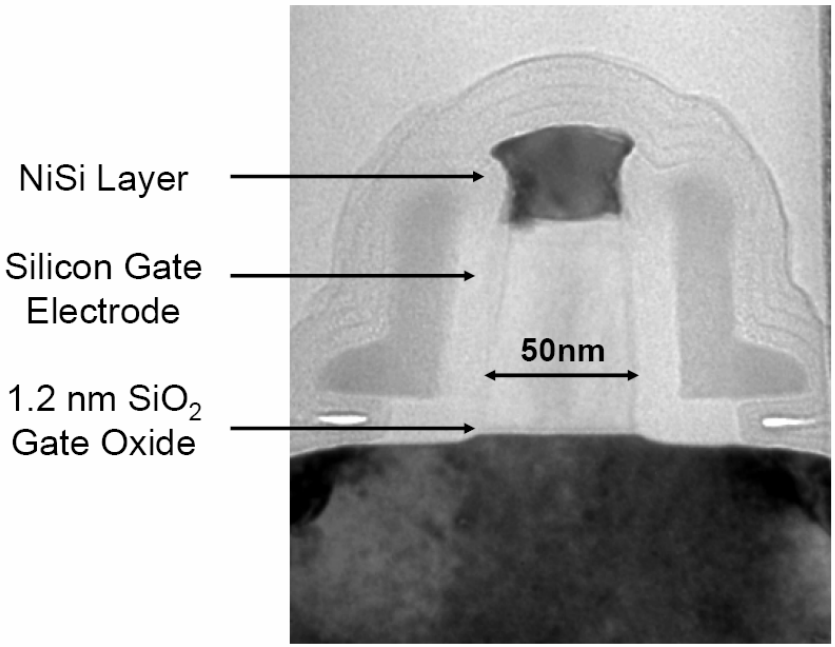
1. Extending LDMOS beyond 2 GHz
2. RF power suitability of deeply scaled CMOS

2. RF power suitability of deeply scaled CMOS

(PhD Thesis of J. Scholvin)

Attractiveness of CMOS:

- System-on-Chip integration
- Low cost
- Low voltage
- Good device models
- Aggressive roadmap
- Wide flavor of devices available



90 nm CMOS

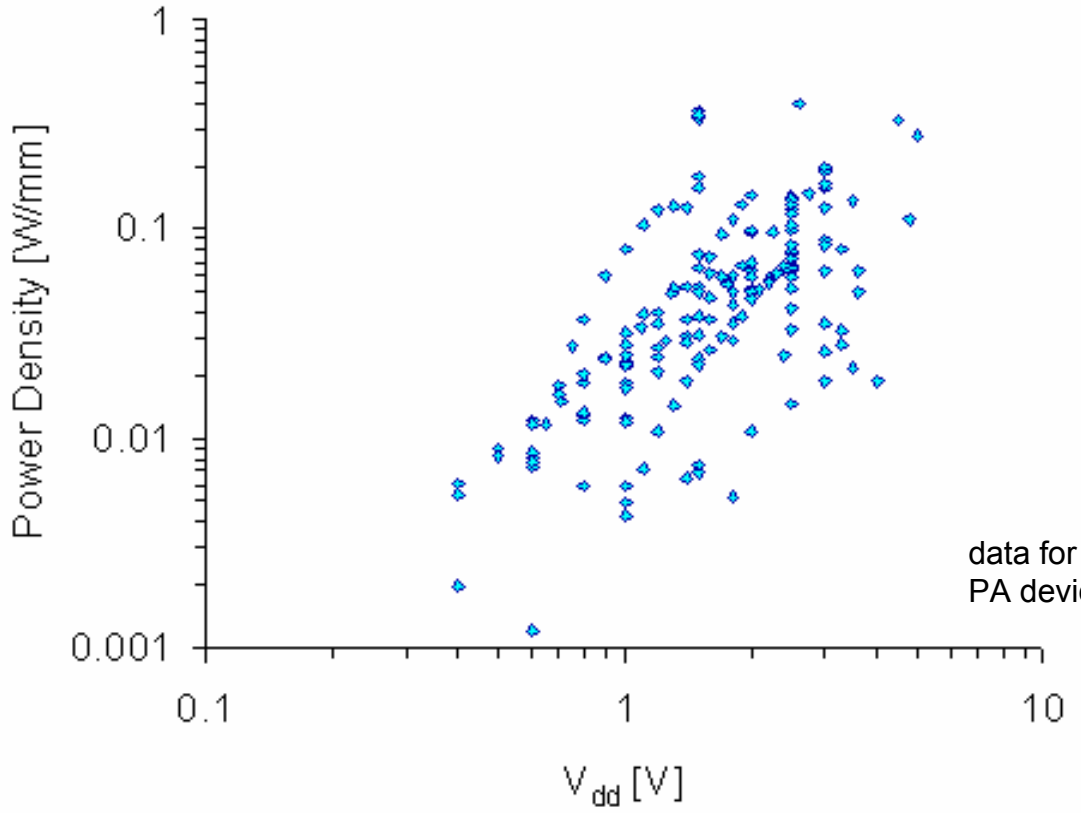
Suitable for:

- High-volume, low cost consumer ap
- Moderate frequencies (2-10 GHz)
- Medium power (<100 mW)
- Current: WLAN, Bluetooth, Cell-phone PA driver, WiMax/802.16

Picture from:
http://www.intel.com/research/silicon/micron.htm#silicon

Issues of CMOS for RF power

- Concerns: CMOS scaling $\Rightarrow V_{dd} \downarrow \Rightarrow P_{out} \downarrow$



- Possible solutions:
  - Raise $V_{dd} \Rightarrow$ impact on reliability
  - Use I/O devices $\Rightarrow$ not really scaling

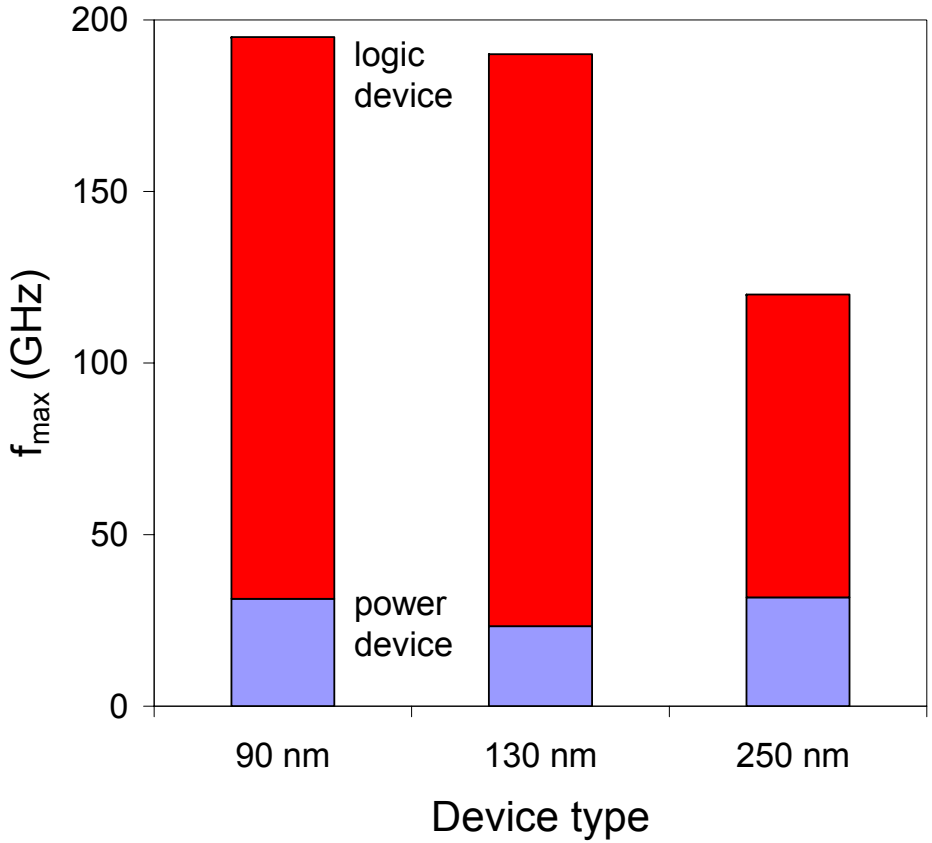
90 nm CMOS:
there is a lot more than 90 nm devices!

- Includes devices with longer gate lengths and thicker gate oxides for I/O drivers and high V operation

- Designed RF power devices in collaboration with IBM

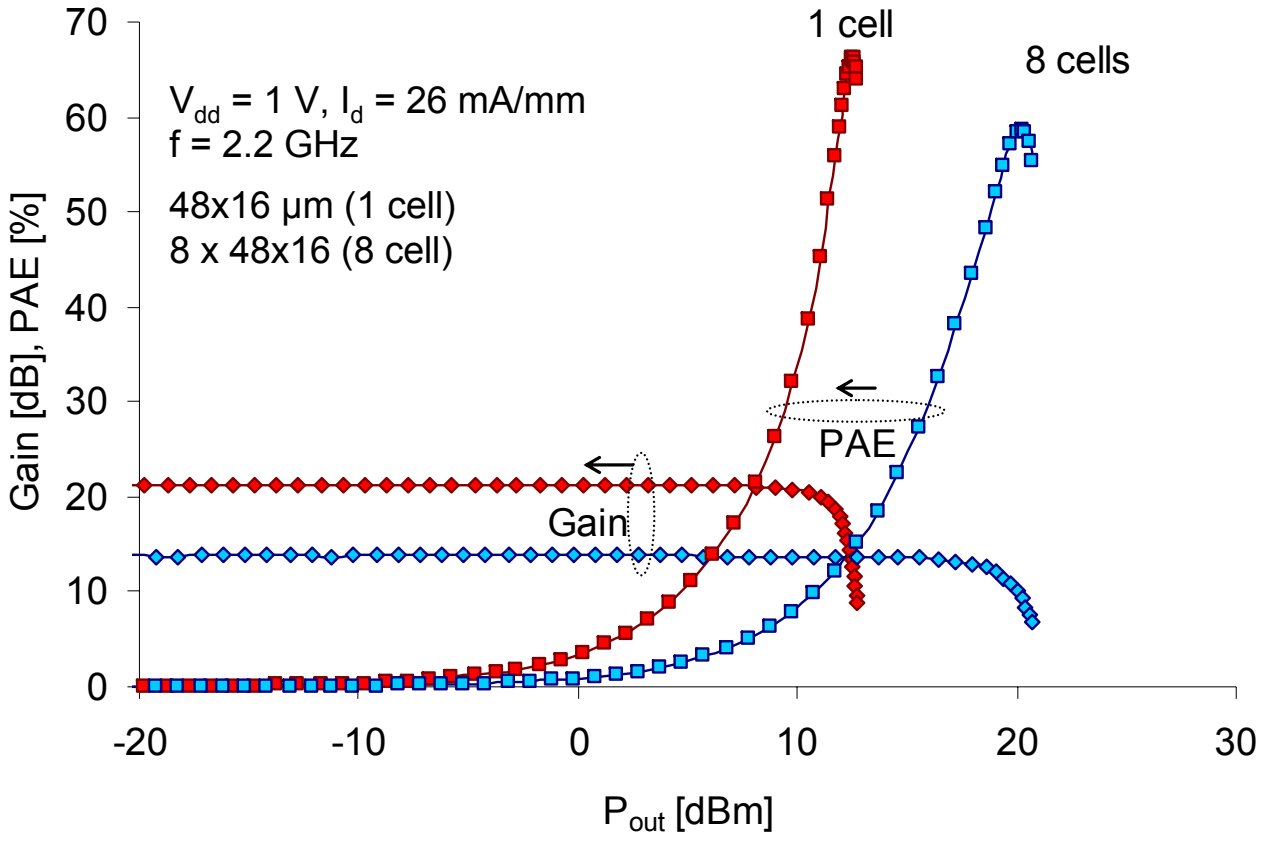
Oxide thickness	thin (14 A)	medium (22 A)	thick (51A)
Nominal voltage [V]	1.0	1.2	2.5
L_g = 90 nm	(x)		
L_g = 130 nm	x	(x)	
L_g = 250 nm	x	x	(x)

The benefits of scaling for RF



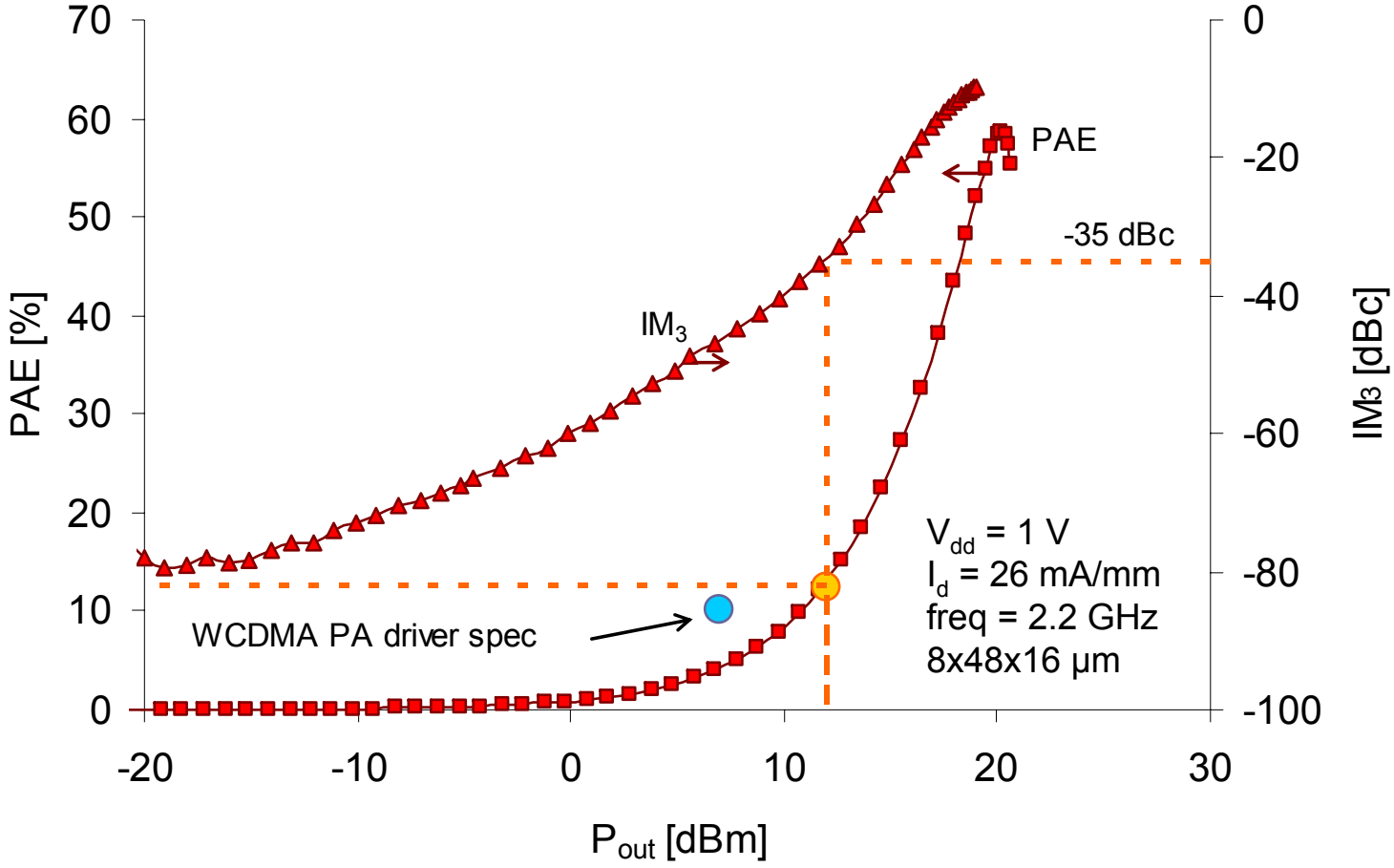
- Logic devices at optimized bias point have very high bandwidth
- But… power devices at class AB bias point have much less bandwidth

RF power performance of standard 90 nm devices



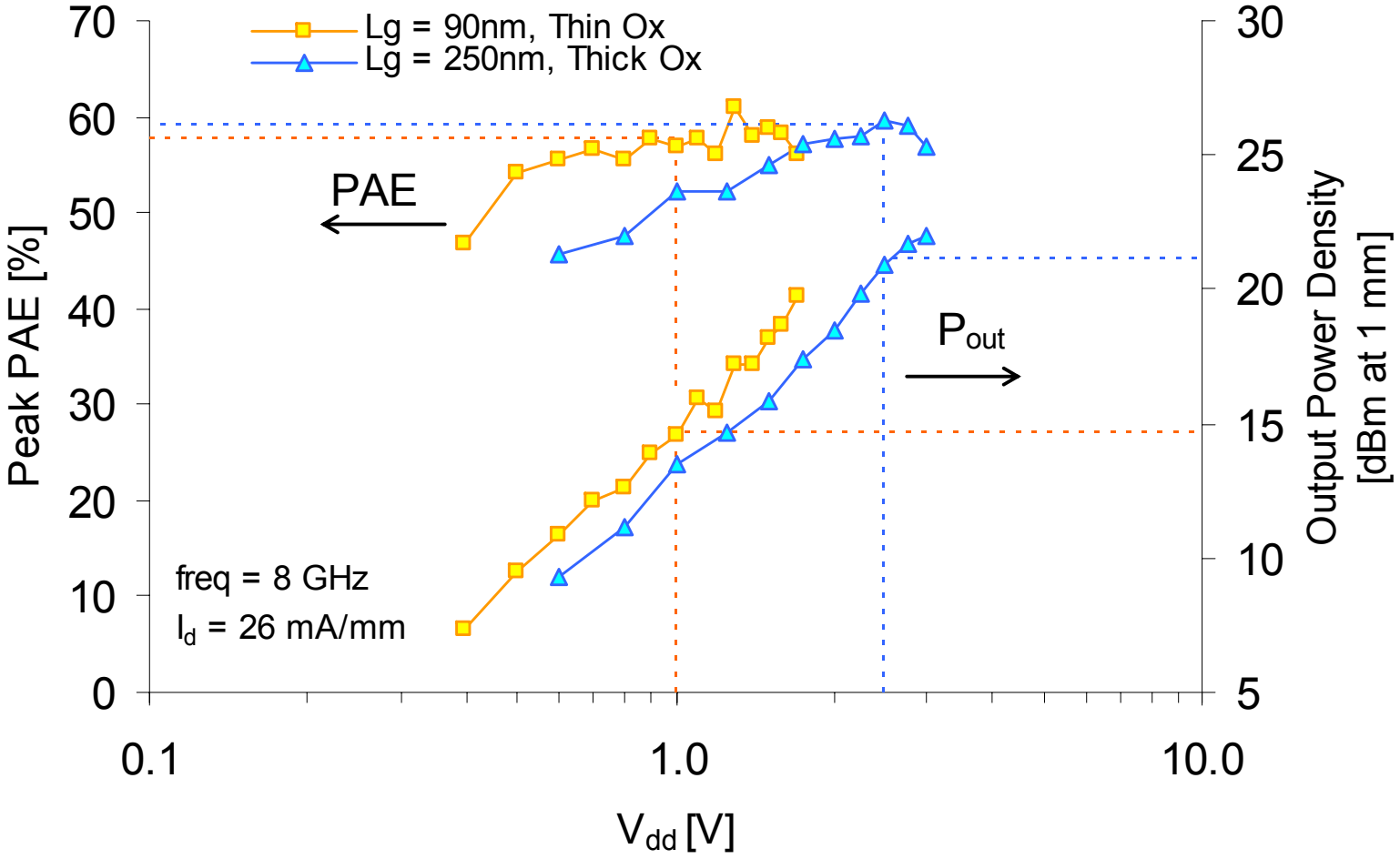
- 1 cell: Peak PAE = 66% at P_{out} = 12.5 dBm
- 8 cell: Peak PAE = 59% at P_{out} = 20.2 dBm

Linear performance of 90 nm CMOS



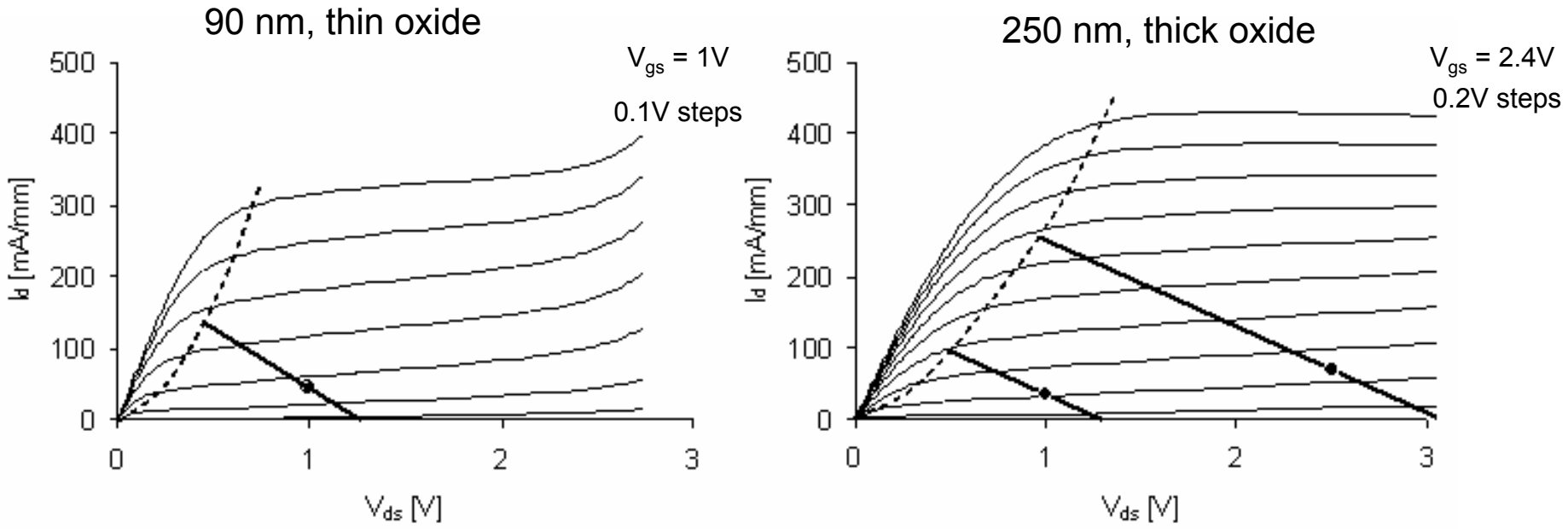
- What is PAE at a given IM_3 ?
  - at IM_3 = -35 dBc, PAE = 12% at P_{out} = 12 dBm
- Exceeds WCDMA PA driver specs

90 nm vs. 250 nm devices at 8 GHz



- At V_{dd} = 1 V, 90 nm has best PAE and P_{out}
- 250 nm device offers highest power density at V_{dd}=2.5 V

90 nm vs. 250 nm

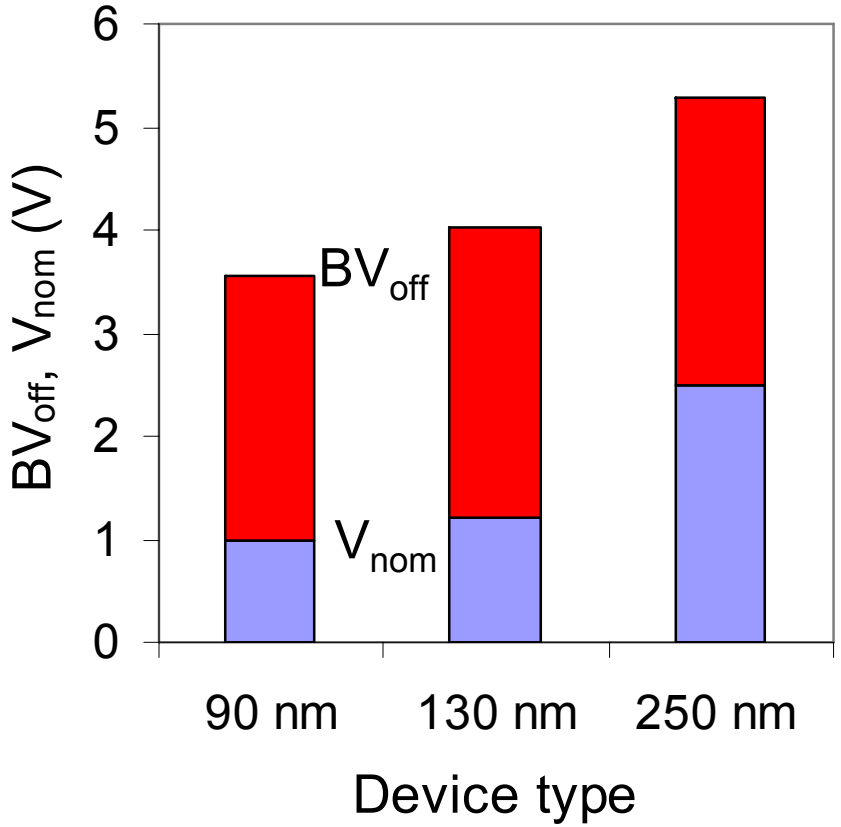


- 250 nm thick oxide device has higher $V_{ds,sat}$
  $\Rightarrow$ compresses earlier and softer $\Rightarrow$ lower P_{out} and peak PAE
- As $V_{dd} \uparrow$ impact of $V_{ds,sat}$ decreases

What about reliability?

For RF power, reliability related to ratio of:

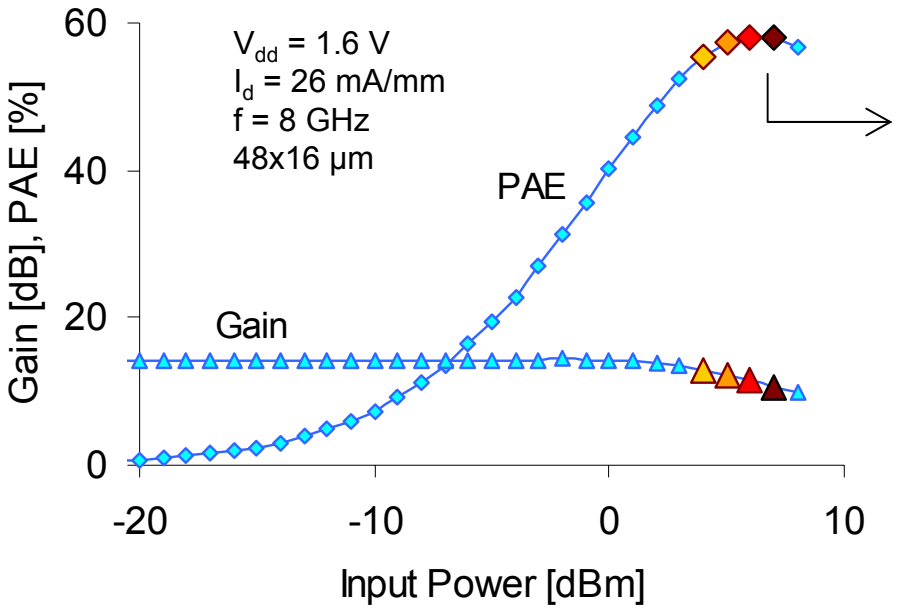
- nominal V_{dd}
- to breakdown voltage

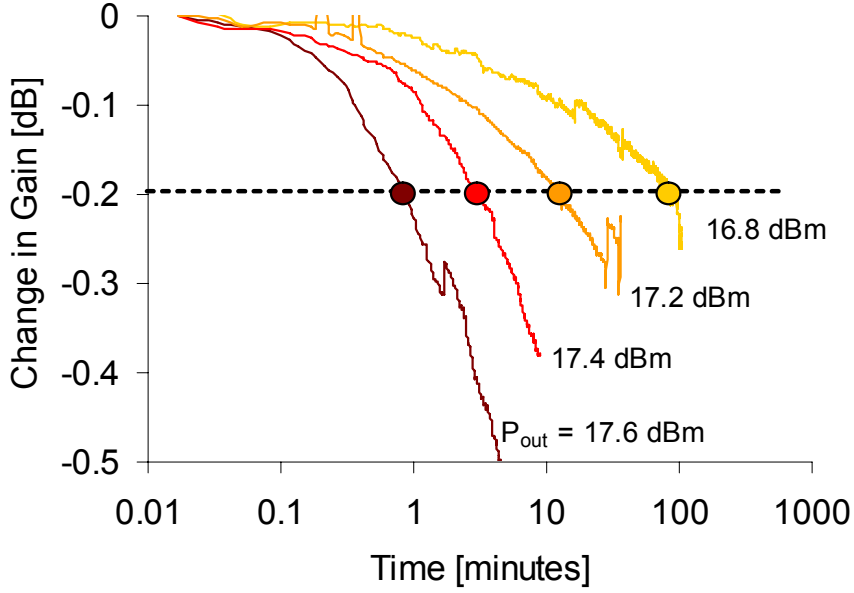


For RF power:

- 90 nm device expected to be ***more*** reliable at V_{dd}=1 V than 250 nm device at 2.5 V

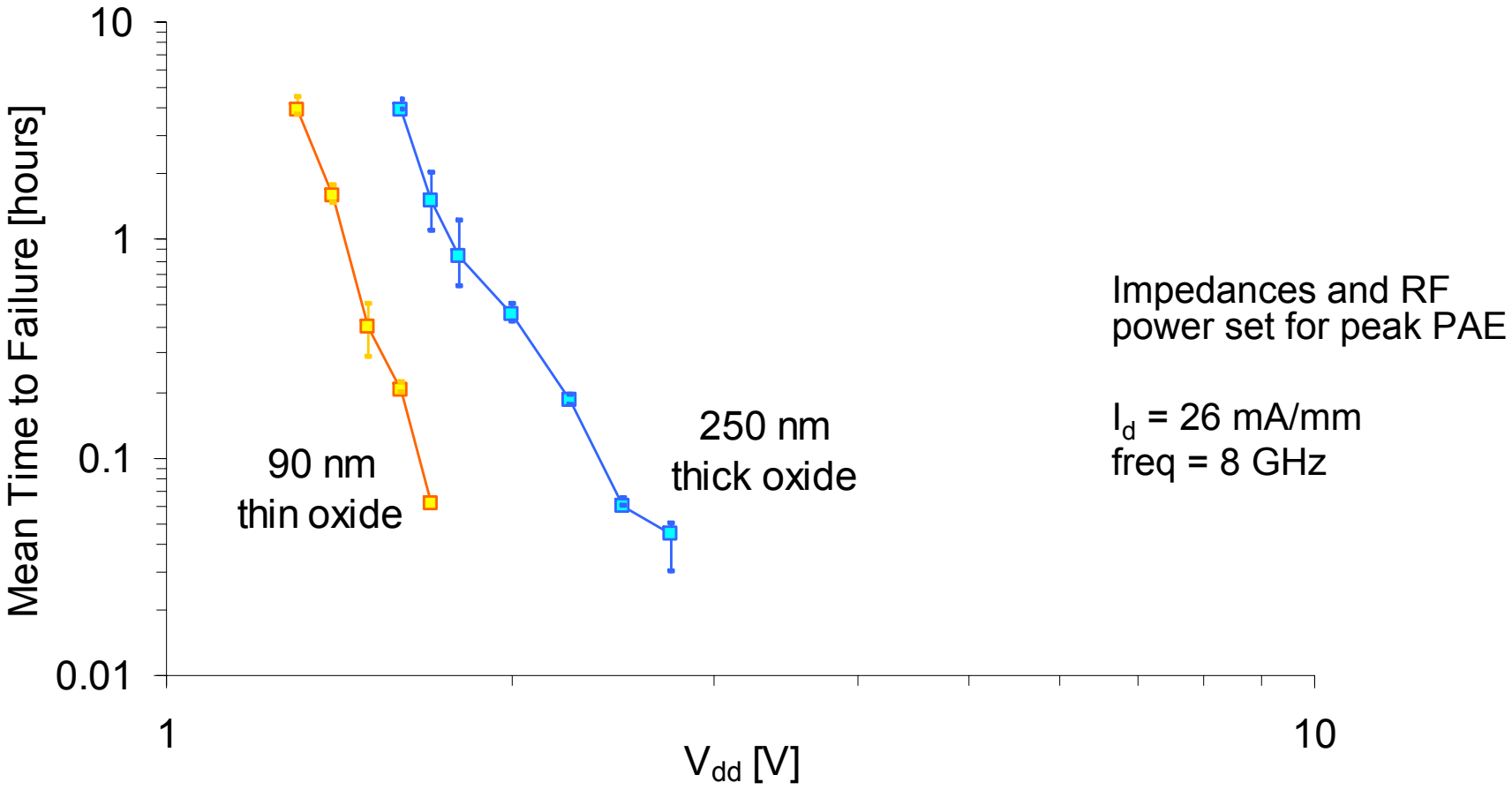
Reliability: impact of output power





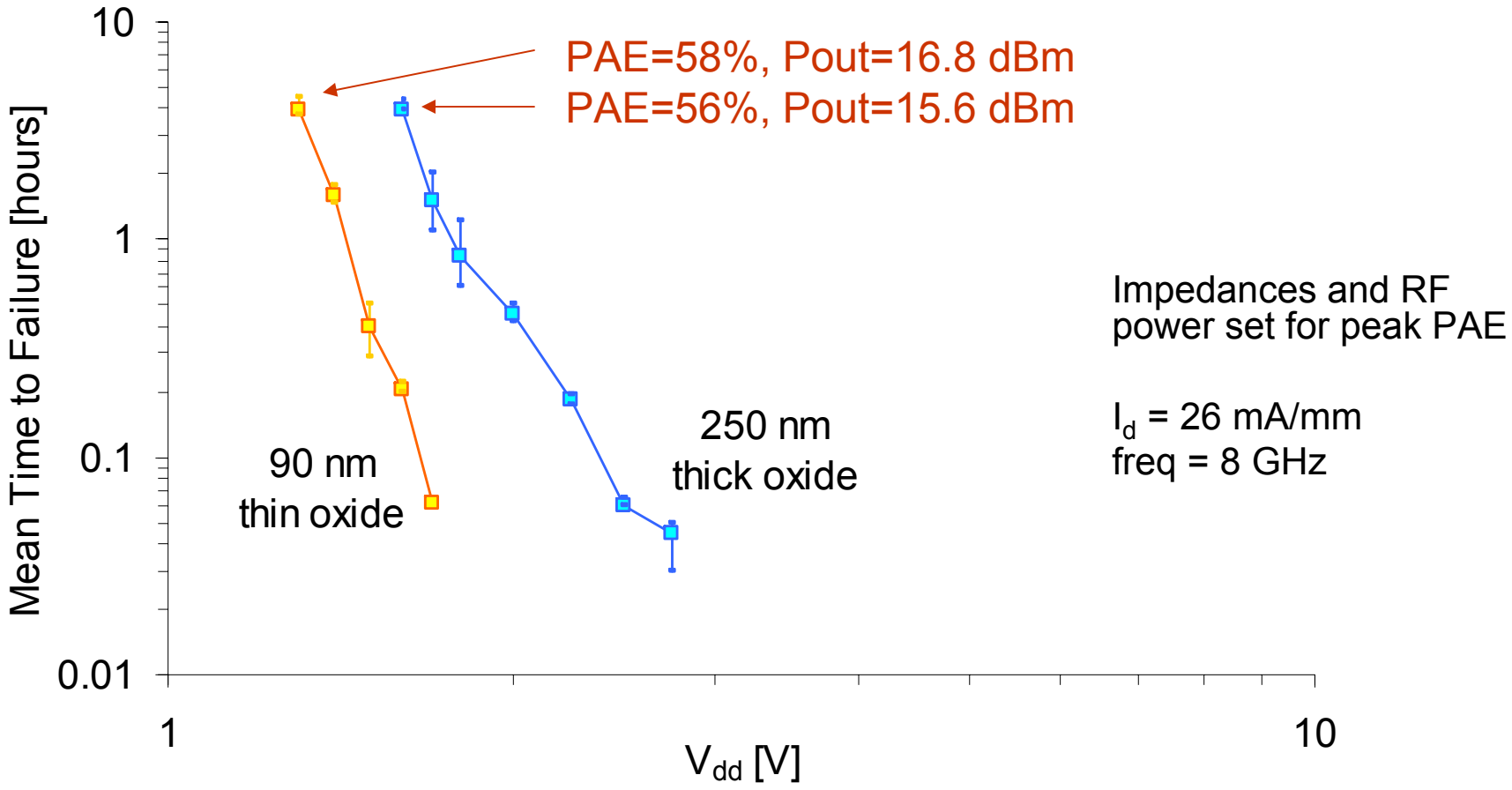
- Run device under continuous RF power conditions
- Measure drop in gain over time, define MTTF as 0.2 dB drop
- Power compression has huge impact on degradation

Reliability: impact of V_{dd}



- For same V_{dd}, thick oxide is more reliable
  - but thin oxide has better performance
- For identical lifetime, how does performance compare?

Reliability: impact of V_{dd}

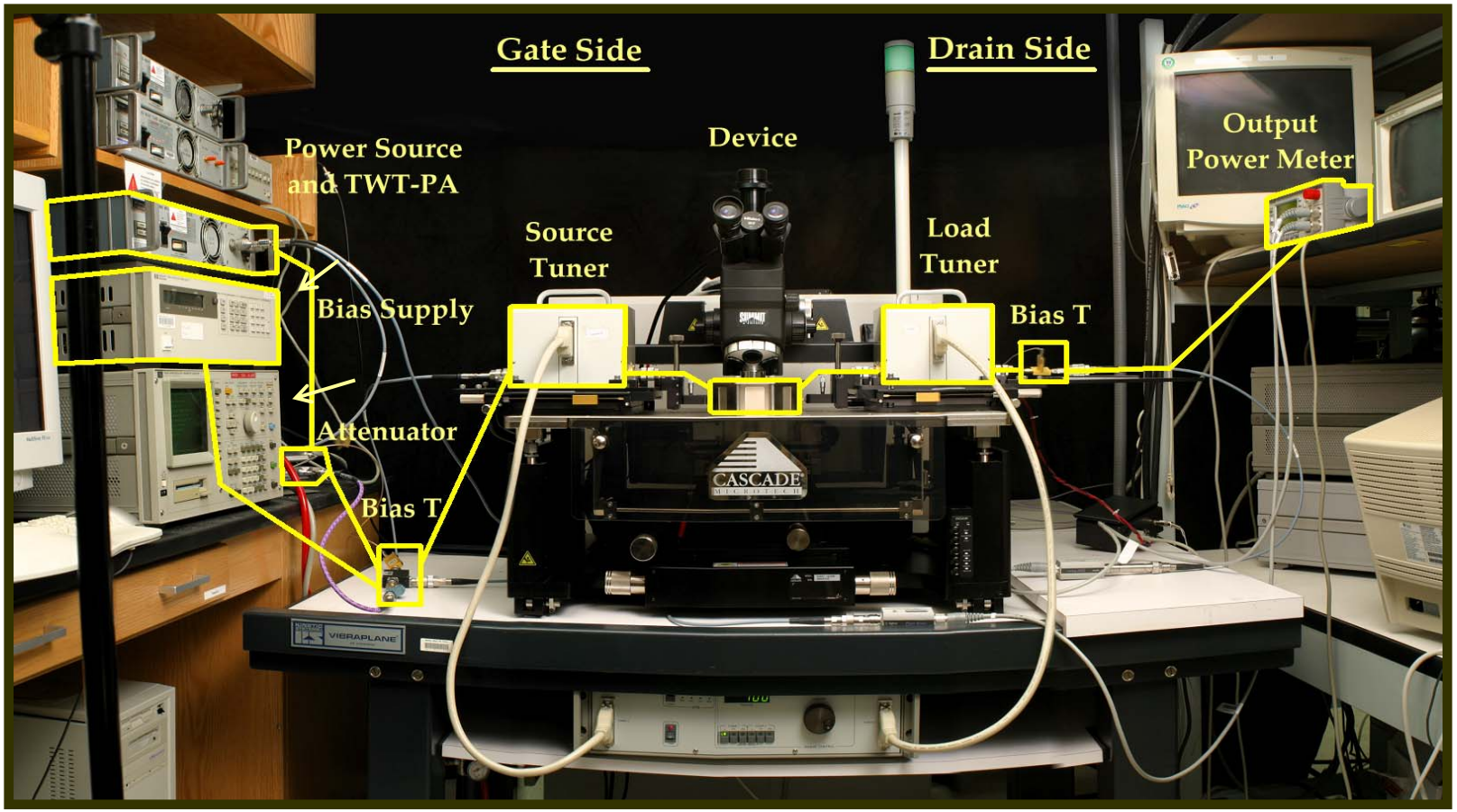


- 90 nm thin ox. outperforms 250 nm thick ox. for high MTTF
  - Low V_{dd} performance of 90 nm device much better than 250 nm device

Conclusions

- Metal-containing gates and low-loss substrates will project LDMOS to 5-6 GHz
- Deeply scaled CMOS suitable for RF power for:
  - Moderate power levels (~100 mW)
  - Very low operating voltage (~1 V and below)
- Scaling will project CMOS beyond 10 GHz
- Si-based RF power technologies will dominate many high-volume consumer applications:
  - WLANs, bluetooth, cellphone PA drivers, RF tags, etc

MIT's RF power measurement setup



- 1.8 - 18 GHz Maury ATS automatic load-pull system
- 8-inch Cascade on-wafer probe station
- Synthesized source with 10 W TWT-PA supplying up to 200 mW at DUT

References

- LDMOS:
  - Bengtsson: MTT 2003
  - Fiorenza: SOI Conf. 1999; MTT-S 2001; IEDM 2002, EDL 2001, 2003, 2005; TED 2002
  - Scholvin: IEDM 2003
  - Van der Heijden: MTT-S 2001

- 90 nm CMOS:
  - Ferndahl: MGWL 2003
  - Scholvin: IEDM 2004