A Metal/Polysilicon Damascene Gate Technology for RF Power LDMOSFETs

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***Abstract*—This letter describes a metal/polysilicon damascene gate technology for RF power LDMOSFETs. We compare the performance of SOI LDMOSFETs with metal/polysilicon damascene gates to that of identical devices with n^+ polysilicon gates. The gate sheet resistance of the metal/polysilicon gate was 0.2 Ω/sq. This very low sheet resistance greatly improved f_{max} and peak PAE, especially for the wide gate fingers that are critical in RF power applications. With a 140 μm gate finger width, f_{max} was improved from 5 GHz to 25 GHz, and peak PAE at 1.9 GHz was improved from 12% to 52%.**

***Index Terms*—Damascene gate, RF LDMOSFET, SOI.**

I. Introduction

A LOW sheet-resistance gate is a critical element of any RF LDMOSFET technology. RF LDMOSFETs are used today at frequencies between 900 MHz and 2 GHz for a wide variety of RF power amplifier applications, including cellular handsets [1] and base stations [2]. The low sheet-resistance gate enables high RF power gain with the wide gate fingers that are needed to produce the large output power levels demanded by these applications. Refractory metal [3] and refractory metal polycide [4] gates are presently utilized in LDMOSFET processes, and have a gate sheet-resistance as low as 0.8 Ω/sq. In order to enhance LDMOSFET performance in 900 MHz and 2 GHz applications, new gate technologies are needed which further reduce the gate sheet resistance. They are also essential to push the frequency limits of LDMOSFETs beyond 2 GHz, making LDMOSFETs effective for emerging RF power applications in the 4–6 GHz range, such as wireless LANs (WLAN) and fixed wireless access (FWA).

Here we describe a metal/polysilicon damascene gate technology implemented in an SOI LDMOSFET process. Though promising in digital CMOS [5], the merits of the metal/polysilicon damascene gate for RF power applications have never been previously demonstrated. The essential advantage of the metal/polysilicon damascene gate is that it is implemented in the back-end of a fabrication process. This allows the use of metals with very high conductivity, such as aluminum or copper, enabling a gate sheet-resistance that is far lower than can be achieved with refractory metals or refractory metal polycides. The metal/polysilicon damascene gate is also self-aligned and therefore does not increase gate-to-source/drain overlap capacitance, as do aluminum gate strap technologies [1] and T-gates [6] that have previously been used with LDMOSFETs.

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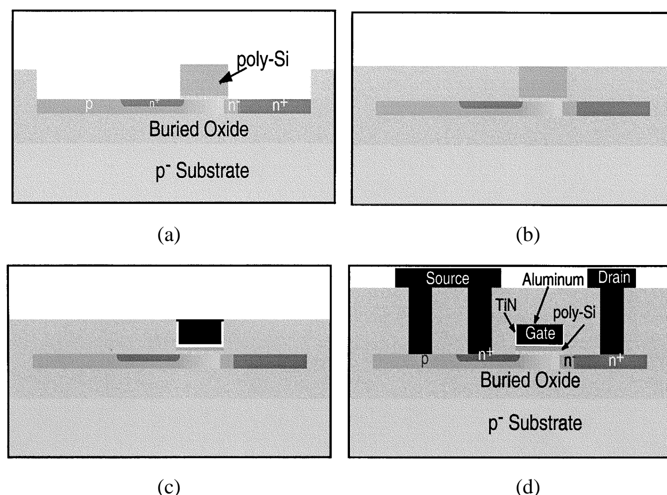

Fig. 1. Depiction of the fabrication process of the metal/polysilicon damascene gate on an RF SOI LDMOSFET. The process uses an oxide CMP step and a metal CMP step to produce the self-aligned gate.

II. Device Fabrication

The low-resistance gate was added to a 0.6 μm RF SOI LDMOSFET technology described in [7]. The fabrication process is sketched in Fig. 1. Following the front-end (after activation anneal), a 500 nm layer of low-temperature oxide was deposited. A CMP process was then used to planarize the oxide and reveal the surface of the polysilicon gates. Next the polysilicon was etched by RIE, creating a notch. The etch was timed to remove all but 50 nm of the polysilicon. Then 50 nm of titanium nitride (TiN) and 500 nm of aluminum (Al) were deposited by sputtering. The TiN layer was used to prevent spiking of the Al through the polysilicon. Finally, the process was finished with a two-level metal back-end. The metal-polysilicon gate as demonstrated here may not be manufacturable because the notch etch has no etch stop. The manufacturability of this structure could easily be improved by adding an etch stop layer to the gate stack, as was done in the CMOS process in [5].

III. Results and Discussion

The suitability of the metal/polysilicon damascene gate for RF power applications was evaluated by comparing the characteristics of an SOI LDMOSFET with a metal/polysilicon dam-

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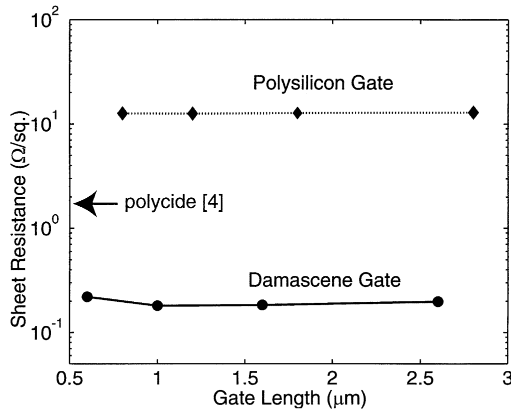

Fig. 2. Sheet resistance measured from Kelvin test structures of metal and polysilicon lines. The sheet resistance achieved by the metal/polysilicon damascene gate is 50 × lower than polysilicon and 5 × lower than WSi.

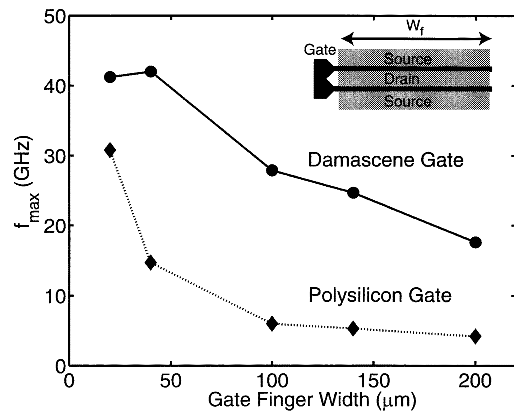

Fig. 3. $f_{\max}$ of co-processed SOI LDMOSFETs with metal/polysilicon damascene gates and polysilicon gates. The metal/polysilicon damascene gate greatly increases $f_{\max}$, especially for large finger widths. Devices had two gate fingers. V$_{dd}$ $= 3.6$ V and V$_{gs}$ was set for maximum $f_{\max}$.

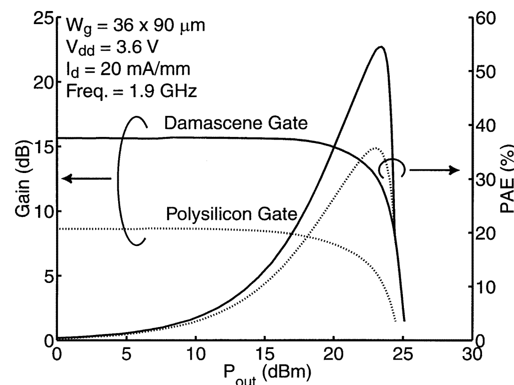

Fig. 4. Load-pull characteristics of 36×90 μm SOI LDMOSFETs with metal/polysilicon damascene gates and polysilicon gates. The improvement in $f_{\max}$ leads directly to an improvement in gain and peak PAE at 1.9 GHz.

ascene gate to a co-processed SOI LDMOSFET with a degenerately-doped polysilicon gate. The gate sheet resistance was measured using Kelvin test structures. Fig. 2 shows that the metal/polysilicon gate sheet resistance was 0.2 Ω/sq. for gate lengths down to 0.6 μm. This level of sheet resistance is 50 times lower than n$^+$ polysilicon and five times lower than the sheet resistance of the silicide in the state-of-the-art RF LDMOSFET process described in [4].

A model of $f_{\max}$ of a MOSFET can be used to estimate the impact of the gate sheet resistance on RF performance. To the first order, $f_{\max} = f_t\sqrt{R_o/R_g}$, where f_t is the short circuit current-gain cutoff frequency, R$_o$ is the output resistance, and R$_g$ is the gate resistance. A simple physical model for the gate resistance is $R_g = (1/3)(R_{sh}W_g/L_g)$, where R_{sh} is the gate sheet resistance, W_g is the gate width, L_g is the gate length, and the 1/3 term accounts for the distributed nature of gate resistance. Using this model and the measured gate sheet resistances given above, and assuming that the use of the damascene gate affects only the gate sheet resistance, the metal/polysilicon damascene gate device is predicted to have an $f_{\max}$ that is 7.1 × greater than that of the polysilicon gate device and 2.2 × greater than that of a state-of-the-art silicide gate device.

The gate's suitability for RF applications was studied by measuring the S-parameters as a function of the gate finger width. Measurements up to 20 GHz were carried out. The effect of the pads were de-embedded using on-wafer open test structures. The test devices had two gate fingers (nominal $L_g = 0.6$ μm) and gate finger widths of between 20 μm and 200 μm. f_t and $f_{\max}$ were extracted from the S-parameters. f_t of the polysilicon gate devices was 18.4 GHz$\pm$1.1 GHz, and f_t of the damascene gate devices was 14.5 GHz$\pm$1.3 GHz, for all finger widths. The variation in f_t was due to wafer-to-wafer and within-wafer gate length variation, and there was no systematic dependence on the gate finger width.

$f_{\max}$ of the devices as a function of the gate finger width is shown in Fig. 3. $f_{\max}$ of the devices with metal/polysilicon damascene gates was significantly higher than $f_{\max}$ of the devices with polysilicon gates. For narrow gate fingers, the damascene gate devices had an $f_{\max}$ of greater than 40 GHz. $f_{\max}$ of the polysilicon gate devices rolled off with gate finger width due to their high gate sheet resistance, while $f_{\max}$ of the damascene gate devices decreased less significantly because of the low resistance of the metal/polysilicon gate. For devices with gate finger widths of between 100 μm and 200 μm, $f_{\max}$ of the metal/polysilicon damascene gate device is larger by a factor of nearly five, close to the 7.1 × increase estimated by the simple model above. The devices with fingers narrower than 100 μm have $f_{\max}$ increased by a lesser amount, and their performance may be limited by gate contact resistance in series with the gate sheet resistance.

The reduction in gate sheet resistance and the increase in $f_{\max}$ translated directly into improved RF power performance. Load-pull characteristics of 3.2 mm RF power cells are shown in Fig. 4. The cells have 36 fingers and a 90 μm finger width. They were measured using an ATN load-pull system at a frequency of 1.9 GHz, a V$_{dd}$ of 3.6 V, bias current of 20 mA/mm, and source and load matching networks set to maximize PAE. The SOI LDMOSFETs with metal/polysilicon gates had greatly increased gain, which significantly improved the peak PAE. The small-signal gain and peak PAE of 36 finger RF power cells with the two different gate types is shown in Fig. 5 for gate finger widths of between 20 μm and 200 μm. The use of the metal/polysilicon damascene gate greatly improves the gain and

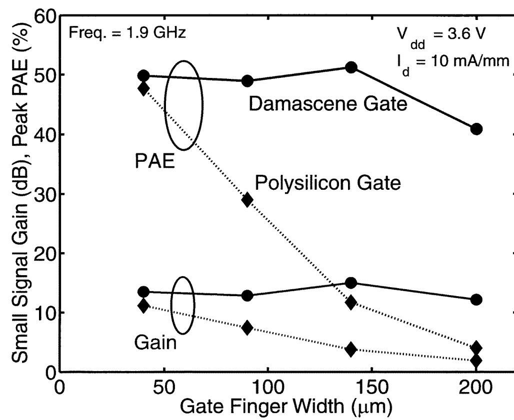

Fig. 5. Small signal gain and peak PAE for SOI LDMOSFETs versus gate finger width at 1.9 GHz. The use of a metal/polysilicon damascene gates allows excellent performance even with wide fingers.

peak PAE, especially for the large gate finger widths necessary for a high output power level. With a 140 μm gate finger width, peak PAE is improved from 12% to 52%.

IV. Conclusion

This letter describes a new metal/polysilicon damascene gate technology for RF power LDMOSFETs. The sheet resistance of the gate was 0.2 Ω/sq., 50 times lower than highly doped polysilicon and five times lower than polycides presently used in RF LDMOSFET processes. The suitability of this gate for RF power applications was demonstrated by fabricating SOI LDMOSFETs with the new gate as well as with standard polysilicon gates. The $f_{\max}$ and the peak PAE were significantly enhanced. For a gate finger width of 140 μm, $f_{\max}$ was improved from 5 GHz to 25 GHz, and the peak PAE at 1.9 GHz was improved from 12% to 52%. The metal/polysilicon damascene gate is demonstrated to be very effective for RF power applications. It may prove to be a critical technology for enhancing RF LDMOSFET performance in present applications, and for leading LDMOSFET technology to applications beyond 2 GHz.

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