Electrical Reliability of RF Power GaAs PHEMTs

A. A. Villanueva[1], J. A. del Alamo[1], T. Hisaka[2] and K. Hayashi[2]
[1] MIT, Room 39-415, Cambridge, MA 02139, USA, [2] Mitsubishi Electric, Itami, Hyogo, Japan

GaAs PHEMTs are broadly used in RF power applications for wireless systems. A major concern with these devices is their gradual degradation as a result of prolonged biasing at high voltages. Previous research has identified the drain side of the device as the region that sustains most of the damage [1], but other mechanisms involving charge modulation under the gate [2] have also been reported. Impact ionization and hot-carrier effects have been closely correlated with electrical degradation [1]-[4], but the details of the physics behind the degradation are not known. In this research, we carry out a systematic investigation of the degradation of RF power PHEMTs under prolonged electrical stress. By examining devices with different geometries as well as TLM test structures, our research isolates degradation mechanisms that separately affect each of the three main regions of the device: source, gate and drain.

In this study, a set of experimental, RF power PHEMTs (L_g = 0.25 um, W_g = 100 um; f_T ~ 40-50 GHz, $BV_{DG,off}$ ~ 12-15 V) were stressed at room temperature. A stressing scheme that keeps the impact ionization rate constant was utilized (constant I_D, constant $V_{DGo}+V_T$) [5]. A bias stepping scheme was employed to maximize the productivity of our experiments. During stressing, the devices were characterized at regular intervals.

Our results showed several forms of degradation. The main observations were that, after initial short transients, R_D increased while R_S decreased (Fig. 1), and V_T decreased producing a corresponding increase in I_{Dss} (Fig. 2). The changes in R_D, R_S and V_T look quite different from each other. Throughout many experiments, we have found them to be uncorrelated. This suggests the existence of at least three different degradation mechanisms that separately affect the three main regions of the device: the source, the intrinsic region underneath the gate, and the drain. The decrease in R_S is consistent with an increase in sheet electron concentration on the source. The small initial decrease of R_D may be due to a similar effect on the drain, but this is swamped by the subsequent long-term increase of R_D [2,4]. The changes in R_S and R_D were found to be permanent (not recoverable). In contrast, the negative shift in V_T was found to be recoverable after room-temperature storage at zero bias (Fig. 3). This has also been observed in [2] and [3] and is consistent with a charge trapping/detrapping mechanism localized underneath the gate (perhaps involving DX centers in the AlGaAs layers [2]).

To look further into the correlation between device degradation and impact ionization, we studied devices with varying lengths of the drain-gate gap (L_{rd}). Devices with longer L_{rd} (and hence higher $BV_{DG,off}$) did not experience significantly different R_D degradation rates, which is contradictory with an impact ionization-driven degradation model. On the other hand, devices with longer L_{rd} showed a slower V_T degradation rate (Fig. 4). This agrees with [2] and [3] where the V_T shift was attributed to hole trapping under the gate.

We also carried out experiments at varying stressing currents (Fig. 5). The degradation rate of R_D was found to be strongly superlinear in I_D (also inconsistent with an impact ionization-driven degradation mechanism). In contrast, the increase of $|V_T|$ steadily followed the increase in stressing I_D. For R_S, once its initial change was exhausted, no further changes were observed as a result of increasing I_D.

In order to get a clearer picture, we studied simpler TLM structures where the n+ GaAs cap has been removed but in which no gate has been fabricated. The TLMs showed two main degradation regimes (Fig. 6). Initially, the low-field resistance, R, decreases and the saturation current, I_{sat}, increases. At a later stage, R increases while I_{sat} remains constant. The first regime can be explained by an increase in n_s, which correlates with the reduction in R_S observed in the PHEMTs. The second regime suggests a degradation of the ohmic contact resistance. Through bias reversal experiments, we found that only one of the ohmic contacts is being damaged. Notably, all changes in R and I_{sat} are non-recoverable. The absence of a recoverable degradation mechanism in the TLMs, which have no gate, is consistent with our association of the recoverable V_T shift in the PHEMTs to the intrinsic region underneath the gate.

In conclusion, we have identified separate electrical degradation mechanisms in the source, gate and drain of RF power PHEMTs. We have found that impact ionization plays a much lesser role than previously thought. In contrast, hole trapping and drain contact resistance degradation are prominent. A previously unidentified increase in the sheet electron concentration has also been observed.

[1] Y. Tkachenko, et al., Proc. IEEE 1995 Microw. and Millim-Wave Monolith. Cir. Symp., 1995, p. 115. [2] C. Canali, et al., IRPS1995, p. 205. [3] G. Meneghesso, et al., IEEE TED, 47, p. 2, 2000. [4] R. E. Leoni and J.C. M. Hwang, IEEE TED, 46, p. 1608 1999. [5] S. D. Mertens et al, IEDM 2001, p.193.

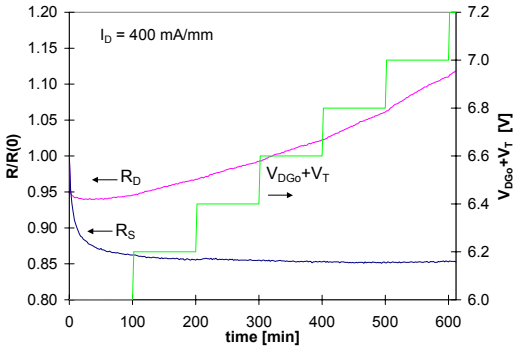

Fig. 1: Time evolution of R_D and R_S (normalized to their initial values), for a voltage step-stress experiment on a PHEMT at constant I_D = 400 mA/mm.

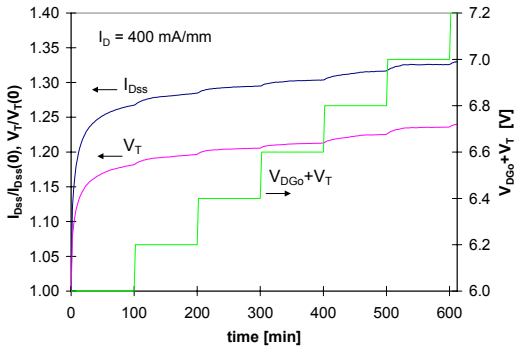

Fig. 2: Time evolution of V_T and I_{Dss} (normalized to their initial values), for a voltage step-stress experiment on a PHEMT at constant I_D = 400 mA/mm (same experiment as Fig. 1).

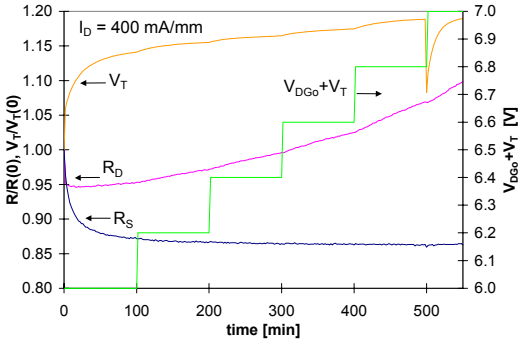

Fig. 3: Time evolution of R_D, R_S, and V_T (normalized to their initial values), for a voltage step-stress experiment at constant I_D = 400 mA/mm. After 500 minutes, stressing was paused for 4 days and then resumed.

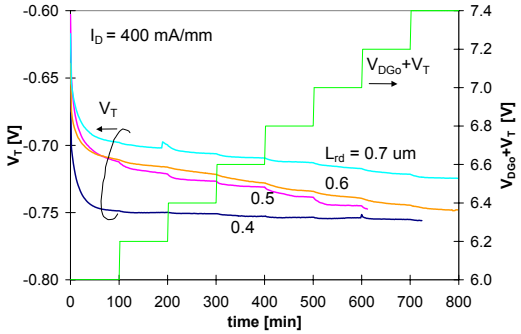

Fig. 4: Time evolution of V_T for a voltage step-stress experiments at constant I_D = 400 mA/mm, performed on four different PHEMTs with different values of gate-drain gap.

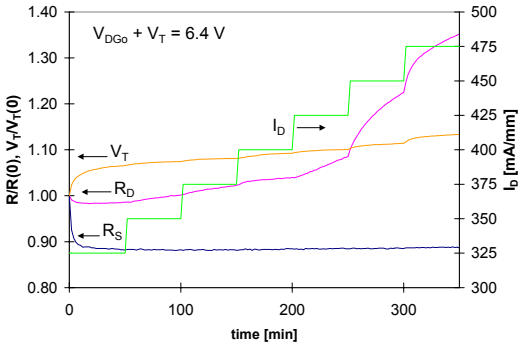

Fig. 5: Time evolution of R_D, R_S, and V_T (normalized to their initial values), for a current step-stress experiment on a PHEMT at constant $V_{DGo}+V_T$ = 6.4 V.

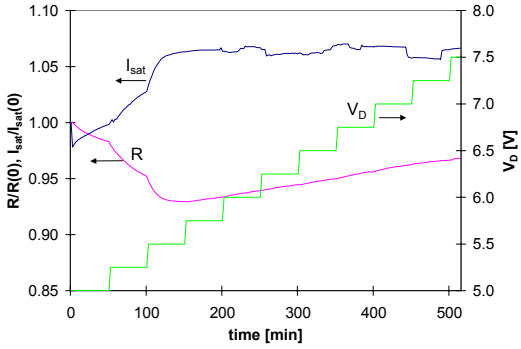

Fig. 6: Time evolution of normalized low-field resistance, R, and saturation current, I_{sat}, during step-stress experiment on a 2 um TLM. The intrinsic voltage drop across the TLM (V_D) is stepped as a function of time.