The impact of substrate surface potential on the performance of RF power LDMOSFETs on high-resistivity SOI

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Abstract

This paper presents an in-depth study of the effects of substrate surface potential on the RF power performance of LDMOSFETs on high-resistivity SOI. Substrate surface inversion and accumulation substantially degrade the RF power performance of these devices by providing an RF shunt between source and drain through the substrate surface. The degradation is most prominent under conditions of low gain, high frequency, and high power compression. The potential of HR-SOI for RF applications can only be realized by preventing the appearance of a continuous conducting path at the substrate surface. Under appropriate conditions, we demonstrate an RF LDMOSFET on HR-SOI with a peak PAE of 40 % at 7.2 GHz.

Introduction

High-resistivity SOI (HR-SOI) is an emerging technology platform for highly integrated RF systems [1]. The high-resistivity substrate enables the co-integration of high performance active and passive RF devices with digital CMOS technology. It is known, however, that an inversion layer beneath the buried oxide (BOX) increases the substrate's RF loss. This hurts the performance of passive devices, including inductors and transmission lines [2]. It has only recently been suggested that the inversion layer may also negatively affect the RF performance of active devices built on HR-SOI [3,4]. This is potentially very significant because it might negate the key advantage of HR-SOI for System-on-Chip applications.

In this work, we examine the effect of the substrate surface potential on the RF power performance of LDMOSFETs on HR-SOI. Our results also apply to other MOSFET designs on HR-SOI. We conclusively demonstrate that inversion and accumulation at the substrate surface (beneath the BOX) degrade the gain and power-added efficiency (PAE) of RF power MOSFETs on HR-SOI. We also show that the PAE degradation becomes worse under conditions of low gain, high frequency and under power compression. Excellent performance can be obtained if a continuous conductive layer is prevented from appearing at the substrate surface. Under appropriate conditions, we have measured a peak PAE of 40 % at 7.2 GHz.

Experimental Results

The LDMOSFETs utilized in this work were reported in [3]. A cross-section is shown in Fig. 1. The devices consist of a 20 nm gate oxide, a 0.6 μm long damascene gate, a 0.5 μm n^- drift length and an under-source body contact [5]. A p-type substrate with a resistivity of 2000 Ohm-cm was used. The SOI wafers have a top silicon layer of 4000 Å, and a 2000 Å BOX. The devices tested here have 36 fingers with a 40 μm unit finger width. In this technology, f_t = 18 GHz and BV_{off} > 20 V.

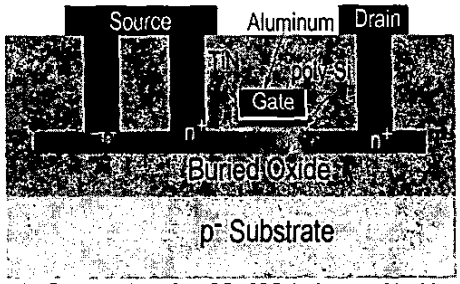

Figure 1: Cross-section of the LDMOS devices used in this work.

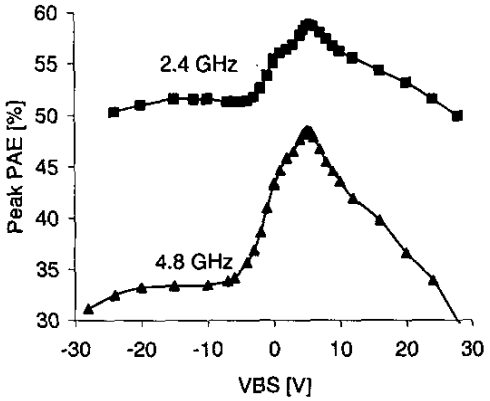

Figure 2: Peak PAE as a function of V_{bs} for 2.4 and 4.8 GHz for bias I_d = 10 mA and V_{ds} = 3.6 V, and fixed matching conditions.

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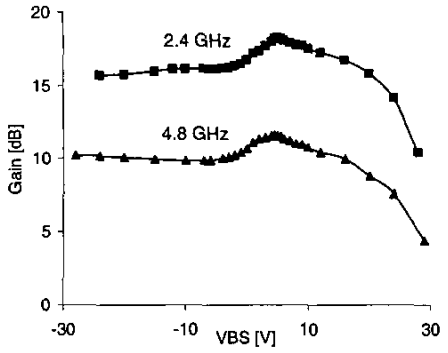

Figure 3: Gain vs. V_{bs} at low input power of P_{in} = -20 dBm at 2.4 and 4.8 GHz for bias I_d = 10 mA and V_{ds} = 3.6 V, and fixed matching conditions.

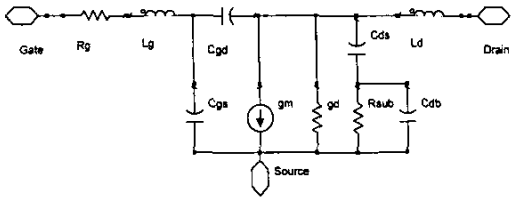

Figure 4: Small signal model topology. The drain RC network consists of the RC paths through the device body as well as well as through the BOX.

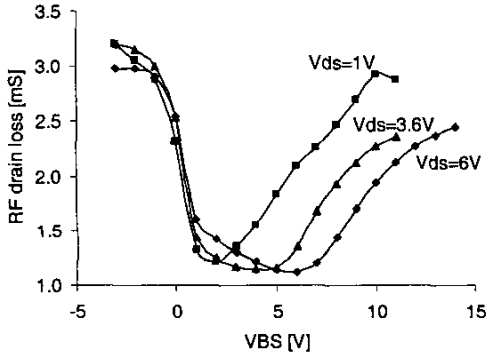

Figure 5: Real part of Y_{22} (drain loss) as a function of V_{bs} at 2.4 GHz for constant I_d = 10 mA. The 100 MHz (≈DC) value of Y_{22} has been subtracted from the measurements, to show only the increase in RF loss.

We investigated the impact of the substrate surface potential by using the back bias voltage with respect to the source (V_{bs}) [3]. Unless indicated otherwise, the device was biased with I_d=6.9 mA/mm and V_{ds}=3.6 V. We find that the substrate bias has an enormous effect on the RF power characteristics of these devices, particularly as the frequency increases (Figs. 2 and 3). With the substrate surface under depletion, the small-signal gain and the peak PAE are significantly higher than under accumulation or inversion. For the peak PAE, the difference can be as high as 7.5 % points at 2.4 GHz, and 15 % points at 4.8 GHz. By optimizing substrate biasing conditions, we measured a peak PAE of 60 % at 2.4 GHz, 50 % at 4.8 GHz and 40% at 7.2 GHz.

Small-Signal Data and Model

In order to understand these results, we have carried out S-parameter measurements as a function of V_{bs} and we have constructed a small-signal equivalent circuit model for the device (Fig. 4). This model includes a three-element RC network between drain and source that accounts for the RF losses through the BOX and the substrate. We find that at 2.4 GHz and for all values of V_{bs}, the losses through this RC network dominate the loss through the output conductance g_d. We also find that there is a large impact of V_{bs} on the RF drain loss into the substrate (Fig. 5). The RF drain loss is defined as $Re\{Y_{22}[2GHz] - Y_{22}[100MHz]\}$. As V_{bs} increases above -1 V, the RF drain loss decreases. At higher values of V_{bs}, it achieves a minimum value and then increases again. The value of V_{bs} at which the minimum loss is obtained depends on the value of V_{ds}: the higher V_{ds}, the higher the optimum V_{bs}.

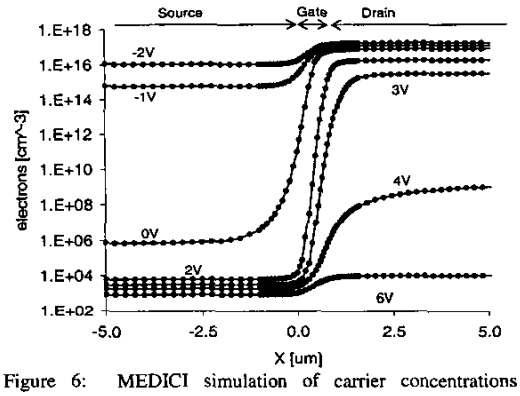

Figure 6: MEDICI simulation of carrier concentrations underneath the BOX for various V_{bs} (V_{gs} = 2 V, V_{ds} = 3.6 V).

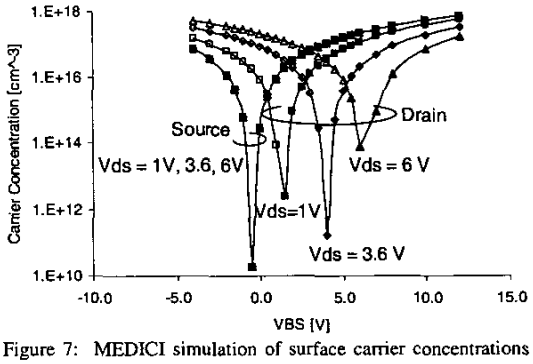

Figure 7: MEDICI simulation of surface carrier concentrations underneath the BOX for various V_{ds} (V_{gs} = 2 V), on the source and drain side of the device. Electrons shown as open, holes as solid shapes.

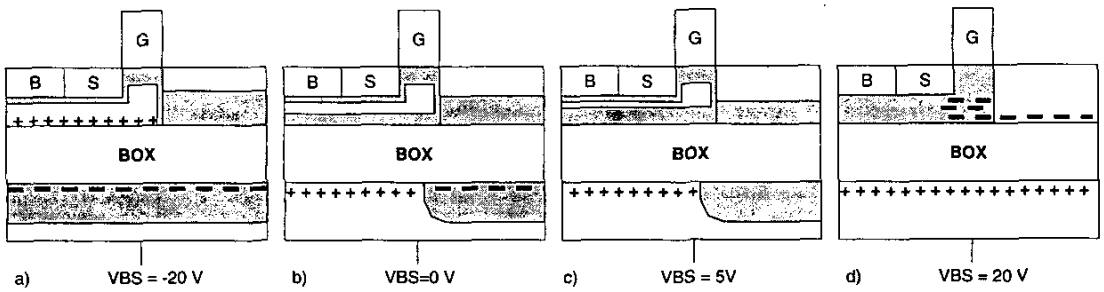

Figure 8a-d: BOX electrostatics as a function of V_{bs}. For large and negative V_{bs} (a), a surface inversion layer of electrons exists underneath the entire device. At intermediate voltages, the substrate under the source goes into accumulation (b), and at higher values of V_{bs} the substrate under the drain goes into depletion (c). For even higher values of V_{bs}, an accumulation layer of holes is formed underneath the entire device (d). On the device layer, body depletion takes place as V_{bs} increases, eventually flooding the body under the gate with electrons (d). Depletion regions are shown in gray, charge layers as + or –.

We also carried out MEDICI simulations of the electrostatics of this device. Fig. 6 shows the carrier concentrations along the substrate surface beneath the BOX. Fig. 7 shows the carrier density under the source and drain for different V_{ds}, and Fig. 8 depicts an overall picture of the substrate surface electrostatics. For large and negative V_{bs}, the substrate surface beneath both the source and the drain is inverted, i.e., an electron inversion layer is present everywhere (Fig. 8a). This results in an electrical short at high frequencies. For large and positive V_{bs}, the substrate surface is accumulated everywhere (Fig. 8d) and a conducting path shunting source and drain also is formed. In both situations the drain loss is high and the RF gain and the PAE are therefore low. At intermediate voltages (Figs. 8b,c), the substrate surface transitions from inversion, through depletion and into accumulation. As V_{bs} increases, the substrate underneath the source makes these transitions ahead of the drain by about V_{ds}. The lowest drain loss and maximum PAE are expected to occur when the substrate surface beneath the source is accumulated but beneath the drain still is depleted (Fig. 8c).

Discussion

The simulation results of Fig. 7 are in excellent agreement with the experimental data shown in Fig. 5. We see in Fig. 5 that the drop in drain loss at $V_{bs} \approx$ -1 V is independent of V_{ds}. This should be the case, since this drop is expected when the inversion layer under the source is eliminated. In the MEDICI simulations (Fig. 7), we find this to occur at around Vbs ≈ -0.5V. This value is independent of V_{ds}.

For a BOX structure, minimum RF loss from the silicon layer into the substrate occurs at flatband. The difference between the flatband voltage of the BOX under the source and drain will be equal to the potential difference, $\Delta\Phi_B$, in the materials used (n- vs. p-Si) plus the difference in the source and drain potential under bias, V_{ds}. Therefore, the drain side will have a flatband voltage greater than the source side by $\Delta\Phi_B+V_{ds}$. This is seen in the simulations shown in Fig. 7. The consequence of this is that as V_{ds} increases, the value of V_{bs} at which the minimum loss is seen to occur shifts to higher values of V_{bs}. The location of these minima in the measured RF loss in Fig. 5 is in excellent agreement with the flatband voltage predicted in the simulations. Regarding the RF power measurements, MEDICI predicts that for a V_{ds} of 3.6 V, flatband occurs at about $V_{bs} \approx$ 4.5 V. This is also in good agreement with the optimum value of V_{bs} in the RF power data of Figs. 2 and 3.

Our analysis, so far, does not explain why the behavior of peak PAE and gain (Figs. 2 and 3) is rather different with the substrate surface in accumulation and inversion. In inversion (V_{bs} < -1 V), the peak PAE settles to a constant value, while in accumulation (V_{bs} > 6 V for V_{ds} = 3.6 V), the peak PAE drops the higher V_{bs} becomes. This can be understood by examining the impact of V_{bs} on the DC characteristics of the LDMOSFET.

As V_{bs} sweeps from -20 V to +20 V, we find that the subthreshold characteristics (Fig. 9) and the output conductance (Fig. 10) markedly degrade. This is indicative of a general worsening of short-channel effects as V_{bs} becomes positive and an electron inversion/accumulation layer is induced at the bottom of the device layer underneath the gate and the drain. An important consequence of this is that g_m drops precipitously for large and positive V_{bs} (Fig. 11), as the gate has increased difficulty in modulating the new deep lying electron conducting path between source and drain. This translates onto a shrinking small-signal RF gain and a drop in peak PAE, as seen in Figs. 2 and 3, respectively.

Substrate surface inversion and accumulation affects linear and saturated power amplifiers in different ways. Experimentally we find that the prominent peak in PAE that appears at intermediate values of V_{bs} occurs only under relatively high

compression conditions. This is seen in Fig. 12 which plots PAE vs. V_{bs} for different P_{out} levels at 4.8 GHz. It is clear that for sufficiently low power levels, the peak in PAE disappears, that is, the status of the substrate surface has no effect on PAE. This result actually makes good sense. Under conditions in which the gain is high, PAE is approximately given by PAE = P_{out}/P_{dc}. Since, for low power levels, I_d approaches the DC value, it then follows that for constant P_{out}, PAE is independent of V_{bs}.

The PAE dependence on V_{bs} arises in fact under conditions in which PAE depends on the gain. This happens when the gain is not high, such as around compression and also at high frequencies. Hence, when using HR-SOI, the substrate surface status is a crucial consideration in non-linear or saturated power applications and at high frequencies. Linear applications are also impacted by V_{bs} but in a different way. In these, it is the small-signal gain that is most prominently affected by V_{bs} (Fig. 3).

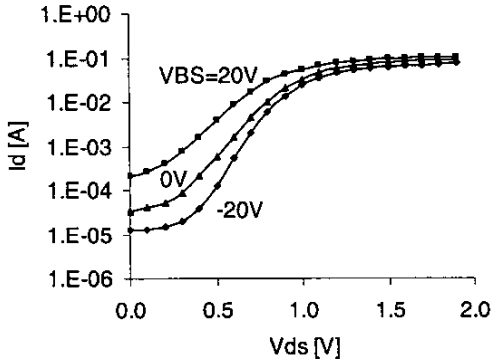

Figure 9: Subthreshold characteristics for different V_{bs} at V_{ds} = 3.6 V. Short channel effects and leakage become more

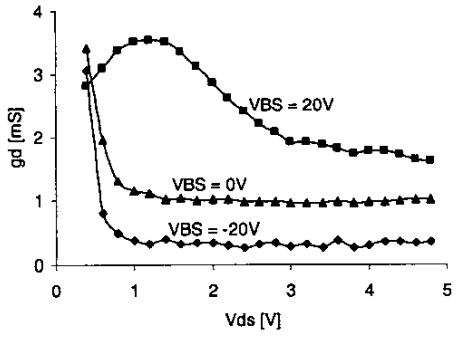

Figure 10: Output conductance for I_d = 10 mA for different V_{bs}.

References
[1] T. Matsumoto et al., IEDM p. 663, 2002.
[2] A. Reyes et al., IEEE MTT Vol. 43, No 9, p. 2016, 1994.
[3] J. Fiorenza et al., IEDM p. 463, 2002.
[4] V. Kilchytska et al, IEEE EDL Vol. 24, No 6, p. 414, 2003
[5] J. Fiorenza et al., IEEE TED Vol. 49, No 4, p. 687, 2002.

Conclusion

We have investigated the impact of the substrate surface potential on the RF power performance of LDMOSFETs on HR-SOI. We conclusively demonstrate that surface inversion or accumulation has a very large deleterious influence on the LDMOSFET's RF power performance, particularly at high frequencies and under power compression conditions. Through appropriate substrate bias tuning, excellent performance can be realized. We have measured a peak PAE of 40 % at 7.2 GHz. This work is important for understanding the optimization of RF power devices on SOI, and to demonstrate that substrate surface effects must be included in the modeling of RF MOSFETs on HR-SOI. Additionally, this work clearly shows that substrate surface inversion or accumulation must be dealt with to fully realize the potential of HR-SOI for RF applications.

Acknowledgements

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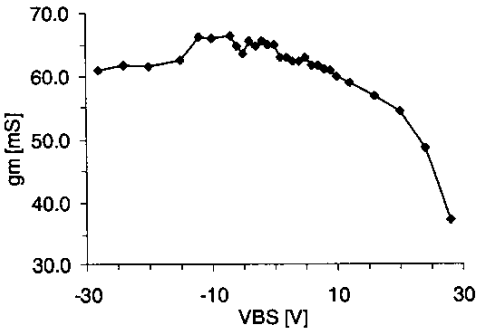

Figure 11: Transconductance vs. V_{bs} for I_d = 10mA. For high V_{bs}, g_m drops as the body shorts the drain to the source.

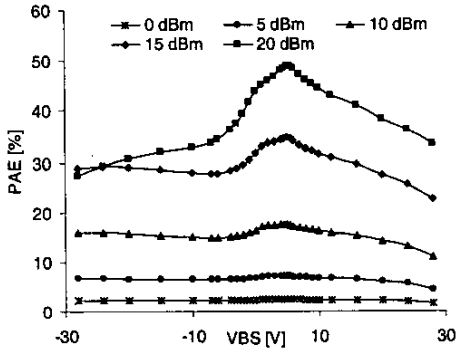

Figure 12: PAE vs. V_{bs} for different levels of output power (0 to 20 dBm) at 4.8 GHz. The device was biased at I_d = 10 mA and V_{ds} = 3.6 V for all V_{bs}.