Electrical Degradation Mechanisms of RF Power GaAs PHEMTs

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Abstract

In this research, we have carried out a systematic investigation of the electrical degradation of RF power PHEMTs. By examining devices with different geometries as well as a variety of test structures, our research confirms previous observations of degradation under the *gate* of the device. We have also identified for the first time a mechanism that affects the *source*. Additionally, we convincingly show that impact ionization (II) is not directly responsible for *drain* degradation. Instead, we find that a hot-electron (HE)-induced chemical reaction at the surface of the drain, coupled with contact degradation appear to be the mechanisms responsible for the drain damage.

1. Introduction

GaAs PHEMTs are widely used in RF power applications. A major concern with these devices is their gradual degradation under prolonged high-voltage biasing. Two distinct degradation phenomena have been identified: charge modulation occurring under the gate [1] and more critically, drain resistance degradation [2-4]. This is often attributed to II (though the detailed mechanisms have not been spelled out) or HE trapping in the passivation layer over the extrinsic drain [3, 5, 6]. The latter explanation appears unconvincing because surface Fermi-level pinning largely screens out the electrical properties of the semiconductor from the charge state of the insulator. Other HE-related mechanisms (such as interface trap creation, as described in [4]) have been proposed, but these have not been widely investigated in PHEMTs. The confusion about the physical origin of R_D degradation prevents the development of an effective solution to this problem.

2. Experimental

In this study, a set of experimental, double-recessed PHEMTs (L_g = 0.25 μm, W_g = 100 μm; f_T ~ 40-50 GHz, $BV_{DG,off}$ ~ 12-15 V) were electrically stressed. Unless specified, our experiments took place in air and at 300K. A stressing scheme that keeps II constant was utilized (constant I_D, constant $V_{DGo}+V_T$) [7]. A bias-stepping scheme was employed to maximize productivity. During stressing, the devices were characterized at regular intervals using a benign but comprehensive test suite [8], [9]. We also examined special transmission-line model (TLM) structures, which will be described in Section 4.

3. Results and Discussion: PHEMTs

Our results showed several forms of degradation in PHEMTs, most significantly in R_D, R_S, and V_T. After initial short transients, R_D increased (Fig. 1), R_S decreased (Fig. 1), and V_T shifted negative (Fig. 2). The changes in R_S and R_D were found to be permanent (not recoverable), while ΔV_T was found to be recoverable after room-temperature storage at zero bias. The degradation of R_D tends to accelerate at higher bias voltages; while that of R_S saturates. During stressing, we also observed that II, as seen in the classical "bell-shaped" curve of I_G vs. V_{GS} (not shown), decreased [10]. These results suggest that there are at least three different degradation mechanisms taking place in each of the main regions of the device: source, gate and drain.

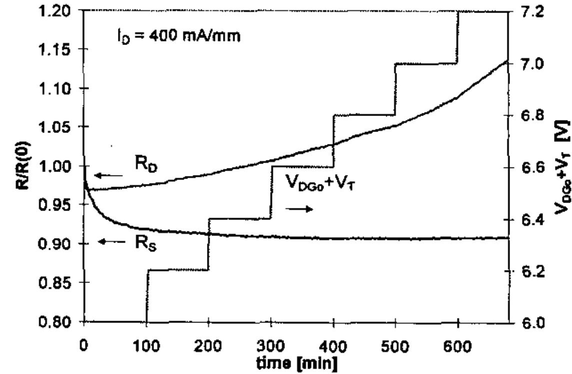

Fig. 1: Time evolution of R_D and R_S (normalized to initial values), for a voltage step-stress experiment on a PHEMT at constant I_D = 400 mA/mm.

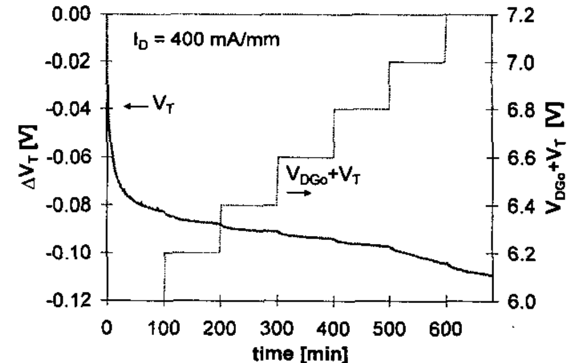

Fig. 2: Time evolution of ΔV_T for a voltage step-stress experiment on a PHEMT at constant I_D = 400 mA/mm (same experiment as Fig. 1)

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In PHEMT power applications, I_{max} is another important figure of merit. We defined I_{max} as the drain current at $V_{GS} = 0.8$ V, $V_{DS} = 1.0$ V. Fig. 3 shows the change in I_{Dss} (measured at $V_{GS} = 0$ V, $V_{DS} = 1.2$ V) and I_{max} during the same experiment as that of Figs. 1 and 2. We find that I_{Dss} increases in a manner that correlates directly with the shift in V_T, as shown in [9]. I_{max} also increases due to the V_T shift, but much less than I_{Dss}. Also, at higher stressing voltages, this increase becomes outweighed by another mechanism which causes I_{max} to decrease. This decrease correlates with the sharp increase in R_D seen in Fig. 1. This suggests that I_{max} is also affected by the same mechanism that causes the R_D degradation, as discussed in [11].

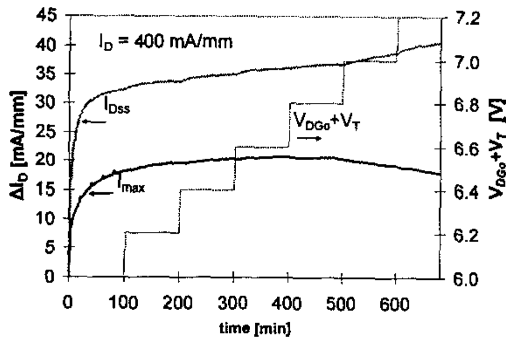

Fig. 3: Time evolution of ΔI_{Dss} and ΔI_{max} for a voltage step-stress experiment on a PHEMT at constant $I_D = 400$ mA/mm (same experiment as Fig. 1).

In order to investigate the role of II in device degradation, we examined the impact of stressing current. We found that even a small increase in I_D (Fig. 4) significantly accelerated the degradation (very dramatically for R_D, less so for R_S). Current step-stressing measurements showed that R_D degradation was strongly superlinear in I_D (Fig. 5), which is inconsistent with an II-related mechanism. For R_S, once its initial change was exhausted, no further changes were produced by increasing I_D (Fig. 5). In contrast, ΔV_T steadily followed the increase in stressing I_D (Fig. 6). I_{max}, like R_D, also displayed a superlinear dependence on I_D (not shown).

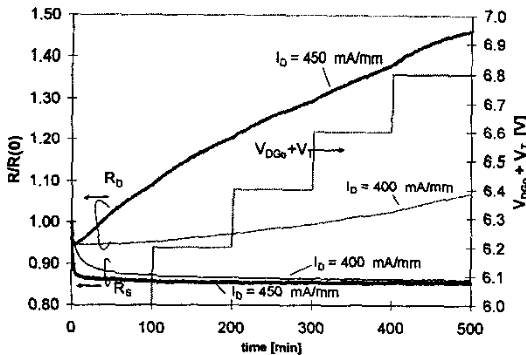

Fig. 4: Time evolution of R_S and R_D (normalized to initial values) for voltage step-stress experiments on identical PHEMTs, at constant values of I_D.

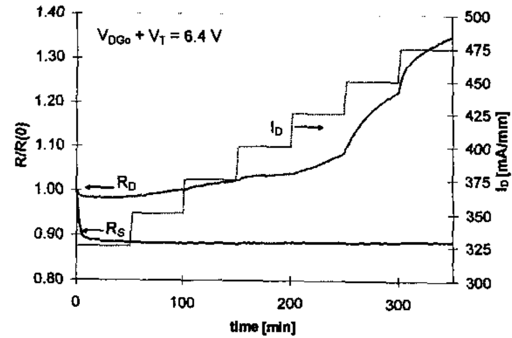

Fig. 5: Time evolution of R_D and R_S (normalized to initial values), for a current step-stress experiment on a PHEMT at constant $V_{DGo}+V_T = 6.4$ V.

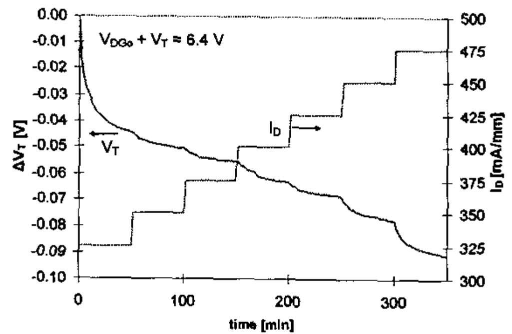

Fig. 6: Time evolution of V_T for a current step-stress experiment on a PHEMT at constant $V_{DGo}+V_T = 6.4$ V (same experiment as Fig. 4).

We also examined devices with varying lengths of the drain-gate gap (L_{rd}), and hence different $BV_{DG,off}$. We found that the extent of L_{rd} did not significantly affect the R_D degradation rates. This is also contradictory with an II degradation model. On the other hand, devices with longer L_{rd} showed a slower V_T degradation rate (Fig. 7). This agrees with [1], where ΔV_T was attributed to holes (generated by II) becoming trapped under the gate.

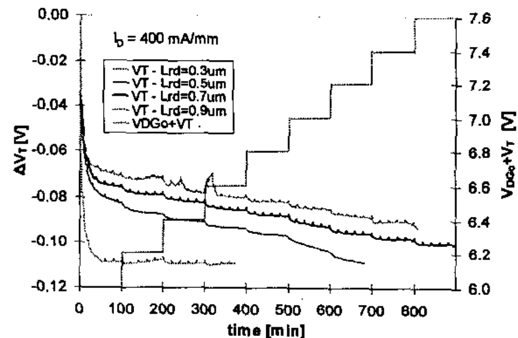

Fig. 7: Time evolution of ΔV_T for voltage step-stress experiments at constant $I_D = 400$ mA/mm, performed on four different PHEMTs with different values of gate-drain gap (Lrd).

The effect of atmosphere on PHEMT degradation was also investigated. We found that in N_2, R_D degradation slows down (Fig. 8), while neither R_S nor V_T are significantly

affected. The change in R_D therefore seems to be due to a surface effect in the extrinsic drain. A possible candidate is a HE-induced surface reaction accelerated by the presence of oxygen or moisture in the air [11]. This is different from the commonly-assumed mechanism of HE trapping in the SiN passivation layer [3, 5, 6].

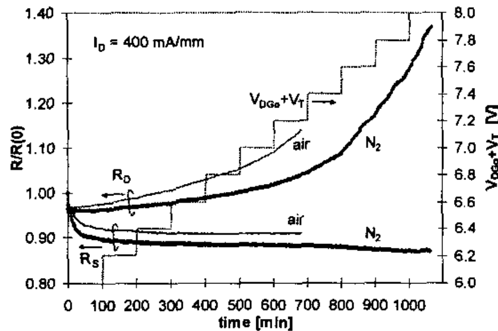

Fig. 8: Time evolution of R_S and R_D for voltage step-stress experiments at I_D = 400 mA/mm (one done in air, the other in N_2).

4. Results and Discussion: TLMs

In order to isolate all the mechanisms involved, we performed experiments on special-purpose TLM structures (Fig. 9). These are the same as PHEMTs, but without a gate. Thus, they are characterized by only two figures of merit—R, the low-field resistance, and I_{sat}, the high-field saturation current. The TLMs allowed us to study the impact of specific device features, such as the extent of exposed surfaces of the n+ GaAs layer (TLM5), the n-GaAs layer (TLM2), and the AlGaAs layer (TLM6). We also designed a "tapped" TLM (TLM4) that enabled us to separate the degradation on the source (anode) from that on the drain (cathode) of the TLM.

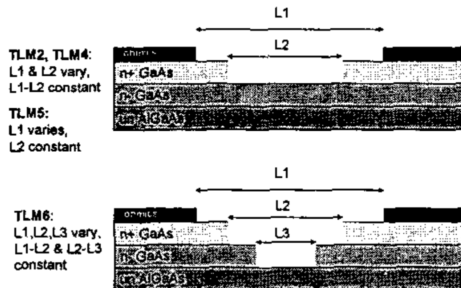

Fig. 9: Cross-sectional view of top layers of various types of TLMs fabricated. TLM2, TLM4, TLM5 are single-recessed; TLM6 is double-recessed. TLM4 is like TLM2, except it has a voltage "tap" in the center of the recessed region.

TLM4, like the other single-recess TLMs, showed two degradation regimes (Fig. 10). Initially, R decreases and I_{sat} increases. At a later stage, R increases while I_{sat} remains rather constant. The first regime can be explained by an increase in sheet-carrier concentration, n_s, while the second regime suggests ohmic contact degradation.

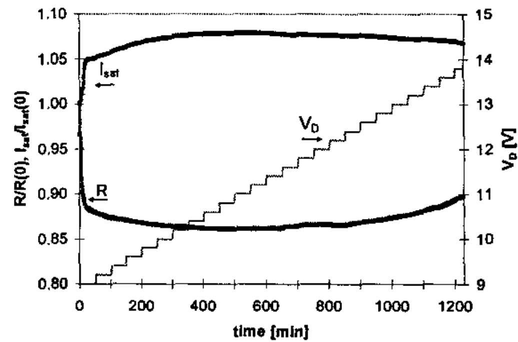

Fig. 10: Time evolution of normalized R and I_{sat}, for a step-stressing experiment on a 7 μm-long "tapped" TLM (TLM4). The intrinsic voltage drop across the TLM (V_D) is stepped as a function of time.

The voltage "tap" in TLM4 allowed us to separate R in its two components associated, respectively, with each half of the device. We call these the "source" and "drain" resistances (Fig. 11). This enabled us to conclude that the observed increase in n_s in the first regime was concentrated on the *source* side, and that it was mostly the *drain* contact that was degrading during the second regime.

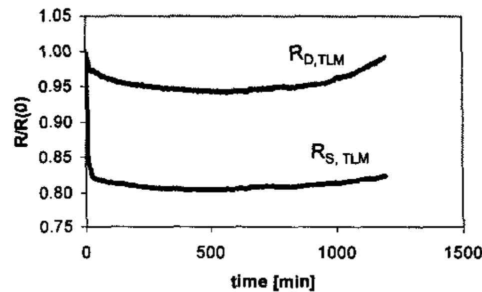

Fig. 11: Time evolution of $R_{D,TLM}$ and $R_{S,TLM}$, for a step-stressing experiment on a 7 μm-long "tapped" TLM (same experiment as Fig. 9).

A double-recessed TLM in which the AlGaAs layer is exposed (TLM6, Fig. 9) put in evidence a third degradation regime; at high voltages, I_{sat} starts to decrease while R continues to increase (Fig. 12). This suggests a degradation of n_s on the drain side of the TLM, associated with the exposed AlGaAs layer.

The advanced regimes of degradation are found to be alleviated in an N_2 environment (Fig. 12); this is also observed in the single-recessed TLMs. Also, all changes in R and I_{sat} in the TLMs (which have no gate) are non-recoverable. Light emission experiments have furthermore revealed a significant decrease in II in the TLMs as a result of stressing. All these observations bear a remarkable correlation with those in PHEMTs.

We also examined the effect of temperature on TLM degradation. Identical step-stressing experiments were performed on single-recessed TLMs (type TLM5) at three different temperatures (25, 75, and 125 °C) in a nitrogen environment. Before any stressing, it was confirmed that

increasing the temperature decreased the current and weakened II effects in these TLMs.

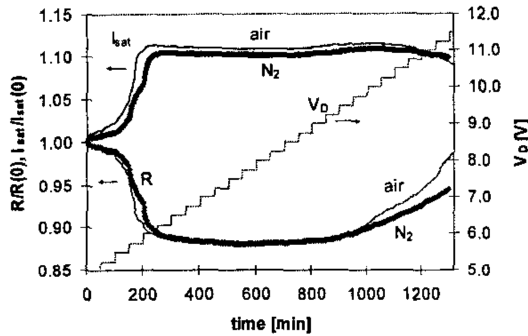

Fig. 12: Time evolution of normalized R and I_{sat} for step-stress experiments on 2.8 μm-long double-recessed TLMs (TLM6). One experiment was done in air, the other in N_2.

By monitoring the changes in R (Fig. 13) and I_{sat} (Fig. 14) in each case, we observed that all changes are accelerated at higher temperatures. This suggests that temperature-sensitive chemical reactions may play an important role in the degradation of the source and drain [11]. It also confirms that II (which has a negative temperature dependence, as shown in [12]) cannot explain the degradation seen in these devices.

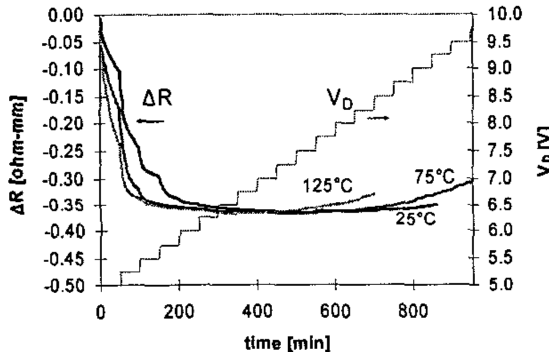

Fig. 13: Time evolution of ΔR for three 1.6 μm-long single-recessed TLMs (TLM5), step-stressed at different temperatures in N_2.

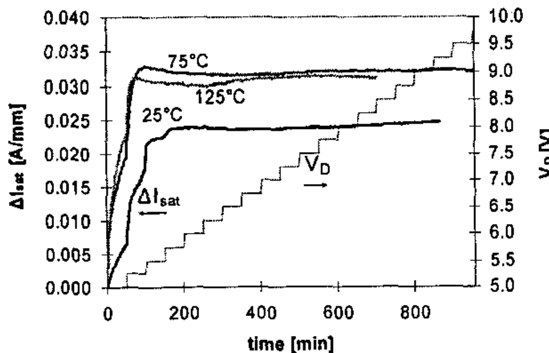

Fig. 14: Time evolution of ΔI_{sat} for three 1.6 μm-long single-recessed TLMs (TLM5), step-stressed at different temperatures in N_2 (same experiment as Fig. 13).

5. Conclusions

The combination of all experiments obtained in this work suggests a picture in which electrical degradation affects the source, gate and drain of the PHEMTs in different and uncorrelated ways. The decrease in R_S (never reported before) is due to an increase in n_s on the source, which is accelerated with temperature. The increase in R_D arises from a decrease in n_s on the drain, plus a degradation of the drain ohmic contact. Both of these drain-degrading mechanisms are surface-related and temperature-dependent, thus possibly indicating moisture-induced corrosion of the semiconductor surface. Specifically, damage could possibly be occurring on the AlGaAs layer adjacent to the gate (thereby leading to an n_s decrease), and on the n+ GaAs layer adjacent to the drain contact (leading to contact degradation). Only hot electrons can contribute to this process, since it takes over 1 eV for channel electrons to overcome the surface barrier. Finally, ΔV_T is consistent with hole trapping under the gate, as previously identified [1]. The understanding developed in this work should be instrumental towards developing effective solutions to these problems.

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