A Model for Hydrogen-Induced Piezoelectric Effect in InP HEMTs and GaAs PHEMTs

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***Abstract*—We have developed a model for the impact of the hydrogen-induced piezoelectric effect on the threshold voltage of InP HEMTs and GaAs PHEMTs. We have used two-dimensional (2-D) finite element simulations to calculate the mechanical stress caused by a Ti-containing metal gate that has expanded due to hydrogen absorption. This has allowed us to map the 2-D piezoelectric charge distribution in the semiconductor heterostructure. We then used a simple electrostatics model to calculate the impact of this piezoelectric polarization charge on the threshold voltage. The model explains experimental observations of hydrogen-induced threshold voltage shifts, both in InP HEMTS and in GaAs PHEMTs. It also suggests ways to mitigate the hydrogen sensitivity of these devices.**

***Index Terms*—HEMT, hydrogen (H), InP, piezoelectric effect, reliability.**

I. Introduction

HYDROGEN (H) degradation has been identified as a serious reliability concern in III-V FETs in general and InP HEMTs in particular [1]. In applications, demanding hermetically-sealed packaging, such as satellite or fiber-optic systems, exposure occurs when H out-gasses from the packaging material and becomes trapped inside the package cavity. With enough time, H diffuses into the transistor and alters its electrical characteristics eventually leading to parametric module failure.

Recent research has shown that among other effects, H exposure results in the formation of TiH_x in Ti/Pt/Au gates commonly used in III-V FETs [2]. This produces compressive stress in the gate, which generates a tensile stress in the heterostructure underneath. The resulting piezoelectric polarization charge causes a threshold voltage shift ΔV_T.

The few reports of the sign and magnitude of ΔV_T in InP HEMTs and GaAs PHEMTs that have been published seem contradictory (all devices have Ti/Pt/Au gates). While reports on [011]-oriented GaAs PHEMTs indicate a positive ΔV_T[3], [011]-oriented InP HEMTs have been found to display positive [4], negative [3], and even negligible V_T shifts [5]. When all the data are graphed together, however, a compelling picture emerges (see Fig. 1). It appears that for GaAs PHEMTs, ΔV_T is always positive and increases as the gate length is reduced. However, no data exists for long devices. For long gate length InP HEMTs, ΔV_T is negative and increasing in magnitude with decreasing L_g. At a certain L_g, however, there is a sign reversal and H-induced ΔV_T becomes positive. For shorter devices, ΔV_T increases.

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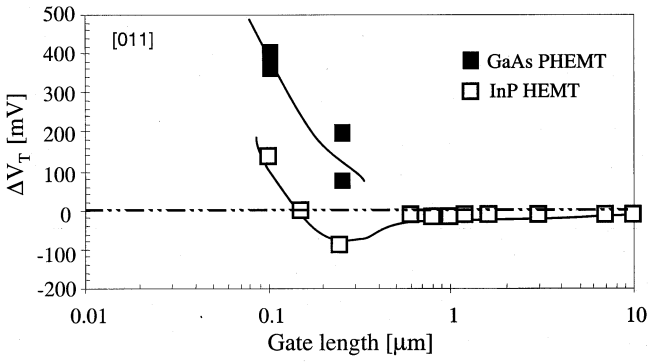

Fig. 1. Reports of ΔV_T caused by hydrogen degradation as a function of gate length for InP HEMTs and GaAs PHEMTs with gates oriented along the [011] direction [2]–[5].

In this work, we present a model for H-induced piezoelectric effect in InP HEMTs and GaAs PHEMTs that explains the peculiar behavior of ΔV_T shown in Fig. 1. Our model sheds light on the key parameters of the problem and provides design guidelines for minimizing H sensitivity of these devices. This paper expands on the work presented in [6].

II. Model

Our modeling approach involves:

1) performing two-dimensional (2-D) mechanical stress simulations of the device structure;
2) computing the resulting piezoelectric charge in the semiconductor heterostructure;
3) estimating its effect on V_T.

First, a 2-D finite-element simulation tool, ABAQUS, was used to calculate the mechanical stress in the device layer structure introduced by an expanding Ti/Pt/Au gate caused by the formation of TiH_x. We modeled the expansion of the Ti layer as a thermal expansion of the bottom layer of the gate stack (this approach neglects the second-order coupling between the electrical field in the semiconductor and its displacement). The mechanical properties of the materials used in the simulations can be found in Table I. We used a finer mesh near the surface of the heterostructure and directly under the gate to provide a detailed picture of the mechanical stress where it has the biggest impact on V_T. We exploited the symmetry of the structure and we only simulated half of it. The center of the gate was fixed, so no displacement can take place in the horizontal direction for any point in the heterostructure underneath the center of the gate. The mesh extends by 20 μm in the vertical direction and 50 μm in the horizontal direction, from the center of the gate. The structure was fixed mechanically at the bottom and on the

TABLE I
MECHANICAL MATERIAL CONSTANTS USED IN THIS STUDY

Material	Young Modulus [GPa]	Poisson's ratio
Ti	116 [12]	0.32 [12]
Pt	168 [12]	0.38 [12]
Au	78 [12]	0.44 [12]
$In_{0.53}Ga_{0.47}As$	100 [11]	0.25 [11]
$In_{0.52}Al_{0.48}As$	96 [11]	0.26 [11]
$Al_{0.24}Ga_{0.76}As$	73 [11]	0.23 [11]
$In_{0.22}Ga_{0.78}As$	111 [11]	0.24 [11]
SiN	320 [12]	0.32 [12]

side far away from the gate. This is a fair assumption as the device is surrounded by material that is not expanding. There are 16 000 mesh nodes in the semiconductor heterostructure and 6400 mesh nodes in the gatestack and passivation layer. The end result of this simulation is the atomic displacements u_x and u_z perpendicular and parallel to the gate, respectively.

In our second step, we use u_x and u_z to compute the polarization vector field $\vec{P}$ and the polarization charge distribution $\rho_{\rm pol}$ throughout the device [7]. The x and z components of the polarization vector for a III-V semiconductor with a [011] surface are, respectively, given by

$$P_x = -\mu d_{14}\left(\frac{du_x}{dz} - \frac{du_z}{dx}\right) \tag{1}$$

$$P_z = -\mu d_{14}\frac{du_x}{dx}. \tag{2}$$

In these equations, μ is the Voight average shear modulus and d_{14} the piezoelectric constant of the material [8]–[11]. The values of these constants are specific to each layer. For the ternary compounds studied in this work, μ and d_{14} were obtained by interpolation from the binaries (see Table II).

The piezoelectric charge can be calculated using

$$\rho_{\rm pol} = -\nabla \cdot \vec{P}. \tag{3}$$

As discussed below, computing the piezoelectric charge is not essential to deriving ΔV_T. However, $\rho_{\rm pol}$, since it is a scalar, provides for a compact way of visualizing and understanding the impact of stress on the electrostatics of the problem.

The final step is to compute the effect of the polarization charge on V_T. For simplicity, we assume a one-dimensional (1-D) model in which ΔV_T is calculated at the center of the gate. This is a fair assumption particularly if V_T is experimentally extracted in the linear regime, as is commonly done [2], [4]. Symmetry arguments show that at the center of the gate, the component of the polarization vector parallel to the gate P_x will be zero, hence we are only concerned with P_z, its component perpendicular to the gate. In our V_T model, we assume

TABLE II
PIEZOELECTRIC MATERIAL CONSTANTS USED IN THIS STUDY. THE TERNARY COMPOUNDS ARE LINEARLY INTERPOLATED IN BETWEEN THE BINARIES

Material	d_{14} [C/dyne]	μ [10^{10} dyne/cm^2]
GaAs	3.36 [8]	48.6 [11]
InAs	1.14 [9]	31.4 [11]
AlAs	5.00 [10]	44.2 [11]

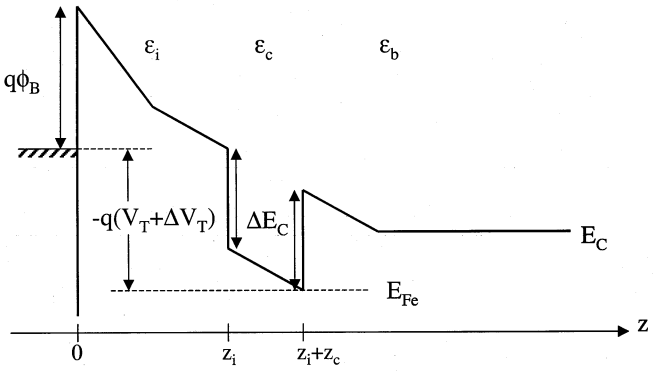

Fig. 2. Energy band diagram at threshold at the center of the gate of a HEMT, perpendicular to the gate. The buffer-substrate interface is unpinned.

that the inversion layer at threshold appears at the bottom of the channel, next to the buffer-channel interface as is the case of double-heterostructure HEMT (it is easy to adapt the theory for other device designs).

We first develop a 1-D model for V_T for the case in which the Fermi-level is unpinned at the heterostructure-substrate interface. Looking at the band diagram in Fig. 2, we can see that in this situation

$$q\phi_B - q(V_T + \Delta V_T) = E_C(0) - E_C(z_i + z_c) + \Delta E_C \tag{4}$$

where

- V_T threshold voltage without any polarization charge;
- ΔV_T threshold voltage shift induced solely by the polarization charge;
- ϕ_B Schottky barrier height of the gate metal;
- ΔE_C discontinuity in the conduction band between channel and buffer;
- E_C energy level of the conduction band edge.
- z_i, z_c thicknesses of the insulator and the channel layer, respectively, as shown in Fig. 2.

Poisson's law states

$$\frac{d\left[\varepsilon(z)\boldsymbol{\mathcal{E}}(z) + P_z(z)\right]}{dz} = \rho(z) \tag{5}$$

where

- $\rho(z)$ Coulombic charge present in the structure;
- $\boldsymbol{\mathcal{E}}(z)$ electric field;
- $\varepsilon(z)$ permittivity of the material.

The values of $\varepsilon(z)$ at the insulator, channel, and buffer layer are denoted by ε_i, ε_c, and ε_b, respectively.

We can integrate (5) from a point z_0 to z to find

$$\boldsymbol{\mathcal{E}}(z)=\frac{\varepsilon(z_0)\boldsymbol{\mathcal{E}}(z_0)+P_z(z_0)}{\varepsilon(z)}-\frac{P_z(z)}{\varepsilon(z)}+\frac{1}{\varepsilon(z)}\int_{z_0}^{z}\rho(z')dz'. \tag{6}$$

The conduction band energy difference between two points z_1 and z_2 in the structure now becomes

$$\begin{aligned}E_C(z_2)-E_C(z_1)=&q\int_{z_1}^{z_2}\boldsymbol{\mathcal{E}}(z')dz'\\ =&q\left[\varepsilon(z_0)\boldsymbol{\mathcal{E}}(z_0)+P_z(z_0)\right]\int_{z_1}^{z_2}\frac{dz'}{\varepsilon(z')}\\ &-q\int_{z_1}^{z_2}\frac{P_z(z')}{\varepsilon(z')}dz'\\ &+q\int_{z_1}^{z_2}\frac{1}{\varepsilon(z')}\left(\int_{z_0}^{z'}\rho(z'')dz''\right)dz'.\end{aligned} \tag{7}$$

In order to derive an expression for $V_T+\Delta V_T$, we select $z_0=\infty$, where $\boldsymbol{\mathcal{E}}(\infty)=0$ and $P(\infty)=0$, and $z_1=z_i+z_c$ and $z_2=0$. Then

$$\begin{aligned}E_C(0)-E_C(z_i+z_c)=&q\int_{z_i+z_c}^{0}\boldsymbol{\mathcal{E}}(z')dz'\\ =&-q\int_{z_i+z_c}^{0}\frac{P_z(z')}{\varepsilon(z')}dz'\\ &+q\int_{z_i+z_c}^{0}\frac{1}{\varepsilon(z')}\left(\int_{\infty}^{z'}\rho(z'')dz''\right)dz'.\end{aligned} \tag{8}$$

Plugging this in (4), we get

$$\begin{aligned}V_T+\Delta V_T=\phi_B-\frac{\Delta E_C}{q}&+\int_{z_i+z_c}^{0}\frac{P_z(z')}{\varepsilon(z')}dz'\\ &-\int_{z_i+z_c}^{0}\frac{1}{\varepsilon(z')}\left(\int_{\infty}^{z'}\rho(z'')dz''\right)dz'.\end{aligned} \tag{9}$$

Only one term on the right side of the equation is dependent on the piezoelectric charge. Then ΔV_T is given by

$$\Delta V_T=-\int_{0}^{z_i+z_c}\frac{P_z(z')}{\varepsilon(z')}dz'. \tag{10}$$

This result suggests that in the absence of Fermi-level pinning below the channel, the threshold voltage shift is only dependent on the piezoelectric charge between the gate and the channel.

If we assume that Fermi-level pinning takes place at the buffer-substrate interface, which is a fair assumption in III-V HEMTs, our model needs to be modified. The corresponding energy band diagram can be seen in Fig. 3. In this case, (4) still holds, but there is an additional constraint imposed by pinning at the bottom of the buffer:

$$\Delta E_C=E_C(z_i+z_c)-E_C(z_i+z_c+z_b)+q\phi_{BB} \tag{11}$$

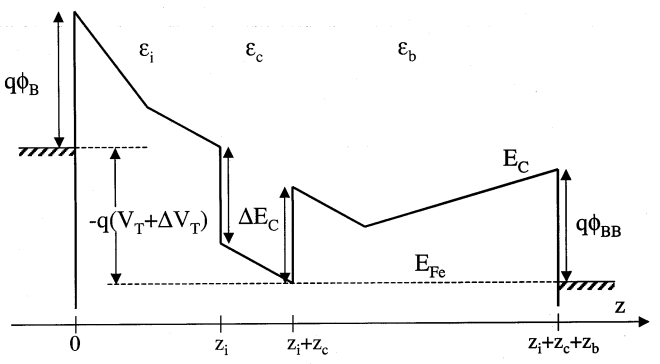

Fig. 3. Energy band diagram at threshold at the center of the gate of a HEMT, perpendicular to the gate. The Fermi-level at the buffer-substrate interface is pinned.

where z_b is the thickness of the buffer layer. We now apply (7) from $z_1=z_i+z_c$ to $z_2=0$, selecting $z_0=z_i+z_c+z_b$

$$\begin{aligned}E_C(0)-&E_C(z_i+z_c)\\ =&q\left[\varepsilon_b\boldsymbol{\mathcal{E}}(z_i+z_c+z_b)+P_z(z_i+z_c+z_b)\right]\\ &\times\int_{z_i+z_c}^{0}\frac{dz'}{\varepsilon(z')}-q\int_{z_i+z_c}^{0}\frac{P_z(z')}{\varepsilon(z')}dz'\\ &+q\int_{z_i+z_c}^{0}\frac{1}{\varepsilon(z')}\left(\int_{z_i+z_c+z_b}^{z'}\rho(z'')dz''\right)dz'.\end{aligned} \tag{12}$$

We also use (7) between $z_1=z_i+z_c$ to $z_2=z_i+z_c+z_b$ and substitute it in (11)

$$\begin{aligned}E_C(z_i+z_c)-&E_C(z_i+z_c+z_b)\\ =&q\left[\varepsilon_b\boldsymbol{\mathcal{E}}(z_i+z_c+z_b)+P_z(z_i+z_c+z_b)\right]\\ &\times\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{dz'}{\varepsilon(z')}-q\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{P_z(z')}{\varepsilon(z')}dz'\\ &+q\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{1}{\varepsilon(z')}\left(\int_{z_i+z_c+z_b}^{z'}\rho(z'')dz''\right)dz'\\ =&\Delta E_C-q\phi_{BB}.\end{aligned} \tag{13}$$

We can solve for $\varepsilon_b\boldsymbol{\mathcal{E}}(z_i+z_c+z_b)+P_z(z_i+z_c+z_b)$ in (13), plug it in (11), and this onto (4) to finally yield

$$\begin{aligned}V_T+\Delta V_T=&\phi_B-\frac{\Delta E_C}{q}\\ &-\int_{z_i+z_c}^{0}\frac{1}{\varepsilon(z')}\left(\int_{z_i+z_c+z_b}^{z'}\rho(z'')dz''\right)dz'\\ &+\int_{z_i+z_c}^{0}\frac{P_z(z')}{\varepsilon(z')}dz'-\frac{\int_{z_i+z_c}^{0}\frac{dz'}{\varepsilon(z')}}{q\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{dz'}{\varepsilon(z')}}\\ &\times\left[\Delta E_C-q\phi_{BB}+q\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{P_z(z')}{\varepsilon(z')}dz'\right.\\ &\left.-q\int_{z_i+z_c+z_b}^{z_i+z_c}\frac{1}{\varepsilon(z')}\left(\int_{z_i+z_c+z_b}^{z'}\rho(z'')dz''\right)dz'\right].\end{aligned} \tag{14}$$

Only two terms on the right-hand side are dependent on the piezoelectric charge. They are responsible for the shift in V_T. Hence

$$\Delta V_T = -\int_0^{z_i+z_c} \frac{P_z(z')}{\varepsilon(z')}dz' + \frac{\int_0^{z_i+z_c}\frac{dz'}{\varepsilon(z')}}{\int_{z_i+z_c}^{z_i+z_c+z_b}\frac{dz'}{\varepsilon(z')}}\int_{z_i+z_c}^{z_i+z_c+z_b}\frac{P_z(z')}{\varepsilon(z')}dz'. \quad (15)$$

Or in simpler terms

$$\Delta V_T = -\int_0^{z_i+z_c} \frac{P_z(z')}{\varepsilon(z')}dz + \frac{1}{z_b}\left(\frac{z_i}{\varepsilon_i}+\frac{z_c}{\varepsilon_c}\right)\int_{z_i+z_c}^{z_i+z_c+z_b} P_z(z')dz'. \quad (16)$$

In this simplification, we have used

$$\int_0^{z_i+z_c}\frac{dz'}{\varepsilon(z')} = \int_0^{z_i}\frac{dz'}{\varepsilon(z')} + \int_{z_i}^{z_i+z_c}\frac{dz'}{\varepsilon(z')} = \frac{1}{\varepsilon_c}\int_0^{z_i}dz' + \frac{1}{\varepsilon_c}\int_{z_i}^{z_i+z_c}dz' = \left(\frac{z_i}{\varepsilon_i}+\frac{z_c}{\varepsilon_c}\right). \quad (17)$$

and

$$\frac{\int_{z_i+z_c}^{z_i+z_c+z_b}\frac{P_z(z')}{\varepsilon(z')}dz'}{\int_{z_i+z_c}^{z_i+z_c+z_b}\frac{dz'}{\varepsilon(z')}} = \frac{\frac{1}{\varepsilon_b}\int_{z_i+z_c}^{z_i+z_c+z_b}P_z(z')dz'}{\frac{1}{\varepsilon_b}\int_{z_i+z_c}^{z_i+z_c+z_b}dz'} = \frac{1}{z_b}\int_{z_i+z_c}^{z_i+z_c+z_b}P_z(z')dz'. \quad (18)$$

For Fermi-level pinning far enough from the bottom of the channel, or for an unpinned substrate-buffer interface, this equation converges toward (10).

With our choice of axis and crystallographic orientation, P_z mostly has a negative value underneath the center of the gate. Because of this, it is simpler to focus on the behavior of $-P_z$, which is predominantly positive. If one ignores the differences in permittivity among the various layers, (16) can be rewritten as

$$\Delta V_T \approx \frac{z_i+z_c}{\langle\varepsilon\rangle}\left[\langle -P_z\rangle_{insulator+channel} - \langle -P_z\rangle_{\text{buffer}}\right]. \quad (19)$$

This suggests that ΔV_T is roughly proportional to the *difference* between the average of $-P_z$ above the channel and the average of $-P_z$ in the buffer layer underneath the channel. Because of this, all aspects of the heterostructure design are important, including the details of the buffer layer.

III. Results

As a model device (see Fig. 4), we have selected a double-heterostructure transistor with a 300 Å insulator layer and a 200 Å channel. The gate stack is made of 250 Å Ti/ 250 Å Pt/3000 Å Au. The device is covered by 600 Å of Si_3N_4. The InP HEMTs in this study have a $In_{0.48}Al_{0.52}As/In_{0.53}Ga_{0.47}As/In_{0.48}Al_{0.52}As$ heterostructure and the GaAs PHEMTs have a $Al_{0.24}Ga_{0.76}As/In_{0.22}Ga_{0.78}As/Al_{0.24}Ga_{0.76}As$ heterostructure.

A typical result of the 2-D finite-element simulations is shown in Fig. 5, which graphs the atomic displacements in the heterostructure of a 1-μm gate length InP HEMT (u_x on the left, u_z on the right). The results all have arbitrary units, as they are all linearly proportional to the amount of expansion of the Ti-layer. The expanding gate compresses the semiconductor in the extrinsic portion of the device away from the gate and down, while stretching and pulling up the material underneath. This atomic displacement information is used to calculate the corresponding piezoelectric charge distribution in the device (see Fig. 6), which exhibits the well known lobes that emanate from the edge of the gate.

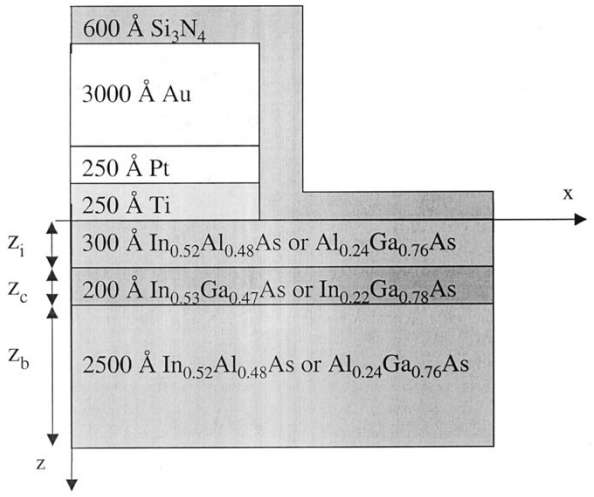

Fig. 4. Simulated device structures. Both the InP HEMT (first material in heterostructure) and GaAs PHEMT (second material in heterostructure) were simulated.

Our model for ΔV_T requires $-P_z$ at the center of the gate. This is shown in Fig. 7 for a 1 μm InP HEMT and GaAs PHEMT under identical stress conditions. The discontinuities in $-P_z$ at the channel boundaries occur because of the change in the material constants at the two heterointerfaces. It can be seen that for the same stress GaAs PHEMTs have a slightly larger piezoelectric polarization than InP HEMTs. This is due to the larger material constants of the different active layers in GaAs PHEMTs with respect to InP HEMTs.

The device gate length has a big impact on the piezoelectric charge distribution and the resulting P_z landscape. For an InP HEMT with a gate length of 0.3 μm, Fig. 8 shows the piezoelectric charge throughout the device structure (inset) and the resulting $-P_z$ directly underneath the center of the gate. In this case, the piezoelectric charge is large throughout the device structure. $-P_z$ decreases sharply with depth, as the polarization charge is large directly underneath the center of the gate. Therefore, the average of $-P_z$ above the bottom of the channel is significantly larger than the average of $-P_z$ below the channel, which results in a *positive* threshold voltage shift. The difference in sign of ΔV_T between this simulated result and the experimental observation on Fig. 1, can be explained by the fact that Fig. 1 contains observations on devices with different heterostructures from different authors, while our simulation work here is all based on a prototypical device sketched in Fig. 4.

For a long InP HEMT with a gate length of 6 μm (see Fig. 9), in contrast, the piezoelectric charge is almost negligible underneath the center of the gate. This causes $-P_z$ not only to be

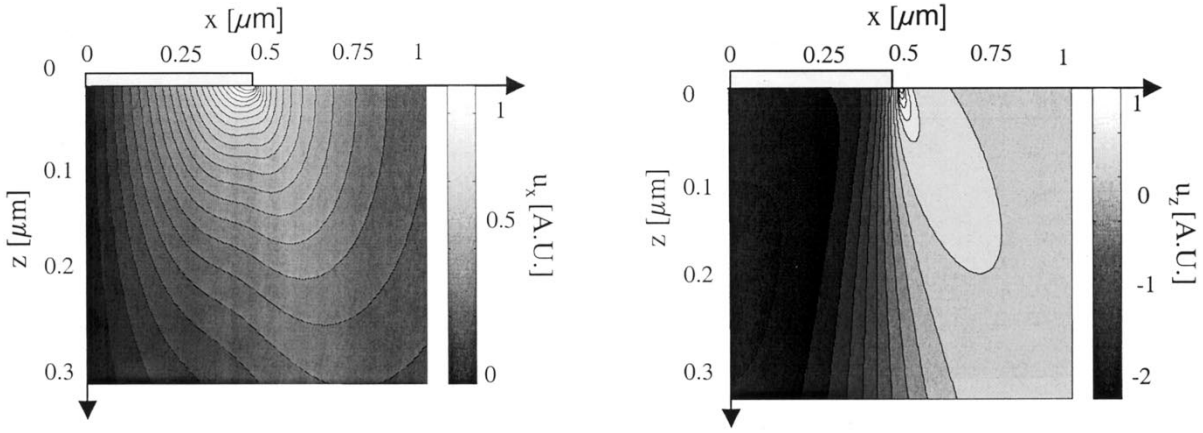

Fig. 5. Relative displacement of semiconductor heterostructure in directions parallel (left) and perpendicular (right) to the gate produced by an expanding gate in a 1-μm gate length HEMT. Calculations by ABAQUS. Only half of the structure is simulated and shown here.

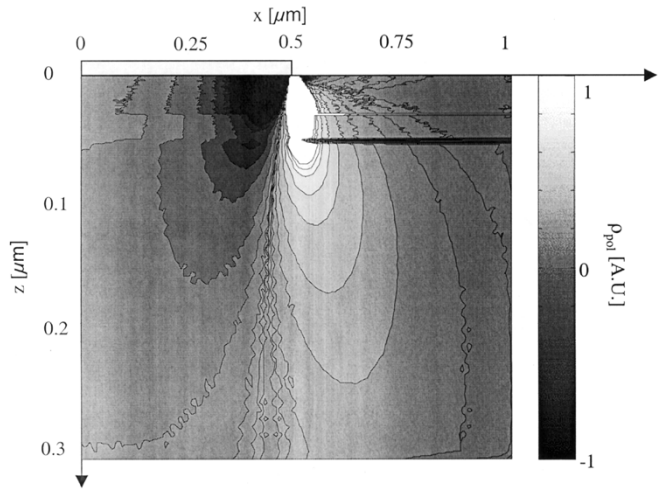

Fig. 6. Relative 2-D piezoelectric charge distribution in the heterostructure of a 1-μm HEMT stressed by an expanding gate. Only half of the structure is simulated and shown here.

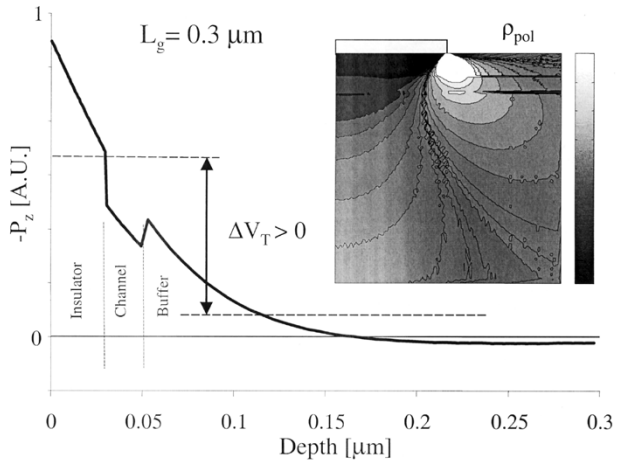

Fig. 8. Piezoelectric polarization vector in the direction perpendicular to the gate $-P_z$ for an InP HEMT with 0.3 μm gate length. Inset shows the corresponding piezoelectric charge distribution.

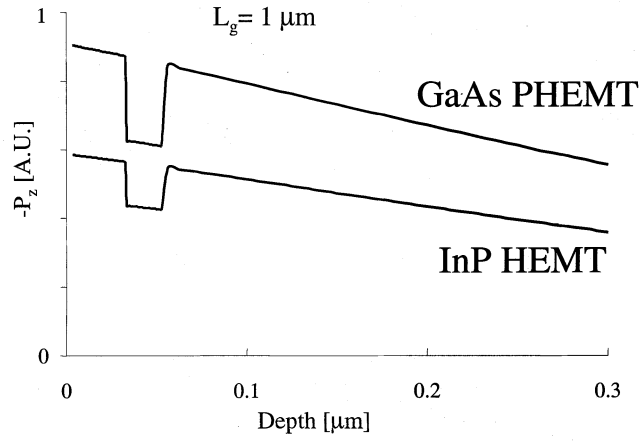

Fig. 7. Piezoelectric polarization vector in the direction perpendicular to the gate $-P_z$ for an InP HEMT and a GaAs PHEMT with 1-μm gate length.

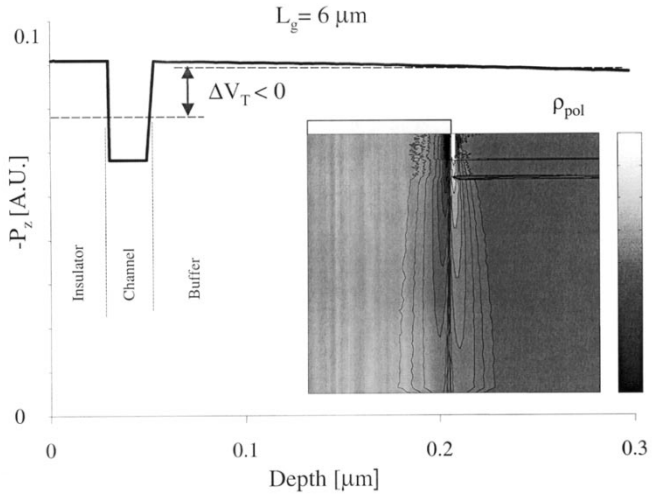

Fig. 9. Piezoelectric polarization vector in the direction perpendicular to the gate $-P_z$ for an InP HEMT with 6-μm gate length. Inset shows the corresponding piezoelectric charge distribution.

smaller by an order of magnitude, but also almost constant throughout the structure except for the channel, where it is lower because of the different material constants. This causes

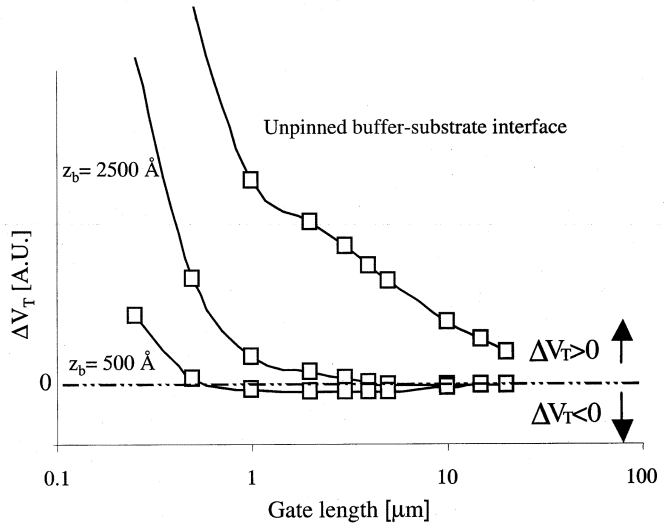

Fig. 10. Relative hydrogen-induced ΔV_T for InP HEMTs of different gate lengths. The different lines are calculations for two different buffer layer thicknesses (with a pinned Fermi-level at the buffer/substrate interface), as well as for an unpinned buffer/substrate interface.

the average of $-P_z$ to be lower above the bottom of the channel than below it and results in a *negative* threshold voltage shift.

Fig. 10 shows calculations of ΔV_T for InP HEMTs of different L_g and buffer thickness. The evolution of ΔV_T with L_g is similar to the experimental observations summarized in Fig. 1. For short devices, a positive ΔV_T occurs, that increases as the gate length decreases. For long devices, a negative ΔV_T is found with a magnitude that increases as the gate length is shortened.

Fig. 10 also shows that the buffer thickness plays an important role in ΔV_T if the Fermi-level is pinned at the buffer-substrate interface. For thinner buffer layers, the gate length at which ΔV_T changes sign becomes shorter. This is because as z_b decreases, $\langle -P_z \rangle$ in the buffer tends to increase causing a negative shift in ΔV_T.

The gate length at which ΔV_T changes sign depends on the details of the layer structure. If the insulator thickness decreases, the sign-change occurs for shorter devices (see Fig. 11). This is because a thinner insulator layer causes the average of $-P_z$ above the channel to decrease relative to the average below the channel and hence ΔV_T becomes more negative.

The design of the gate stack affects ΔV_T greatly. If the gate material above the expanding Ti layer is more rigid, such as if the thickness of these layers increases or when a higher Young's modulus is set for these layers, it absorbs more of the stress caused by the expanding gate. This decreases the stress in the heterostructure underneath, which results in a lower ΔV_T and a change in sign at a shorter gate length. On the other hand, lowering the rigidity of the gate increases ΔV_T and sets the sign-change at higher gate length. This can be done by thinning the Au layer in the gate from 3000 Å to 1000 Å (see Fig. 12). We also found that thinning the Ti layer will decrease ΔV_T and make the gate length at which ΔV_T changes sign shorter. Similarly, if we remove the nitride layer in our simulations, we find that the stress in the heterostructure increases and lowers ΔV_T significantly at shorter gate lengths (see Fig. 13). This makes sense since the nitride adds rigidity to the device structure.

The only difference between InP HEMTs and GaAs PHEMTs is the magnitude of the material constants. As a consequence, similar conclusions can be made for GaAs PHEMTs. This is seen in Fig. 14, which shows the H-induced threshold voltage shift for GaAs PHEMTs and InP HEMTs

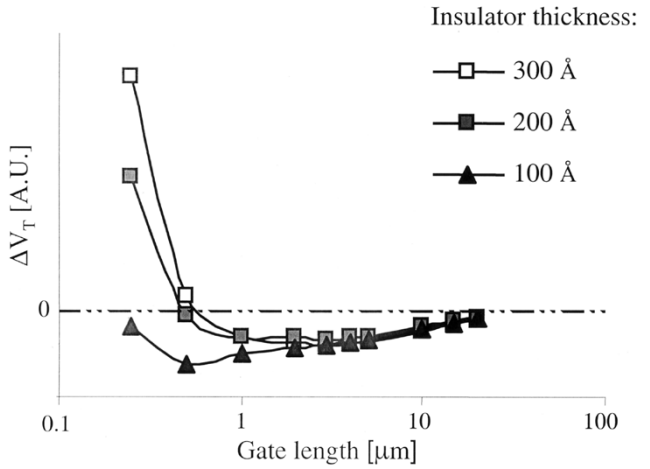

Fig. 11. Relative hydrogen-induced ΔV_T for InP HEMTs with insulator thicknesses of 100, 200, and 300 Å. The Fermi-level is pinned 500 Å below the channel.

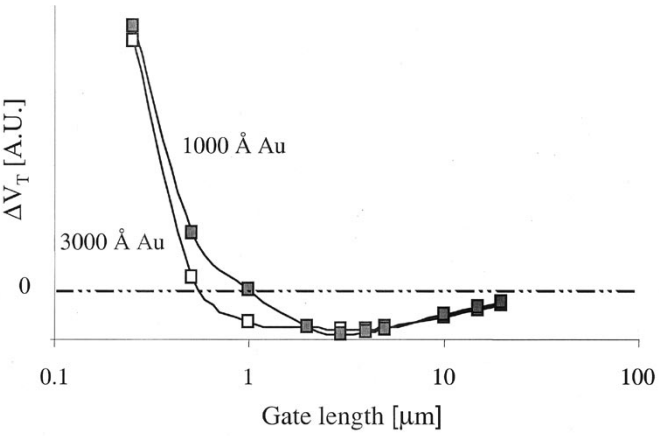

Fig. 12. Relative hydrogen-induced ΔV_T for InP HEMTs of different gate lengths with a Au thickness of 1000 Å and 3000 Å. The Fermi-level is pinned 500 Å below the channel.

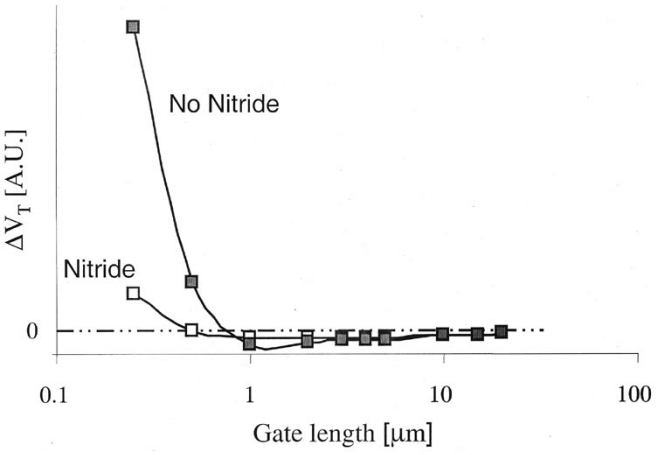

Fig. 13. Relative hydrogen-induced ΔV_T for InP HEMTs of different gate lengths, with and without silicon nitride covering the gate. The Fermi-level is pinned 500 Å below the channel.

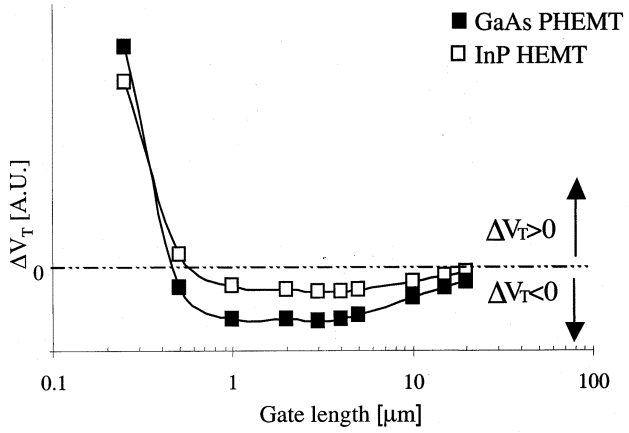

Fig. 14. Relative hydrogen-induced ΔV_T for InP HEMTs and GaAs PHEMTs of different gate lengths. The different lines are calculations for the Fermi-level pinned at 500 Å below the channel.

of different gate lengths. For identical conditions, it is found that GaAs PHEMTs show a larger ΔV_T than InP HEMTs, but otherwise a similar behavior.

IV. Discussion

Our study suggests that the H-induced piezoelectric effect can be mitigated through design of the gate and heterostructure of a device. One can change the gate orientation to [010], which according to this model would eliminate any H-induced piezoelectric ΔV_T, but for technological reasons, this solution is not always viable.

This research suggests that the gate-stack can be redesigned to minimize the stress in the device hetero-structure. This can be accomplished by thinning the Ti-layer, as this will reduce the magnitude of the stress, or by adding layers on top of the Ti layer, that absorb stress. Any measure that increases the rigidity of the gate structure will decrease ΔV_T. Separating the Ti-layer from the semiconductor structure should also diminish ΔV_T significantly, as the stress is most important immediately underneath the Ti-layer.

The H-induced piezoelectric effect can also be mitigated by engineering the heterostructure. By increasing the thickness of the channel compared to the thickness of the insulator, ΔV_T will decrease, because of the lower polarization vector in the channel. Thinning the buffer layer and setting the point where Fermi-level pinning takes place closer to the bottom of the channel should also minimize ΔV_T.

The results of our model hinge on the material constants that are used. Some of these are not well known. Nevertheless, the general behavior of ΔV_T on device design is not expected to be very different from what is computed here. This study is useful in that it reveals the key variables that impact hydrogen-induced ΔV_T in HEMTs.

V. Conclusions

We have modeled the hydrogen-induced ΔV_T in InP HEMTs and GaAs PHEMTs due to the piezoelectric effect. The modeling results are broadly consistent with experimental observations. The modeling study reveals that it is possible to mitigate this problem through careful design of the semiconductor heterostructure and the gate stack. Our work also suggests that it is possible to select a device design that is insensitive to hydrogen at a certain gate length.

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