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An Insulator-Lined Silicon Substrate-Via Technology With High Aspect Ratio

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***Abstract*—We have developed a novel high-aspect ratio substrate- via technology in silicon that features a SiN insulator liner. In this technology, the via is completely filled with electroplated Cu. We have demonstrated vias with an aspect ratio of 30 and we have verified the integrity of the liner in vias with an aspect ratio of 8. The impedance of individual vias was measured in the microwave regime using a high-frequency test structure. The measured inductance of vias with aspect ratios between 3 and 30 approach the theoretically expected values.**

***Index Terms*—Ground inductance, interconnections, Si RF technology, substrate-via, through-wafer via.**

I. INTRODUCTION

Substrate-vias are widely used in GaAs microwave and millimeter-wave ICs to provide low-impedance ground connections [1]–[5]. In many RF applications, silicon is starting to replace GaAs due to its lower costs and its logic integration capabilities [6]. As silicon RFICs strive for high-performance high-frequency operation, it becomes increasingly important to reduce all extrinsic parasitics. Of particular concern are the source impedance of MOSFETs and the emitter impedance of BJTs, which greatly affect the gain and efficiency of RF amplifiers [3]–[5], [7]. Toward these goals, substrate-vias in Si have been demonstrated using KOH etching [8]. This approach, however, demands substantial backside processing and results in poor aspect ratio vias with a large footprint at the wafer surface [8]. We have developed a through-wafer via technology for silicon, which allows the implementation of high-aspect ratio, low-impedance ground connections. Because this via technology incorporates an insulator liner, it could also be used to distribute power and ground in logic circuits and MEMS. Furthermore, this technology has enabled a novel isolation scheme to reduce crosstalk in mixed-signal circuits for system-on-a-chip (SOC) applications [9]. Our technology uses the same anisotropic plasma etch used in previous Si-via technologies, which have reached aspect ratios of 2.5 [6] and 17 [10]. The novelty of our via technology is that it features an insulator liner and that the vias are completely filled with Cu. As a consequence, they exhibit very low impedance over a broad frequency range. Additionally, we have fabricated a test structure that has allowed us to measure the impedance of a single via in the microwave regime.

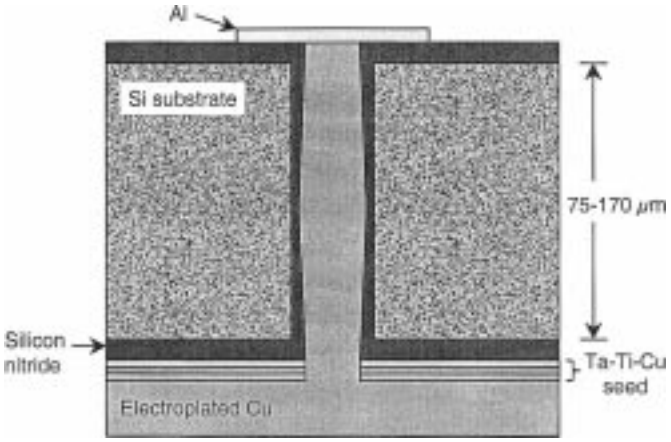

Fig. 1. Conceptual cross-sectional drawing of a substrate-via conformally lined with silicon nitride and filled with Cu. An Al pad is used to connect to the top of the via. In this work, the substrate thickness varied between 75 and 170 μm.

II. FABRICATION TECHNOLOGY

The substrate-via fabrication process was developed at the Microsystems Technology Laboratories at Massachusetts Institute of Technology (MIT). An illustration of the via concept is depicted in Fig. 1. In our work, substrate thicknesses ranged from 75 to 170 μm. The technology that we have developed can also be utilized in substrates of regular thickness. For characterization purposes, trenches as well as vias were fabricated.

Via etching was performed from the front of the wafer using a surface technology systems time-mutiplexed, inductively-coupled plasma DRIE, which uses a Bosch etch to produce nearly vertical sidewalls [11]. The etch rate was about 2 μm/min. Trench aspect ratios as high as 49 were achieved.

The insulator liner was made of silicon nitride, which in addition to electrically insulating the via from the substrate, it prevents Cu diffusion into silicon [12]–[14]. SiN was deposited by PECVD at 400 °C using a Novellus Concept-1. Depositions were carried out on the front and back of the substrate to improve the liner conformality. Hence, the liner was thinnest at the middle of the via sidewall. Measurements have shown that while the nitride thickness at the sidewall near the opening remains relatively constant with aspect ratio, the mid-sidewall

Manuscript received April 4, 2001; revised May 8, 2001. This work was supported by the SRC. The review of this brief was arranged by Editor J. M. Vasi.

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Publisher Item Identifier S 0018-9383(01)07325-7.

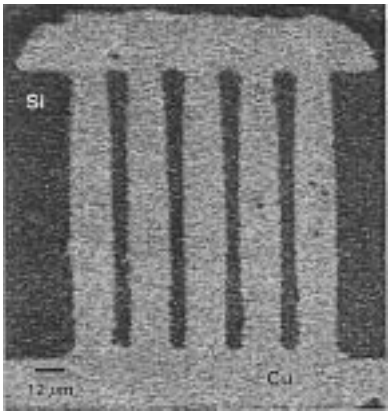

Fig. 2. SEM cross section of substrate-vias with an aspect ratio of 8. The substrate is 100-μm thick, and each via is 12-μm wide. These vias are conformally lined with silicon nitride and overfilled with Cu (prior to the CMP step).

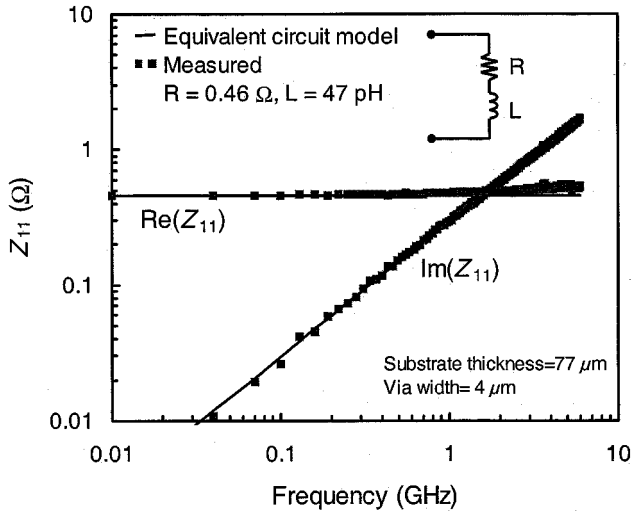

Fig. 3. Z_{11} versus frequency of a one-port test structure with a 4-μm wide and 77-μm deep via. The real part of Z_{11} is independent of frequency, while the imaginary part exhibits a linear dependence. This represents the ideal behavior of a simple resistor and inductor in series. The solid line plots simulation results of this equivalent circuit model from which the indicated values of resistance and inductance are extracted. The slight rise in resistance with frequency is due to the skin effect.

thickness decreases drastically. Using our current technology, conformality of the nitride is limited to an aspect ratio of approximately 15 in trenches.

Copper was electroplated in a Cu sulfate solution using a pulse-reverse current source [15], [16]. Before electroplating, a Ta–Ti–Cu seed layer was e-beam deposited on the backside of the substrate. Due to the directionality of the e-beam deposition and the high-aspect ratio of the via, the seed does not significantly coat the sidewalls. Hence during electroplating, the via fills with Cu from the bottom to the top. This method produced no seams or voids in the via. In this approach, the rate of filling of the via had a slight inverse dependence on the opening width. Additionally, the Cu deposition rate varied across the wafer. By overfilling the vias and using CMP to remove excess Cu, we were able to obtain a Cu filling that was flush with the surface for all via dimensions across the entire wafer. Contact to the via at the top was made through a patterned Al layer. We have succeeded in filling trenches with Cu with an aspect ratio of 49, and vias with an aspect ratio of 30. We have verified conformality of the liner in fully filled vias with an aspect ratio of 8, as shown in Fig. 2.

III. Results and Discussion

A test structure for measuring the impedance of a single via was designed and fabricated. This is a one-port 50-Ω ground-signal-ground coplanar transmission line with the via under test at the end of the signal line (Fig. 4 inset). The ground pads are shorted to the Cu ground plane through a large number of vias. Characterized vias ranged from 2.6 μm to 25 μm in nominal opening width on a 77-μm substrate. S_{11} was measured from 10 MHz to 6 GHz and converted to Z_{11}. The series resistance and inductance of the test structure pads were not de-embedded, so the actual impedance of a via is lower than the measured value.

For all vias, the real part of Z_{11} was found to be largely independent of frequency, while the imaginary part was positive and increased linearly with frequency (Fig. 3). These results suggest a simple via equivalent circuit model that consists of a resistor and an inductor in series. For vias with low-resistance the skin effect caused a noticeable increase in via resistance (seen in the increase in the real part of Z_{11} in Fig. 3) and a small decrease in inductance with frequency. This effect is more pronounced in vias with larger opening widths. Due to the limited range of frequencies in which we have characterized our vias, we have not been able to discern their parasitic capacitance to the substrate. At higher frequencies, this parasitic capacitance is likely to result in a self resonance.

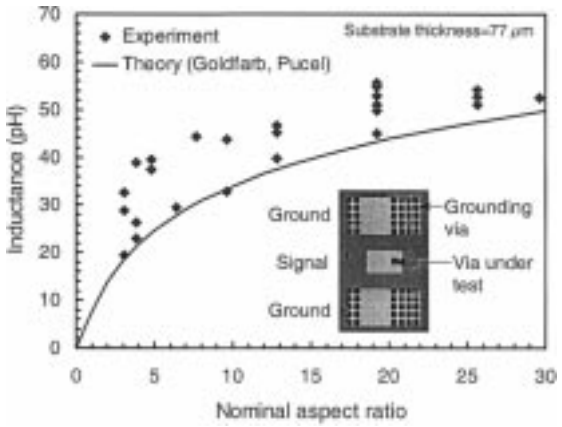

Fig. 4. Extracted inductance versus nominal aspect ratio of vias on a substrate thickness of 77 μm. Each data point represents a different via. Plotted in a solid line is the theoretical inductance [17]. The inset is a picture of an actual test structure with a 12-μm wide via under test. This one-port test structure was designed to measure the impedance of a single via. The multiple grounding vias are introduced to reduce the impedance of the ground pads.

Fig. 4 shows the extracted inductance of several vias at 6 GHz as a function of the nominal via aspect ratio. The actual aspect ratio is slightly smaller due to widening of the via opening during the DRIE etch but a detailed characterization of this effect is difficult and has not yet been performed. Also, vias with aspect ratio greater than 15 may have nonconformal liners. The inductance data in Fig. 4 is tightly clustered indicating the reproducibility of the process. As the via aspect ratio increases, so does the inductance. Fig. 4 also includes a theoretical calculation using the model of Golfarb and Pucel [17]. The lower lying experimental data points agree well with this theoretical model. This gives us confidence that the proposed technology can produce vias with theoretically minimum inductance.

IV. Conclusions

We have successfully developed a high-aspect ratio, insulated substrate-via technology for low-inductance power and ground distribution

in Si ICs. We have demonstrated fully-lined and completely filled substrate-vias with aspect ratios of 8. We have measured the inductance of individual vias and found that it approaches theoretically expected values. This technology is promising for low-loss power and ground distribution in Si RF ICs and MEMS, as well as for substrate crosstalk isolation in SOC applications.

ACKNOWLEDGMENT

The authors would like to thank J. G. Fiorenza, A. A. Ayón, J. Voldman, A. Fan, and the staff at the Microsystems Technology Laboratories at MIT for fabrication advice, D. A. Hitko for assistance with the measurements, and K. A. Jenkins for help with the test structures.

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