RF Power LDMOSFET on SOI

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***Abstract*—We have fabricated a SOI laterally diffused MOSFET that is designed for use in radio frequency power amplifiers for wireless system-on-a-chip applications. The device is fabricated on a thin-film SOI wafer using a process that is suitable for integration with SOI CMOS. An under-source body contact is implemented and both a high breakdown voltage and a high f_t are attained. The device performance compares favorably with bulk silicon rf power MOSFETs. For a gate length of 0.7 μm the device f_t is 14 GHz, $f_{\max}$ is 18 GHz, and the breakdown voltage approaches 25 V.**

***Index Terms*—LDMOSFET, RF CMOS, RF SOI.**

I. Introduction

THIS work describes a laterally diffused MOSFET (LDMOSFET) on thin-film silicon on insulator (SOI) that is designed for use in the transmitter rf power amplifier in portable wireless applications. Bulk silicon LDMOSFETs have been very successful in these applications [1], and implementation of a LDMOSFET in thin-film SOI may enable power amplifiers with improved gain, efficiency and bandwidth. Moreover, implementation of a LDMOSFET in thin-film SOI may allow the integration of the rf power amplifier (PA) into a wireless system-on-a-chip, in which all of the digital, analog, and rf circuits of a wireless system are integrated on to a single die. While thin-film SOI is a promising technology platform for a single chip system, the realization of a high performance rf power device in thin-film SOI is recognized as particularly challenging [2]. This paper demonstrates a LDMOSFET on SOI that compares well with bulk silicon LDMOSFETs. In this device, the body contact, which is critical to attaining a high breakdown voltage, is fabricated beneath the source. The intrinsic performance of this SOI LDMOSFET is as good or better than any know rf power MOSFET on SOI.

There is limited previous work on the development of MOSFET's on thin-film SOI for RF PA applications. Matsumoto *et al.* demonstrated a "Quasi-SOI" device with a high breakdown voltage and good rf performance, but its exotic fabrication process makes it incompatible with CMOS [3]. In [4], a rf PA is demonstrated on SOI that utilizes a technology that is adapted from standard SOI CMOS. The breakdown voltage of the technology is low, and the PA that is demonstrated operates from a power supply of only 1.8 V, too low to be useful in most modern wireless communication systems. In recent work, [5], a SOI LDMOSFET was fabricated, but it uses an inferior "stripped" body contact. This body contact increases the gate and drain capacitance for a given effective gate width, resulting in a reduced transconductance and frequency response. In [6], the intrinsic performance of the SOI MOSFET that was fabricated was poor because of the lack of a body contact and high overlap capacitance. The approach demonstrated in this letter addresses these weaknesses and yields unprecedented performance.

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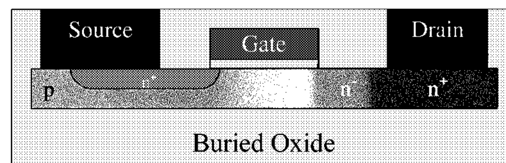

Fig. 1. Cross section of the rf power SOI LDMOSFET that was fabricated.

II. Device Fabrication

A cross section of the LDMOSFET that is demonstrated is shown in Fig. 1. The partially depleted SOI LDMOSFETs were fabricated on p-type ⟨100⟩ full-dose SIMOX wafers with an active silicon thickness of 200 nm, a buried oxide of 400 nm, and a resistivity of 10–20 Ω-cm. The process was designed so that the SOI LDMOSFET can be integrated into an SOI CMOS process. The silicon thickness is the same as the film thickness in mainstream SOI CMOS [7]. LOCOS isolation was used. The shortest n^+ polysilicon gate is 0.7 μm, the n^- lightly doped drain (LDD) region is 0.5 μm, and the gate oxide thickness is 30 nm. The lateral body doping profile was formed by masking the drain of the device, implanting the source with boron of dose 1.3×10^{13} cm^{-2} and energy 25 KeV, and annealing the wafers for 300 min at 1000 °C. The n^- LDD region was created by a phosphorous implant of dose 3×10^{12} cm^{-2} and energy 55 KeV. The n^+ source and drain regions were formed by a masked implant of dose 5×10^{15} cm^{-2} and energy 25 KeV. The n^+ implant mask defines the length of the n^- region. The dopants were activated by a 20 s, 1000 °C RTA process. After processing, the silicon thickness beneath the gate is 180 nm, and the n^+ junction depth beneath the source is 100 nm.

III. Results and Discussion

The output characteristics of a typical device are shown in Fig. 2. There is no sign of a "kink" or indication of impact ionization up to a drain voltage of 7 V. The transfer characteristics are shown in Fig. 3. The device transconductance rises quickly beyond threshold and settles to a flat plateau, which is typical of an LDMOSFET.

The S-parameters of the devices were measured to 6 GHz, and f_t and $f_{\max}$ were calculated by extrapolating at a slope of

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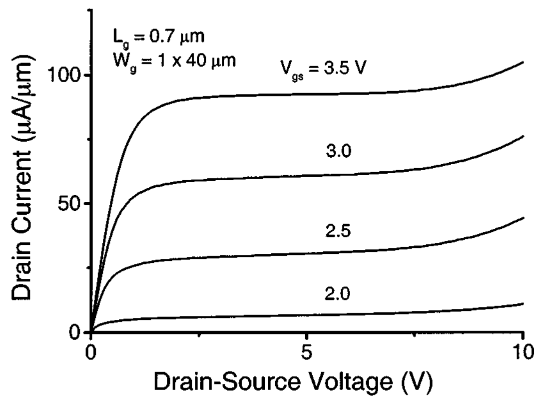

Fig. 2. Output characteristics of a fabricated SOI LDMOSFET. No trace of the "kink" effect is seen.

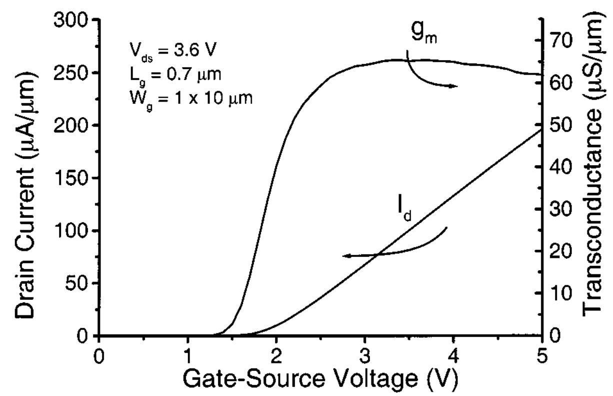

Fig. 3. Transfer characteristics of SOI LDMOSFET with a drain-source voltage of 3.6 V.

20 dB/decade from h_{21} and G_{ma}, respectively. The f_t of a device with two 20 μm wide fingers was 14 GHz. Power amplifier applications demand that a technology is able to yield devices with many gate fingers and a large total gate width. A ten-fingered device with 100 μm fingers was fabricated, and its f_t was 12.5 GHz. The $f_{\max}$ of the device with 20 μm fingers was 18 GHz, and rolled off with the inverse of the gate finger width due to the resistance of the polysilicon gate.

The SOI LDMOSFET utilizes an under-source body contact [8] to attain the high breakdown voltage required by rf PA applications. In the source, the n^+ doping is compensated by the body doping implant near the buried oxide. This creates a low-resistance p-type link beneath the source, and the body is shorted to the n^+ source by the source metal. The contact between the p-type source region and the metal is ohmic, but the specific contact resistance is high (1×10^{-4} Ω-cm) because the body doping implant dose is not high. This body contact design is a natural choice for an SOI LDMOSFET because it can be created using a standard rf LDMOSFET process and it requires no additional masking steps or unorthodox processing. Unlike the body contact schemes used in SOI CMOS [9] and the work in [5], this body contact prevents floating body effects without reducing the effective gate width or limiting the unit gate finger width.

The efficacy of the body contact is demonstrated in Fig. 4, which compares a device fabricated with the standard process to an identical device that was fabricated without a body contact. The body contact suppresses the "kink" effect, and substantially improves the on-state breakdown voltage ($BV_{\rm on}$) and off-state breakdown voltage ($BV_{\rm off}$). $BV_{\rm on}$ of the body-contacted device is greater than 10 V and $BV_{\rm off}$ is nearly 25 V. In contrast, the floating body device exhibits a pronounced kink and degraded on-state and off-state breakdown. $BV_{\rm off}$ of a larger, ten-fingered device is reduced to 20 V.

The suitability of our SOI LDMOSFETs for rf power applications is illustrated in Fig. 5, which plots f_t vs. $BV_{\rm off}$, the two most important figures of merit for a rf power device. Bulk silicon and SOI MOSFETs from the literature are included in the figure. Fig. 5 shows that the performance of our SOI LDMOSFETs is excellent in comparison to bulk silicon rf power MOSFETs from the literature. Our device also compares favorably to all other SOI rf power MOSFETs.

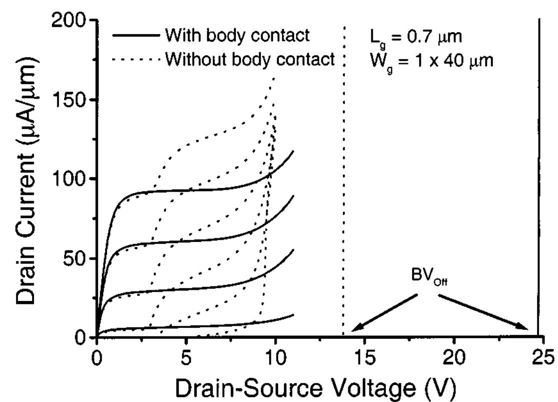

Fig. 4. Comparison of the output characteristics of a SOI LDMOSFET with a floating body and with a grounded body. $V_{gs} = 3.5$, 3.0, 2.5, 2.0, 1.5, 1, and 0 V.

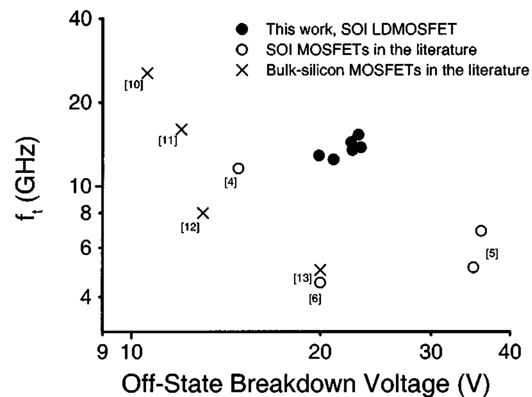

Fig. 5. $f_t - BV_{\rm off}$ tradeoff for the rf SOI LDMOSFET and bulk and SOI RF power MOSFETs from the literature.

IV. Conclusion

An rf SOI LDMOSFET with a high breakdown voltage and a high cutoff frequency has been demonstrated. The high breakdown voltage was achieved through the use of a simple, but effective, under-source body contact. This is a promising technology for rf PAs in future generations of highly integrated wireless systems.

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