Physical Mechanisms Limiting the Manufacturing Uniformity of Millimeter-Wave Power InP HEMT's

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***Abstract*—We have developed a methodology to diagnose the physical mechanisms limiting the manufacturing uniformity of millimeter-wave power InAlAs/InGaAs HEMT's on InP. A statistical analysis was carried out on dc figures of merit obtained from a large number of actual devices on an experimental wafer. correlation studies and principal component analysis of the results indicated that variations in Si delta-doping concentration introduced during molecular-beam epitaxy accounted for more than half of the manufacturing variance. Variations in the gate-source distance that is determined by the electron-beam alignment in the gate formation process were found to be the second leading source of manufacturing variance. The statistical methodology used in this work is suitable for continuous process yield diagnostics and improvement in a manufacturing environment.**

I. Introduction

The InP high electron mobility transistor (HEMT) is the leading contender for high-power high-efficiency millimeter-wave power amplifiers [1], [2]. As the InP HEMT technology matures, manufacturing issues come to the foreground. To date there has been little work on understanding the key factors affecting the manufacturing uniformity of these devices. Such a study has been hampered by the considerable amount of work that it takes to measure millimeter-wave power figures of merit. Manufacturing uniformity control and improvement is critical because high cost represents a significant road block in the development of millimeter-wave systems.

In this work we have carried out a statistical study of dc figures of merit of InP power HEMT's that strongly impact the millimeter-wave performance of these devices. All of the selected figures of merit were measured in actual devices. A statistical analysis of the results using a principal components analysis (PCA) was carried out. This analysis was instrumental in revealing the two dominant physical sources of variability in these figures of merit. The methodology used in this work can be easily implemented in a manufacturing environment for continuous process diagnostics and improvement.

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II. Experimental

The devices studied in this work are 0.1 μm gate length and 25 μm gate width double-heterostructure InP power HEMT's on one experimental 3-in wafer from Lockheed Martin Sanders [3], [4]. The heterostructure was grown by molecular-beam epitaxy (MBE) and includes two Si delta-doped layers above and below the channel. The devices feature an electron-beam written T-gate and a selectively recessed depleted cap. A total of 50 devices located on every other die of the wafer were studied. All figures of merit were measured with an identical probe configuration, allowing fast and completely automated measurements.

We selected ten dc figures of merit that map to key millimeter-wave power figures of merit. They are listed in Table I. They include the threshold voltage, V_T, the maximum transconductance, $g_{m\max}$, the gate-source voltage at which $g_{m\max}$ occurs, $V_{\rm GS}(g_{m\max})$, the maximum drain current, $I_{D\max}$, the output conductance, g_d, the off- and on-state breakdown voltages, $BV_{\rm dg_off}$, $BV_{\rm ds_off}$ and $BV_{\rm ds_on}$, and the source and drain resistances, R_s and R_d. The measurement conditions for these figures of merit are also summarized in Table I. Basically, V_T, $g_{m\max}$, $V_{\rm GS}(g_{m\max})$ and $I_{D\max}$ were obtained from the transfer characteristics. g_d was obtained from two transfer characteristics at two close values of $V_{\rm ds}$. $BV_{\rm dg_off}$ and $BV_{\rm ds_off}$ were extracted using the drain-current injection technique [5]. $BV_{\rm ds_on}$ was measured using the gate-current extraction technique [6]. R_s and R_d were obtained using the end-resistance technique [7]. Of the 50 devices that were measured two were found to be anomalous and their corresponding data were discarded. Table I lists the mean and standard deviation of each figure of merit. The standard deviation as percentage of the mean is additionally given. Variations of the figures of merit never exceed 16% across the entire wafer.

The correlation matrix of the measurements of the figures of merit is shown on Fig. 1. Each vignette lists the correlation coefficient between two figures of merit. A correlation coefficient close to one indicates a strong positive correlation between the two selected figures of merit; if close to -1, the correlation is strong but negative; if close to zero, the correlation is weak. Some of the correlation coefficients on Fig. 1 can be interpreted directly. For example, R_s and R_d exhibit a strong positive correlation coefficient of 0.68. This suggests a contact resistance or doping level control problem and excludes misalignment of the gate process from being a dominant source of variation in these figures of merit (it would result in a negative correlation coefficient).

Spatial information is often useful in identifying sources of variability. Fig. 2 shows the spatial distribution across the wafer

TABLE I
DEFINITIONS AND THE MEASURED VALUES OF THE DC FIGURES OF MERIT USED IN THIS WORK ($L_g = 0.1\ \mu$m, $W_g = 25\ \mu$m). "STDV" REFERS TO THE STANDARD DEVIATION OF THE FIGURES OF MERIT

Symbol	Figure of Merit	Measurement Conditions	Mean	Stdv	Units	Stdv/|Mean| (%)
V_T	Threshold voltage	V_{ds}=1.2 V, I_D=1 mA/mm	-1.442	0.072	V	5.0
g_{mmax}	Maximum transconductance	V_{ds}=1.2 V	718	49	mS/mm	6.8
$V_{GS}(g_{mmax})$	Gate-source bias for GM_{max}	V_{ds}=1.2 V	-0.656	0.078	V	12
I_{Dmax}	Maximum drain current	V_{ds}=1.2 V, V_{gs}=0.4 V	846	68	mA/mm	8.0
g_d	Output conductance	V_{ds}=1.2 V, V_{gs}=0 V	91	11	mS/mm	12
BV_{dg_off}	Drain-gate off-state breakdown voltage	I_D = 1 mA/mm, I_G =-1 mA/mm	3.85	0.21	V	5.5
BV_{ds_off}	Drain-source off-state breakdown voltage	I_D = 1 mA/mm, I_G =-1 mA/mm	2.09	0.26	V	12
BV_{ds_on}	Drain-source on-state breakdown voltage	I_D = 200 mA/mm, I_G =-1 mA/mm	1.63	0.14	V	8.6
R_s	Source resistance	I_S=I_G=100 mA/mm, I_D=0	0.24	0.04	Ohm*mm	16
R_d	Drain resistance	I_D=I_G=100 mA/mm, I_S=0	0.31	0.05	Ohm*mm	16

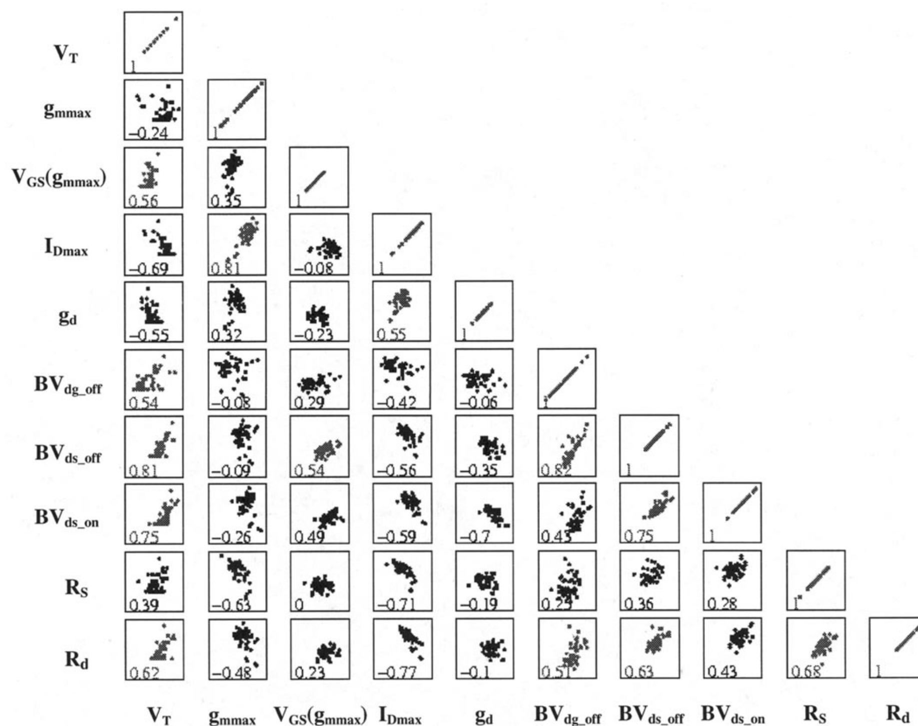

Fig. 1. Correlations among dc figures of merit. The number in each vignette indicates the correlation coefficient.

of two figures of merit: $BV_{\text{dg_off}}$ and $g_{m\,\max}$. While $BV_{\text{dg_off}}$ exhibits a circular symmetry, $g_{m\,\max}$ appears to show a linear gradient from left to right in the figure. This suggests that there are at least two different and independent mechanisms at play that result in variations in the figures of merit.

From examination of the data in Figs. 1 and 2 alone, it is not possible to uncover the physical sources of variability. In order to further our insight into the physics underlying variations in the figures of merit we have performed PCA of the data.

III. PRINCIPAL COMPONENT ANALYSIS

PCA is a statistical technique that performs a coordinate transformation from the original space of electrical measure-

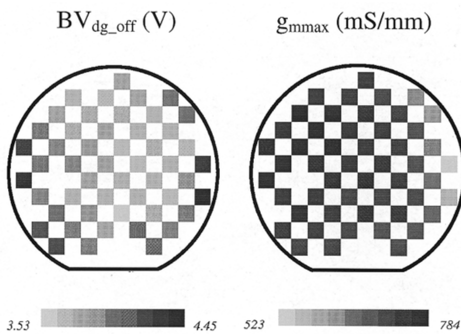

Fig. 2. Spatial distribution on the wafer of $BV_{\rm dg_off}$ and $g_{m\,\max}$. The fact that these two distributions are very different suggests that there are at least two major mechanisms that result in manufacturing variations.

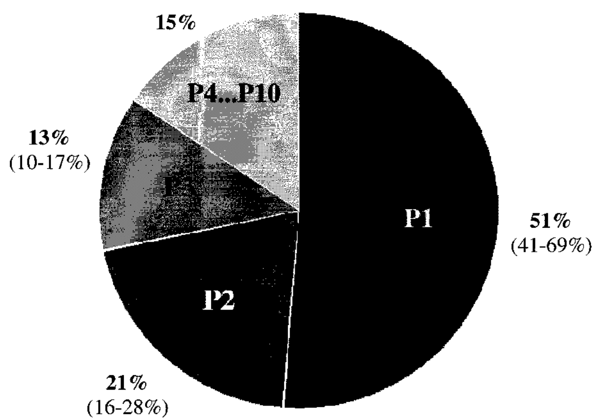

Fig. 3. Relative importance of the principal components in the manufacturing variance. P1 explains 51% of the variance of the manufacturing process.

ments to a new space of uncorrelated "principal components." These principal components are ordered according to the total variance that they account for in the original data: first P1 is selected to account for the maximum possible variance in the data set, then the second component, P2, is selected to maximize the variance of the residual after P1 is removed, and so on. A comprehensive treatment of PCA can be found in [8]. More details about the use of PCA in our work can be found in [9]. In the first pass, all figures of merit were weighted equally. Emphasis on selected figures of merit can be made by introducing appropriate weights.

The relative contribution of each principal component to the total variance of the data set is shown in Fig. 3. This figure shows that the most significant component, P1, accounts for 51% of the total variance of the process. Correct identification of this component followed by appropriate corrective action can significantly improve the manufacturing uniformity of this process. The second and the third components account for 21% and 13% of the total variance respectively. The rest of the components add up to a total of 15%. 80% confidence intervals for the contributions of each principal component can be found as in [8]. They are listed in brackets in Fig. 3. P1, for example, accounts with 80% confidence for 41% to 69% of the variance of the entire data set. The confidence intervals of components P5 through P10 overlap badly. This indicates that the experimental data is

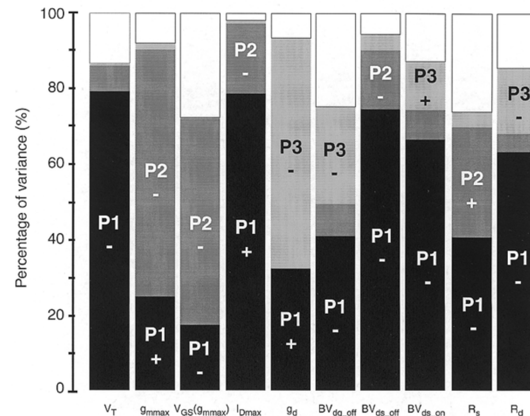

Fig. 4. Contributions of each of the principal components to the variance of each dc figure of merit. The signs indicate whether a component has a positive or negative correlation with a given figure of merit (see text).

insufficient for computing their values and identifying them. Identification and correction of the first three components, however, is sufficient for dramatic uniformity improvement.

In order to carry out the identification of the leading principal components, their relative impact on each dc figure of merit should be examined. Fig. 4 shows a percentage of the variance of each figure of merit that is attributed to each principal component. For example, P1 accounts for nearly 80% of the variance of V_T. In contrast, P1 accounts for less than 25% of the variance of $g_{m\,\max}$, while P2 accounts for nearly 70% of it. P3 is seen to enter strongly in the variance of g_d. The percentages shown in Fig. 4 are statistically significant for each of the three most important components. The standard deviations of the contributions of the first three principal components toward any figure of merit did not exceed 9% under the assumption of a multivariate normal distribution [8]. Hence Fig. 4 is a reliable vehicle for physical identification of the three leading principal components.

Fig. 4 also indicates the sign of the correlation between the principal components and the figures of merit. PCA does not yield the absolute signs of the correlations, just the relative sign among all correlations of a given principal component. For example, the correlation between P1 and V_T has a contrary sign to the correlation of P1 and $I_{D\,\max}$. In Fig. 4, a choice of signs has been made that makes physical sense and that aids the identification of the physical origin of the principal components. This is discussed in detail below.

Spatial distributions of the principal components can also be constructed. They are exhibited on Fig. 5 for P1, P2 and P3. The circular symmetry of P1 and the linear gradient distributions of P2 and P3 offer further clues for their identification. This figure also shows how these three principal components are uncorrelated: their spatial distributions are very different.

We now proceed to give a physical interpretation to P1, P2 and P3. The previous section suggests that these principal components are closely related to various steps of the manufacturing process. The identification is facilitated by Fig. 4, which indicates the nature of relationships between the principal components and the figures of merit.

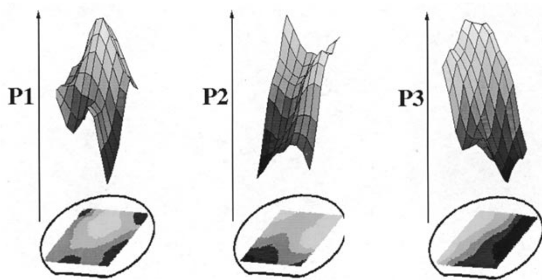

Fig. 5. Spatial distributions on the wafer of the first three principal components. Notice that the first component, P1, has a radial distribution, while P2 and P3 exhibit linear gradients along orthogonal directions.

A. Interpretation of P1

Fig. 4 shows that P1 has a strong positive correlation with $I_{D\,\max}$ and strong negative correlations with V_T, the breakdown voltages, and the parasitic resistances. This behavior can only be explained by associating P1 with the sheet carrier concentration in the channel of the device, n_s. Let us examine this hypothesis in detail.

- P1 accounts for 78% of the variance in V_T, and the correlation is negative. Higher n_s increases the inversion charge in the channel in equilibrium which makes V_T more negative.
- The impact of P1 on $I_{D\,\max}$ is large (77%) and positive. This is consistent with the fact that $I_{D\,\max}$ in InP power HEMT's is limited by n_s [11].
- P1 has a relatively large impact on the variances of all three breakdown voltages, and the correlation between P1 and these quantities is negative. It is well known that all these breakdown voltages decrease when n_s is increased [4], [10].

  P1 accounts for a substantial fraction of the variance of R_s and R_d and exhibits a negative correlation. This is also consistent with P1 being related to n_s in the channel since a portion of R_s and R_d is the access resistance from the edge of the ohmic contact to the edge of the gate. Additionally, this is a power device design with a surface depleted cap in which the access resistance is dominated by n_s.
- P1 has a small but positive correlation with the variance of $g_{m\,\max}$. This is also consistent with the identification of P1 as related to n_s. $g_{m\,\max}$ is the extrinsic transconductance and it should increase slightly when n_s increases through the negative impact of n_s on R_s.

  The negative correlation between P1 and $V_{\mathrm{GS}}(g_{m\,\max})$ can be explained through the impact of n_s on V_T. As n_s increases, V_T shifts down and with it the whole g_m vs. V_{gs} curve shifts to lower voltages, thus decreasing $V_{\mathrm{GS}}(g_{m\,\max})$.
- The positive correlation between g_d and P1 stems from the fact that g_d increases with the bias current at which it is measured which in turn increases with n_s as discussed above.

The preceeding discussion makes it quite convincing that P1 is directly associated with the sheet carrier concentration of electrons in the channel, n_s. But what makes n_s change? There are two possibilities for it, one is the InAlAs insulator thickness, the second one is the Si doping level in the delta-doped supply layers. The weak correlation between P1 and $g_{m\,\max}$ allows us to rule out the first option since a change in insulator thickness should strongly affect the transconductance of the device through the insulator capacitance. Hence, P1 represents the Si doping level in the supply layers. The Si dopants are introduced during the MBE growth of the structure in the form of two delta-doped layers above and below the channel. The sample is rotated during MBE growth in order to compensate for spatial nonuniformity of the Si flux emanating from the effusion cell. This compensation is not perfect and a variation of Si concentration with a circular symmetry results on the wafer. This is precisely what is observed for the spatial distribution of P1 over the wafer shown in Fig. 5.

B. Interpretation of P2

P2 has a positive correlation with R_s, but only a weak influence on R_d (Fig. 4). Its impact on $g_{m\,\max}$ is very large (63%), but there is none on g_d. There is also negligible influence of P2 on V_T. This strongly suggests that P2 is related to the gate-source extrinsic region of the device. A likely explanation for the correlation of P2 with the figures of merit is the identification of P2 with the variations in the gate-source distance L_{gs}. Let us examine this hypothesis in detail.

- P2 has a negligible impact on V_T, because V_T does not depend on the position of the source contact relative to the gate.
- The negative correlation of P2 and $g_{m\,\max}$ arises through R_s, which is directly affected by L_{gs}.
- The negative correlations between P2, $V_{\mathrm{GS}}(g_{m\,\max})$ and $I_{D\,\max}$ are related. The peak and subsequent drop in transconductance in the devices under test results from the blow up of source resistance at high current values due to velocity saturation [12]. A higher value of L_{gs} makes this condition occur at smaller values of current, thus leading to a smaller $V_{\mathrm{GS}}(g_{m\,\max})$ and $I_{D\,\max}$.
- As an extrinsic source related parameter, P2 should have no impact on g_d and the breakdown voltages.
- The positive correlation between P2 and R_s makes sense since R_s is linearly proportional to L_{gs}.
- In principle, since R_d is related to L_{dg} and that in turn is affected by L_{gs}, one would expect a negative correlation between R_d and P2: the higher L_{gs}, the smaller L_{gd} and R_d ought to be. This is not observed in our results. There is no statistically significant correlation between R_d and P2. A possible explanation for this is that these are asymmetric devices with the gate placed closer to the source. Thus, the relative impact of misplacing the gate is significantly higher on the source side than on the drain side. Additionally, asymmetric gate placement makes the impact of n_s variations higher in R_d than R_s, as observed in Fig. 4. This makes it harder to identify any other sources of variance in R_d.

Gate-source distance variations are determined by the reproducibility of the positioning of the electron beam process used to write the gate. P2 has a roughly linear distribution on the wafer

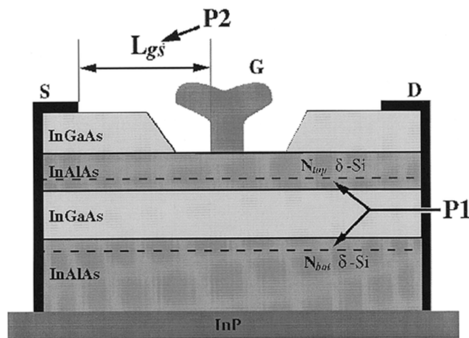

Fig. 6. Identity of the first two principal components in the structure of an InP power HEMT.

(Fig. 5). This is consistent with the identification of P2 as an electron-beam process related variable, since the electron beam draws the gate on the wafer scanning the die in a linear manner. Fig. 6 shows a schematic diagram of the device indicating the physical origin of P1 and P2.

C. Interpretation of P3

The results of Fig. 4 indicate that P3 affects only g_d, $BV_{\mathrm{dg_off}}$, and R_d. This suggests a strong association of P3 with the extrinsic drain portion of the device. Upon detailed examination of all correlations and their signs, no single structural parameter of the device could be found that is consistent with all results. The detailed origin of P3 remains unknown.

IV. Discussion

Measurements on transmission line model (TLM) test structures were carried out in an effort to confirm the identity of P1. The saturation current that is obtained in a TLM structure when a relatively high voltage is applied is directly proportional to n_s and the electron saturation velocity v_{sat}. Since v_{sat} is set by the nature of the material, it should not be affected by small manufacturing variations. Hence, the maximum current in a TLM constitutes a direct probe of the sheet carrier concentration in the channel of a HEMT with a depleted cap.

The TLM's used in this work were 100 μm wide and 50 μm long. The saturation current was measured at 10 V in every die in which transistor measurements had been performed. Fig. 7 shows the obtained maximum current in each TLM, $I_{\max}$, as a function of the value of P1 for every die. There is a very close correlation across the entire wafer in these two parameters: the correlation coefficient is 0.84. In consequence, this measurement constitutes an independent confirmation of the identification of P1 as the Si delta-doping concentration with a direct impact on the sheet carrier concentration n_s made earlier.

Our findings are in substantial agreement with those of Elliott *et al.* [13] on TRW's 3-in fabrication line for InP-based HEMT and HBT MMIC's. These authors single out MBE growth as the most critical node in InP HEMT MMIC production. This is in agreement with the MBE origin of P1 in our work. Additionally, they identified gate formation as the second most critical node for HEMT's. They found that gate length and gate-source spacing are critical parameters. While we have not been able to isolate the impact of the gate length variations, we relate P2 to the distance between the gate and the source, in agreement with the findings in [13].

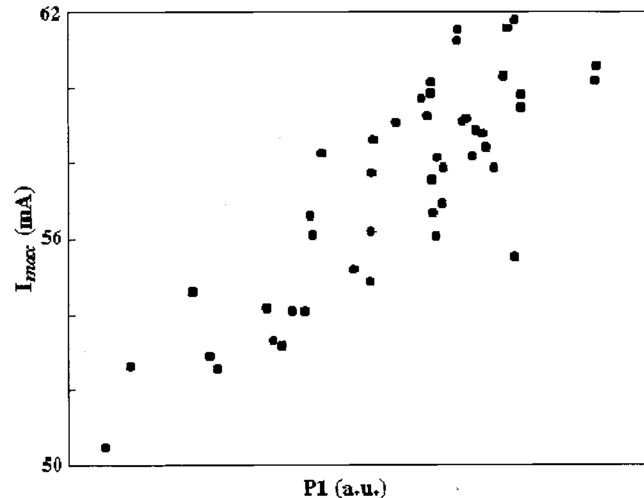

Fig. 7. Maximum current through a TLM test structure versus the P1 value for the HEMT device on the same die. The correlation coefficient is 0.84.

V. Conclusion

In summary, we used PCA to identify the two most important sources of manufacturing variability in InP power HEMT's: the concentration of Si dopants in the delta-doping layers of the device and the distance between the gate and the source. Jointly these two components account for 72% of manufacturing variations in this process. Our findings are in agreement with those reported by Elliott *et al.* [13] on TRW's InP based MMIC fabrication line. Necessary statistical data were obtained from simple dc measurements on actual transistors—no specialized test structures were required. Our methodology can be easily implemented in a manufacturing environment for continuous process uniformity diagnostics and improvement.

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