

A New Gate Current Extraction Technique for Measurement of On-State Breakdown Voltage in HEMT's

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Abstract—We present a new simple three-terminal technique for measuring the on-state breakdown voltage in HEMT's. The gate current extraction technique involves grounding the source, and extracting a constant current from the gate. The drain current is then ramped from the off-state to the on-state, and the locus of drain voltage is measured. This locus of drain current versus drain voltage provides a simple, unambiguous definition of the on-state breakdown voltage which is consistent with the accepted definition of off-state breakdown. The technique is relatively safe and repeatable so that temperature dependent measurements of on-state breakdown can be carried out. This helps illuminate the physics of both off-state and on-state breakdown.

Index Terms—Electric breakdown, impact ionization, measurement, MESFET's, MODFET's.

GREAT STRIDES have been made in understanding and improving off-state breakdown (BV_{off}) in HEMT's [1]–[5]. However, there has been little work on the on-state breakdown voltage (BV_{on}), even though BV_{on} is a parameter of primary importance for power devices [6]. This is largely due to difficulties in defining and measuring this figure of merit.

Typically on-state breakdown is thought of as a significant upturn in the drain current, or as a rise in the output conductance [7]. Thus, one approach for determining BV_{on} is to bias the device at a given gate voltage, and to increase V_{DS} gradually until a rise in I_D is observed. Unfortunately this measurement is frequently destructive, as observing the rise in I_D requires biasing the device in a region of significant carrier multiplication. Furthermore, this definition is rather ambiguous due to the significant output conductance typically present in short gate length HEMT's. An alternative approach is to use a burnout criterion [6]—the device is biased at a given gate voltage, and the drain voltage is increased until the device is destroyed. While such a definition is precise, it is undesirably destructive. A simple, reproducible definition and technique to measure BV_{on} is needed.

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The physics underlying on-state breakdown offer some insight into how one might define BV_{on} . It is widely thought that carrier multiplication started by channel electrons is responsible for BV_{on} . If this is the case, it should be possible to define on-state breakdown by means of I_G . This is because it is known that when carrier multiplication takes place in the channel, some fraction of the impact ionization generated holes escape through the gate. These holes create the classic “bell” shape in I_G [8]. Thus by measuring I_G we should obtain some picture of the impact ionization in the channel [9]. Meneghesso *et al.* have shown that in the on-state, I_G is a reasonable metric for impact ionization. They have also made an implicit connection between I_G and BV_{on} [9].

Since $|I_G|$ is much smaller than I_D , it is much more sensitive to impact ionization, and should be a better predictor for BV_{on} . Furthermore, Rohdin has recently suggested that burnout may be correlated to constant impact ionization in the channel [6]. Thus, to the extent that I_G measures impact ionization, an I_G -based definition of BV_{on} may be sensible from a reliability perspective as well. Finally, BV_{off} is typically defined at a given gate current (e.g., $I_G = -1$ mA/mm) [10]. Obviously it is desirable to define BV_{on} so it is consistent with the BV_{off} definition. In other words, BV_{on} should converge to BV_{off} as the device is turned off.

These considerations motivate us to propose a simple gate current extraction technique as a measurement of BV_{on} . The measurement is depicted in Fig. 1: I_G is held constant at a desired value (a typical condition is -1 mA/mm), and I_D is ramped from $|I_G|$ to some reasonable value (typically 20–40% of $I_{D\text{max}}$). In this way, a locus of V_{DS} versus I_D is traced for constant I_G (Fig. 1); we define this locus as BV_{on} . This definition is sensible in several respects. First, it is consistent with the standard definition of BV_{off} , i.e. $|I_G| = I_D = 1$ mA/mm. Second, since the rise in I_G reflects a rise in I_D , the measurement defines a locus of rising output conductance which is typically associated with BV_{on} . Third, as we discuss below, the technique allows investigation of the physics behind BV_{off} and BV_{on} . Finally, it does a reasonable job of predicting burnout.

The technique is illustrated on a state-of-the-art $0.1 \mu\text{m}$ InAlAs/In_{0.67}Ga_{0.33}As HEMT [1] in Fig. 2, where BV_{on} loci for several values of I_G are superimposed on the output characteristics. Note that as the device is turned on, BV_{on} first drops from 4.2 V (the value of BV_{off}) to less than 2.5

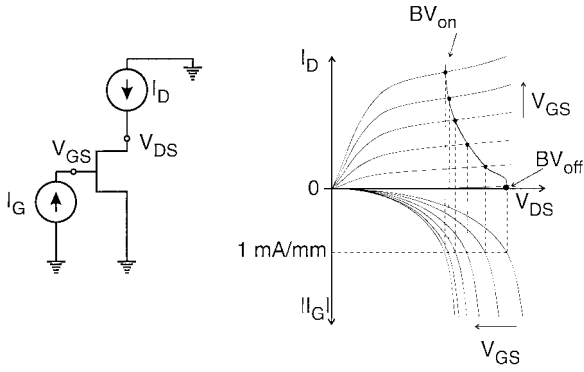


Fig. 1. Gate current extraction technique for measuring BV_{on} . A constant current (typically 1 mA/mm) is extracted from the gate while I_D is swept from the off-state (1 mA/mm) to the on state. The technique traces a breakdown locus of V_{DS} versus I_D .

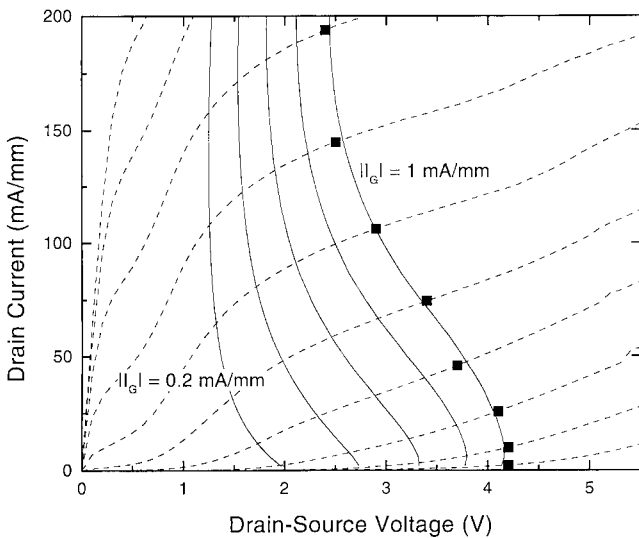


Fig. 2. BV_{on} versus I_D for a 0.1 μm InAlAs/In_{0.67}Ga_{0.33}As HEMT for different values of I_G . The data are superimposed on the output characteristics. As an independent verification of the technique, the points on the output characteristics at which $|I_G| = 1$ mA/mm are plotted as well. The constant I_G criteria additionally tracks the sudden rise of drain conductance often associated with BV_{on} .

V, and then saturates. Examining the output characteristics, we see that for $V_{DS} > BV_{on}$, the drain conductance begins to rise, indicating that the device is entering the region normally associated with BV_{on} . As a verification of the technique, we also plot the points on the output characteristics at which I_G reaches -1 mA/mm. The fact that these points fall on the BV_{on} locus demonstrates that the measurement is relatively safe and reproducible. Although one could obtain this information by measuring the output characteristics, such an approach typically results in device degradation, as it requires driving V_{DS} to BV_{off} while the device is on (as was done to obtain Fig. 2).

To confirm further the versatility of the technique, we compare in Fig. 3 the results of BV_{on} measurements for a 0.1 μm InAlAs/In_{0.67}Ga_{0.33}As HEMT, a low-noise 0.1 μm pHEMT (AlGaAs/In_{0.22}Ga_{0.78}As), and a high-breakdown 1 μm InAlAs/In_{0.53}Ga_{0.47}As HEMT. We have also tested

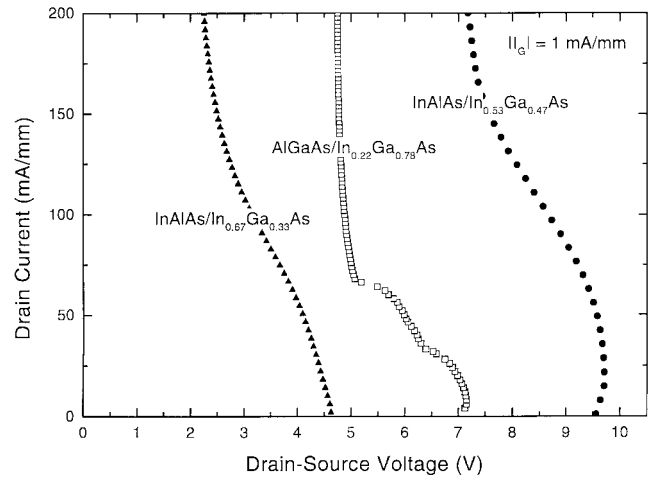


Fig. 3. BV_{on} versus I_D for a 0.1- μm InAlAs/In_{0.67}Ga_{0.33}As HEMT, a 0.1 μm AlGaAs/In_{0.22}Ga_{0.78}As pHEMT, and a 1 μm InAlAs/In_{0.53}Ga_{0.47}As HEMT. All three devices show similar BV_{on} behavior.

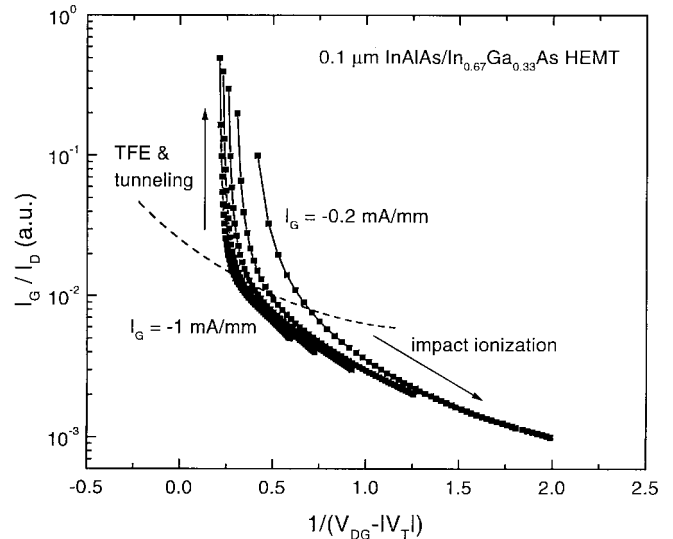


Fig. 4. I_G/I_D versus $1/(V_{DG} - |V_T|)$ along BV_{on} loci for different values of I_G for 0.1- μm InAlAs/In_{0.67}Ga_{0.33}As HEMT. The device shows a clear transition to impact ionization behavior.

the repeatability of the technique by performing extensive temperature-dependent measurements of BV_{on} in these devices. We find that in the GaAs-based device, BV_{off} drops with increasing temperature, while BV_{on} increases slightly. In InP-based devices, on the other hand, both BV_{off} and BV_{on} drop with increasing temperature. Given the positive temperature dependence of impact ionization in InGaAs on InP [9], these results indicate that while BV_{off} may be due to tunneling/thermionic field emission [[5], the BV_{on} locus is more dominated by impact ionization.

This picture is supported by Fig. 4, which plots I_G/I_D versus $1/(V_{DG} - |V_T|)$ along the BV_{on} contours for different values of extracted gate current in the InAlAs/In_{0.67}Ga_{0.33}As device. As can be seen, at lower values of I_G/I_D , which correspond to higher values of I_D (I_G is held constant while I_D is varied in this measurement), all the curves converge to classical impact ionization type behavior. This has been

independently confirmed by sidegate measurements. On the other hand, at higher values of I_G/I_D (closer to the off-state), the data become almost vertical, suggesting an I_D independent mechanism, such as tunneling/TFE, as the device is turned off. The pHEMT and the lattice-matched device behave similarly. This behavior of I_G/I_D makes the gate current extraction technique a powerful tool for understanding BV physics in HEMT's.

Statistical burnout measurements on several InAlAs/In_{0.67}Ga_{0.33}As HEMT's [1] suggest that BV_{on} is a reasonable predictor for burnout. In order to measure burnout, we inject a given current into the drain, and gradually increase I_G until the device blows. Such an approach allows us to avoid oscillation problems. Approximately 150 devices on three wafers with different sheet carrier concentrations were destroyed to obtain a reasonable statistical distribution. Our measurements showed that burnout occurs at an approximately constant value of I_G on all three wafers *regardless of I_D* so long as the device is fully on. This suggests that the burnout is associated with the total multiplication current (mapped by I_G), and not with the drain current, consistent with [6]. As burnout occurs at $|I_G| \approx 3$ mA/mm, a constant gate current criteria of around 1 mA/mm seems reasonable for predicting the burnout locus. Of course, the appropriate current criteria might be different for alternative designs—for example, a device with an insulator hole barrier might be expected to burn out at a lower value of I_G than the devices we consider here.

In summary, we have presented an unambiguous definition and a simple, nondestructive measurement technique for BV_{on} in HEMT's. The technique measures a locus of BV_{on} in a single scan, and is consistent with the standard BV_{off} definition. The technique also provides a diagnostic for the physics of BV_{on} , and is useful in projecting burnout.

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