Briefs

Nonlinear Source and Drain Resistance in Recessed-Gate Heterostructure Field-Effect Transistors

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Abstract—**We have profiled the parasitic source and drain resistances versus current in recessed-gate HFET's with heavily-doped caps, using an InAlAs/n$^+$-InP HFET as a vehicle. We observe a dramatic reduction in the parasitic resistances at moderate-to-high currents as significant current passes through the cap. Consequently, we note very little dependence in g_m on the length of the extrinsic gate-source region. This is an experimental verification of predictions of two-layer models in the literature.**

I. Introduction

An expanding market for millimeter-wave applications has fueled interest in developing high-frequency heterostructure field-effect transistor (HFET) technologies capable of handling large currents and voltages as well as achieving low noise. One key aspect of optimizing an HFET for such applications is reducing the parasitic source and drain resistances. The large-signal parasitic resistances (R_S and R_D) raise the on-resistance of a device at low V_{DS}, increasing the saturation voltage ($V_{DS}^{\rm sat}$) and adding thermal noise. The small-signal source resistance (r_s) is well known to degrade figures of merit such as g_m, $f_{\rm max}$, and, to a lesser extent, f_T. In addition, the small-signal drain resistance (r_d) can degrade f_T dramatically through its contribution to the Miller effect [1].

In order to reduce parasitic resistance, most high-frequency device designs take advantage of recessed-gate technology, in which a heavily-doped cap is removed over the intrinsic device area in a self-aligned manner but retained over the extrinsic region. The cap in such a scheme is widely known to screen the extrinsic channel from surface depletion effects [2]. Several studies, however, suggest that a doped cap layer may interact with the extrinsic channel in a more complex manner [3]–[6], with electrons moving between the cap and channel via tunneling or thermionic field emission. The low-resistance cap thus conducts in parallel with the channel, reducing parasitic resistance substantially.

Despite the performance implications tied to the physics of a capped extrinsic region, studies to date have concentrated primarily on developing two-layer models [3]–[6], with experimental work addressing only a few discrete low-current bias points or making only indirect device I-V curve comparisons [5], [6]. To the best of our knowledge, there have been no direct measurements of the nonlinear source and drain resistances versus current over the full current range of a typical HFET.

This work presents such an experimental study of the extrinsic source resistance in an InAlAs/n$^+$-InP HFET technology employing InP epitaxial layers as both the active channel and as an etch-stopper in a selectively-recessed n$^+$-InGaAs cap scheme [7], [8].

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II. Results

The heterostructure design and device fabrication used in this work has been previously summarized in [8]. In addition to standard recessed-gate devices and associated test structures, we also fabricate "uncapped" devices for comparison. These are processed identically except for having the cap layer selectively etched off completely at the start of the process.

A key step in investigating the physical operating mechanisms of the cap in our devices is to fully characterize the sheet resistances of and contact resistances to the cap and channel layers. To this end, we employ both the Transmission-Line Model (TLM) and the Floating-Gate TLM (FGTLM) techniques [9] on both capped and uncapped samples, using a small bias of $\sim$100 mV. The FGTLM method applied to devices with varying gate lengths (L_g) yields the channel sheet resistance ($R_{sh}^{\rm chan}$) beneath the gate. The same method applied to devices with varying source-to-gate gap lengths (L_{sg}) determines $R_{sh}^{\rm chan}$ and the channel contact resistances ($R_c^{\rm chan}$). Finally, TLM structures on capped samples yield the cap contact ($R_c^{\rm cap}$) and sheet ($R_{sh}^{\rm cap}$) resistances. In this manner, we find a value for ($R_{sh}^{\rm cap}$) of 50 $\Omega/\Box$ as well as values for $R_c^{\rm cap}$ and $R_c^{\rm chan}$ of 0.15 $\Omega\cdot$ mm and 2.4 $\Omega\cdot$ mm, respectively. We also measure an uncapped extrinsic $R_{sh}^{\rm chan}$ of 1150 to 1350 $\Omega/\Box$, which agrees closely with the value measured separately beneath the gate, as expected. In the capped extrinsic region, however, $R_{sh}^{\rm chan}$ is reduced to 600 $\Omega/\Box$. The two-fold reduction results primarily from the anticipated increase in n_s, supported by simulation results, and possibly from a consequent improvement in channel electron mobility (μ_e) as well [10].

Two benefits to device performance resulting from this cap-induced reduction in $R_{sh}^{\rm chan}$ are reflected in peak g_m and I_D. Comparing g_m versus V_{GS} at $V_{DS} = 4$ V for both capped and uncapped 1.7 μm $\times$ 30μm HFET's, we find that the capped device achieves peaks values for g_m and I_D of 180 mS/mm and 400 mA/mm, respectively, compared with 85 mA/mm and 250 mA/mm for the uncapped device. Furthermore, while g_m for the capped device degrades upon the onset of significant gate leakage beyond $V_{GS} = 1$ V, the uncapped device shows a gradual decline in g_m beginning at about $V_{GS} = 0.25$ V. This is most likely due to velocity-saturation effects in the relatively low-n_s extrinsic device [1].

These performance benefits of the cap are not fully explained as due simply to a cap-induced increase in extrinsic n_s, however. We find that peak g_m in our devices varies by less than 10% over source-gate separations (L_{sg}) spanning 2 μm to 10 μm, corresponding to a less than 0.5 $\Omega\cdot$ mm variation in r_s. This variation is an order of magnitude less than expected based on the 600 $\Omega/\Box$ $R_{sh}^{\rm chan}$ value of the capped extrinsic channel alone, suggesting considerable conduction by the low-R_{sh} cap itself as predicted by reported two-layer extrinsic region models [5], [6].

We explore the behavior of the extrinsic region in detail by profiling R_S and r_s versus I_S ($I_S \simeq I_D$ for a well-designed HFET at typical operating biases) directly for the extrinsic source, using the gate-current-injection technique [8] illustrated in the inset of Fig. 1. Except at very small I_S, the measured V_{DS} represents quite closely the potential drop across the parasitic source, which we shall

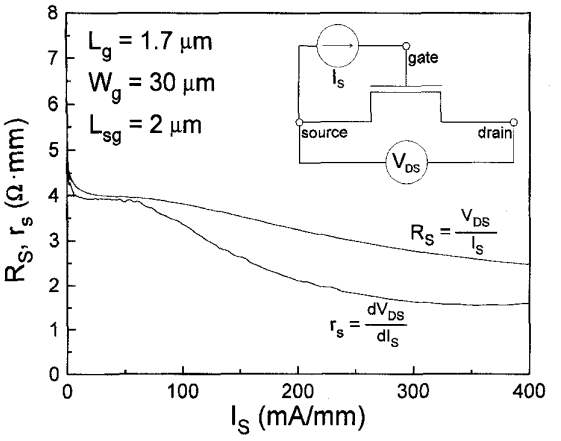

Fig. 1. R_S and r_s versus I_S for $L_{sg} = 2\,\mu$m, measured using the gate-current-injection method show as inset.

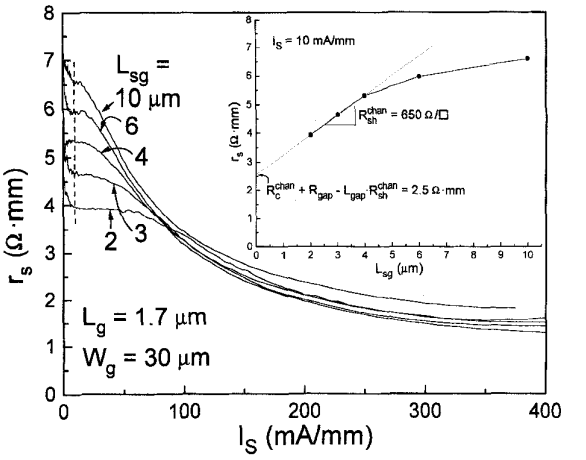

Fig. 2. r_s versus I_S for various values of Lsg. Inset shows r_s versus L_{sg} at $I_S = 10$ mA/mm (indicated on main graph by dashed line).

subsequently write as $(V_{S0} - V_S)$ (where V_{S0} is the potential at the end of the extrinsic source nearest the gate and V_S is the potential of the source contact). The ratio $(V_{S0} - V_S)/I_S$ yields R_S while the derivative $d(V_{S0} - V_S)/dI_S$ yields r_s.

Fig. 1 shows the result for a nominal L_{sg} value of 2 μm. As I_S increases from 0, R_S and r_s initially drop rapidly up through $I_S \simeq$ 8 mA/mm before stabilizing to a constant value of about 4 $\Omega\cdot$ mm. The initial drop is due to an unwanted channel-resistance component that quickly becomes negligible beyond $I_S \simeq 8$ mA/mm. As I_S is increased further, we find that both R_S and r_s remain constant at 4 $\Omega\cdot$ mm over the low-current range up to $I_S \simeq 80$ mA/mm, the behavior associated with a typical, linear source resistance.

Beyond $I_S \simeq 80$ mA/mm, however, R_S and r_s begin a continuous decline, with r_s dropping most rapidly to a value of only $\sim$1.5$\Omega\cdot$ mm by the time I_S reaches 400 mA/mm. The resulting low r_s at higher currents permits excellent peak values for figures of merit such as g_m and $f_{\max}$, despite the higher value of the large-signal resistance R_S.

Focusing on r_s, a comparison between r_s versus I_S scans for various values of L_{sg} between 2 μm and 10 μm reveals distinct low- and high-current scaling trends, as illustrated in Fig. 2. At low currents, where r_s is constant with I_S, we find that r_s increases significantly as L_{sg} is scaled up. We also note that while the $L_{sg} = 2\,\mu$m devices shows a relatively large I_S window over which r_s remains constant before declining, this width of this window decreases with increasing L_{sg}, virtually disappearing for $L_{sg} > 6\,\mu$m. As I_S increases, however, and r_s begins to decline, the L_{sg} dependence observed at low currents disappears completely. Indeed, we find that all the curves merge (within statistical device variation) once I_S exceeds 100 mA/mm. This behavior is responsible for the remarkable lack of L_{sg}-dependence in the values of peak g_m for our devices mentioned above.

III. Discussion

The behavior of r_s versus I_S observed above fits well with the predictions of a full two-layer model that includes transport in the cap layer and electron transfer between cap and channel [5], [6]. We sketch such a model for the source region in Fig. 3. A similar model applies to the extrinsic drain, but with current traveling in the opposite direction. In this model, the cap/barrier/channel layer structure forms a diode, with the capped extrinsic source region thus modeled as a distributed diode-resistor network. Because of the presence of this diode, coupling between cap and channel is extremely weak at low I_S and the channel-cap transfer length (L_T) is therefore large compared

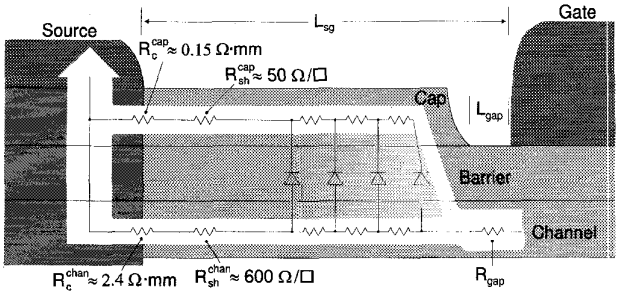

Fig. 3. Schematic cross-section of the extrinsic source region of an InAlAs/n$^+$-InP HFET, illustrating current transfer between the n$^+$-InGaAs cap and n$^+$-InP channel.

with our L_{sg} range. Almost all current is thus initially carried by the $R_{sh}^{\rm chan} = 600\ Omega/\square$ channel layer and we observe a constant r_s that scales up with increasing L_{sg}.

We explore this scaling behavior with L_{sg} in the inset to Fig. 2, which plots r_s measured at $I_S = 10$ mA/mm versus L_{sg}. For the smallest three L_{sg} values, we find that r_s scales up linearly with L_{sg} in a manner consistent with a simple, linear parasitic source resistance proportional to the source-gate separation. This scaling begins to fail for devices with $L_{sg} > 6$ μm, suggesting that $L_T < 6$ μmeven at $I_S = 10$ mA/mm. From slope of r_s versus L_{sg} for $L_{sg} \lesssim 4$ μm, we extract $R_{sh}^{\rm chan} = 650\ \Omega/\square$ for the capped channel, matching our FGTLM results. In addition, linear extrapolation to the r_s-axis yields a value of 2.5 $\Omega\cdot$ mm corresponding to the residual components of the low-current source resistance: $R_c^{\rm chan}$, uncapped gap resistance $R_{\rm gap}$, and a term $[-L_{\rm gap} \cdot R_{sh}^{\rm chan}]$ correcting for the fact that the cap does not extend the full source-gate separation. We bound $L_{\rm gap}$ to be within 0.1 μm based on our cap recess process details, yielding an upper limit for this term of $\sim$0.06 $\Omega\cdot$ mm. Based on this bound, the extrapolated resistance from the plot, and the value for $R_c^{\rm chan}$ measured via FGTLM, we extract the gap resistance $R_{\rm gap}$ of $\sim$0.16$\Omega\cdot$ mm. This value is consistent with a 0.1 μm uncapped gap and the value of the uncapped $R_{sh}^{\rm chan}$ extracted previously.

As I_S increases further, current passing through the extrinsic channel begins to generate a relatively large potential drop in this layer, which also approximates the voltage across the cap/barrier/channel diode in the region nearest the gate. At sufficiently high I_S this voltage grows large enough for the diode to turn on and for significant

current to transfer into the cap. The largest transfer occurs nearest the gate where the diode voltage is greatest, with a rapid falloff toward the source. As I_S increases, L_T thus quickly shrinks, dropping well below L_{sg}. Since the overall source-gate resistance of the cap, including R_c^{cap}, is only about 0.25 $\Omega\cdot$ mm compared with 3.5 $\Omega\cdot$ mm for the underlying channel, r_s declines rapidly with increasing I_S and becomes very insensitive to L_{sg} as observed.

The onset of the r_s decline with increasing bias (which we define as a drop to 90% of low-current r_s) thus marks the bias at which the L_T has decreased to become comparable to L_{sg} for a given device. Since this transfer length is determined by the nonlinear coupling between channel and cap, we expect it be a function of $(V_{S0}-V_S) = I_S \cdot R_S$. For longer L_{sg} devices, this voltage is attained at lower I_S. In addition, L_T need not shrink as much in long L_{sg} devices in order to achieve $L_T < L_{sg}$ and initiate a decline in r_s. Thus, we expect the decline in r_s for longer L_{sg} devices to begin at lower I_S, consistent with the behavior previously observed in Fig. 2.

By noting the value of $(V_{S0} - V_S)$ at which r_s begins to decline for a particular L_{sg}, we can estimate the value of L_T corresponding to this bias. Performing this extraction over a range of L_{sg} values leads to a profile of L_T versus $(V_{S0} - V_S)$, from which we estimate that the channel-cap diode begins to turn-on at approximately 0.22 V. This value is consistent with the thermionic-emission barrier height from the cap to the gate-barrier layer.

While we expect the decline in r_s with increasing I_S to apply to all capped HFET structures in the III-V material systems, the rate and onset of this decline should depend on both R_{sh}^{chan} and on the diode I-V curve of a given cap/barrier/channel structure. The consequences of this dependence are well illustrated by contrasting Fig. 2 in this work with Fig. 10 of [6]. This work models R_S versus I_D for pseudomorphic HEMT structures. The predicted decline in r_s with current in these HEMT's qualitatively matches our reported results quite well. However, instead of displaying a low-current bias range in which r_s remains flat, the decline in r_s begins immediately as I_S rises from 0 V due to the much smaller diode turn-on voltage characteristic of a HEMT's doped barrier layer.

IV. Conclusions

We find through direct experimental measurement that a cap technology is effective at reducing parasitic source and drain resistance through two distinct mechanisms. The cap reduces the underlying channel sheet resistance by a factor of two, through the well-known screening of surface Fermi-level pinning. In addition, however, we also observe a dramatic reduction in both the large- and small-signal source and drain resistances at moderate-to-high currents through a parallel cap-conduction mechanism. This existence of this phenomenon is key to achieving high-performance in a process with large source-drain separation for relaxed lithographic tolerance in a manufacturing environment.

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The Effect of Drain Offset on Current-Voltage Characteristics in Sub Micron Polysilicon Thin-Film Transistors

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***Abstract*—We have examined the effect of drain offset structures with lengths ranging from 0.0 μm to 1.0 μm on submicron polysilicon TFT devices. The drain offset was found to exhibit resistive behavior that tends to lower the TFT drive current as it reduces the leakage current. For the range of channel lengths studied (1.0 μm to 0.35 μm) the optimum drain offset length was 0.35 μm.**

I. Introduction

Polysilicon thin-film transistor (TFT's) have been widely investigated for active matrix liquid crystal display (AMLCD's). In addition to their higher current drive capability [1], polysilicon TFT devices offers the flexibility of being used to build peripheral drive circuitry on the same substrates to interface with AMLCD. Since the electric-field at the drain side of a TFT is maximum in the off-state, the use of the drain offset structure reduces the penetration of drain depletion width, and consequently the electric field. In this brief, we present a model that describes the effect of drain offset on the drive and the leakage current of polysilicon TFT.

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