$Si/Si_{1-x}Ge_x$ Valence Band Discontinuity Measurements Using a Semiconductor-Insulator-Semiconductor (SIS) Heterostructure

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***Abstract*— We have measured the valence-band discontinuity of strained $Si_{1-x}Ge_x$ on (100) unstrained Si using $p-Si_{1-x}Ge_x/Si/p-Si_{1-x}Ge_x$ semiconductor-insulator semiconductor (SIS) structures with Ge compositions in the range $10 < x < 25\%$. The epitaxial heterostructures were grown by ultra-high-vacuum chemical-vapor-deposition. A new data analysis procedure is proposed for extracting small ΔE_v values out of the current-voltage characteristics of the SIS heterostructures as a function of temperature. Our data indicates that the valence band discontinuity between Si and $Si_{1-x}Ge_x$ can be approximated by $\Delta E_v = 6.4x$ meV for $0 < x < 17.5\%$.**

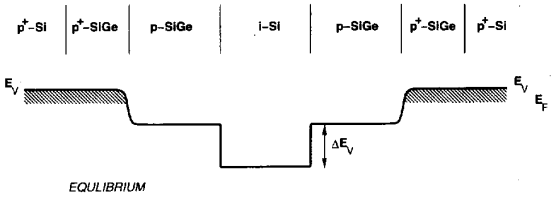

Fig. 1. Conceptual band diagram of a p-$Si_{1-x}Ge_x/i$-Si/p-$Si_{1-x}Ge_x$ SIS heterostructure in equilibrium.

I. Introduction

THE growth of high-quality strained $Si_{1-x}Ge_x$ epitaxial layers on Si substrates has recently led to the demonstration of a wealth of Si-compatible heterojunction devices [1], [2], among which heterojunction bipolar transistors (HBT) have stirred considerable interest [3]–[6]. To a large extent, the conduction and valence band discontinuities, ΔE_c and ΔE_v respectively, determine the electronic properties of a heterojunction system. Because of this, accurate knowledge of band alignments is essential to designing heterojunction devices.

To date, the total bandgap difference, ΔE_g, of the $Si/Si_{1-x}Ge_x$ heterojunction system is relatively well known. It has been predicted by theoretical calculations [7] and verified experimentally [8]. In contrast, there remain serious discrepancies about the precise value of the valence band discontinuity [9]. Theoretical band alignment calculations [10], [11] predict $\Delta E_v \approx \Delta E_g$. Results of several experimental measurements of ΔE_v present a conflicting picture [12]–[21]. For device applications, it is particularly problematic that very few device-type measurements of ΔE_v have been reported for low Ge compositions ($x < 20\%$), a regime of importance for HBT's and other devices. Below $x = 20\%$, only the recent data of Brighten *et al.* [19], [20] are available and they are obtained by a capacitance-voltage technique which is known to be very vulnerable to the presence of traps [22].

In view of this situation, there is a need for transport-based device-type measurements of ΔE_v for strained $Si_{1-x}Ge_x$ on unstrained Si substrates, especially for low Ge compositions. The purpose of this work is to fill this gap. We have used a specially designed semiconductor-insulator-semiconductor (SIS) heterostructure. This symmetric structure demonstrated its worth by settling the controversy about the band alignment in the GaAs/AlGaAs heterojunction system [23], [24] and has been subsequently used in a large number of III–V compound semiconductor systems [25]–[28]. To the knowledge of the authors, it has never been used in the $Si/Si_{1-x}Ge_x$ system.

II. Theory

A Semiconductor-Insulator-Semiconductor heterostructure consists of an undoped wide bandgap material sandwiched between two doped narrow bandgap layers, as schematically illustrated for the $Si/Si_{1-x}Ge_x$ system in Fig. 1. In equilibrium, this heterostructure has a symmetric square-shaped potential barrier which lends itself to simple analysis and allows accurate extraction of band discontinuities. This section summarizes the theory of the electrostatics and the current-voltage (I-V) characteristics of this structure and presents the scheme used to extract ΔE_v. This description is necessary since a number of assumptions that have become common in the III–V literature need to be carefully reviewed in light of the small values of ΔE_v expected in the $Si/Si_{1-x}Ge_x$ system.

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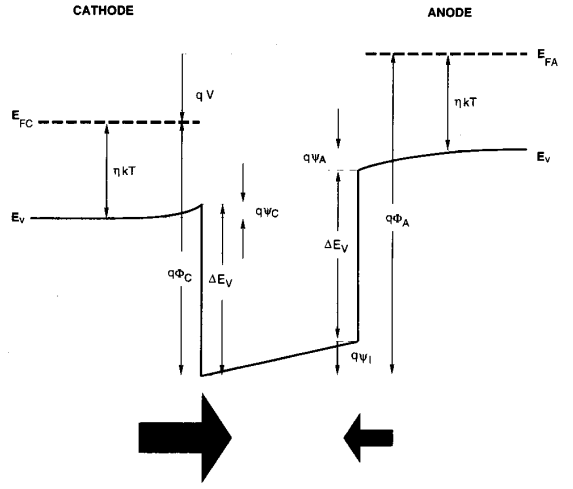

Fig. 2. Valence band schematic of SIS heterostructure under bias V. E_{FC} and E_{FA} are the quasi-Fermi level of the cathode and the anode layers, respectively. The black arrows indicate hole flow. The size of the arrows is to illustrate the relative magnitude of the hole flow under the indicated bias.

In our work, as Fig. 1 indicates, we assume that ΔE_v is identical for both heterojunctions and is independent of temperature. We also assume that the middle Si barrier layer is undoped and the $Si_{1-x}Ge_x$ layers are equally p-type doped to a non-degenerate level. Highly doped p^+-$Si_{1-x}Ge_x$ and p^+-Si layer structures are placed on both sides of the S-I-S heterostructure in order to provide low resistivity contacts to the outside world.

When a small bias V is applied to one terminal of the SIS structure with respect to the other, the band diagram tilts as sketched in Fig. 2. We label as cathode the $Si_{1-x}Ge_x$ layer with the more positive potential, and as anode the $Si_{1-x}Ge_x$ layer with the more negative potential. In this notation, the cathode injects holes over or through the barrier which are then collected by the anode. Since the structure is symmetric, all electrical characteristics should be symmetrical about zero bias. Over a certain range of bias and temperature, thermionic emission of holes over the barrier layer from the cathode to the anode is expected to limit the current transport in the device. Under such conditions, the hole current is thermally activated and from the activation energy, ΔE_v can be extracted with minimal assumptions [24].

ΔE_v for $Si_{1-x}Ge_x$ on unstrained (100) Si for compositions of practical interest is considerably smaller than in the GaAs/AlGaAs and other III–V heterojunction systems. This restricts the temperature range in which hole thermionic emission dominates. At high temperatures, we have experimentally found that thermionic emission dominates only when $5kT$ does not exceed ΔE_v (see experimental results below). This puts an upper limit to the measurement temperature. At low temperatures, thermionic emission is suppressed and tunneling across the barrier dominates hole transport. Tunneling is enhanced for low ΔE_v barriers and high bias. Therefore, to minimize tunneling and extend the thermionic emission temperature range at low temperatures, *small* biases must be used.

The following four equations describe the electrostatics of the intrinsic SIS heterostructure [29]:

$$V = \psi_C + \psi_I + \psi_A \tag{1}$$

$$\epsilon_C \mathcal{E}_C = \epsilon_I \mathcal{E}_I = \epsilon_A \mathcal{E}_A \tag{2}$$

$$\mathcal{E}_s = \frac{kT}{q} \cdot \frac{\sqrt{2}}{L_D} F\left(\frac{q\Psi_s}{kT}, \frac{n_0}{p_0}\right) \tag{3}$$

$$F\left(\frac{q\Psi}{kT}, \frac{n_0}{p_0}\right) = \frac{\Psi}{|\Psi|}\left[\exp\left(-\frac{q\Psi}{kT}\right) + \frac{q\Psi}{kT} - 1 + \frac{n_0}{p_0}\left(\exp\left(\frac{q\Psi}{kT}\right) - \frac{q\Psi}{kT} - 1\right)\right]^{\frac{1}{2}}. \tag{4}$$

Equation (1) describes how an applied bias V is distributed in the band bending of an accumulation layer in the cathode, ψ_c, the voltage drop across the Si barrier layer, ψ_I, and band bending in the depletion region in the anode, ψ_A, as shown in Fig. 2. Equation (2) matches the electric displacement, $D = \epsilon\mathcal{E}$, at the two heterojunction interfaces in the absence of interface charge (an assumption in this work). This uniquely determines a relationship between the electrostatic potential drops ψ_C, ψ_I and ψ_A. ϵ_C and ϵ_A are the dielectric permittivities of the cathode and anode $Si_{1-x}Ge_x$ layers respectively. ϵ_I is the permittivity of Si. $\mathcal{E}_I$, the electric field across the undoped Si insulator layer, is constant for the undoped Si barrier layer. $\mathcal{E}_C$ and $\mathcal{E}_A$ are the surface electric fields at the cathode-insulator and anode-insulator interfaces, respectively.

Equation (3) describes the relationship between the surface electric field on the narrow bandgap side at one of the heterojunction interfaces, $\mathcal{E}_s$, and the corresponding potential dropped in the $Si_{1-x}Ge_x$ semiconductor, Ψ_s. For the cathode (anode), $\mathcal{E}_s$ becomes $\mathcal{E}_C$ ($\mathcal{E}_A$) at the cathode (anode)-insulator interface and Ψ_s becomes ψ_C (ψ_A). In (3), L_D is the Debye length in the $Si_{1-x}Ge_x$ layer, T is the temperature, k is Boltzmann constant, q is the electron charge, p_0 and n_0 are the equilibrium hole and electron concentration, respectively. Finally, the function $F(\frac{q\Psi}{kT}, \frac{n_0}{p_0})$ in (3) is given in (4) for a p-type semiconductor. The effective hole mass and permittivities of SiGe required by the model are interpolated between those of Si and Ge. The effects of unintentional doping in the Si barrier layer will be discussed and resolved in the discussion section.

We have built a computer model that numerically solves these equations by starting from an anode potential, ψ_A, to obtain the anode-insulator surface electric field, $\mathcal{E}_A$, using (3). The electric field in the Si barrier layer, $\mathcal{E}_I$ and the surface electric field at the cathode-insulator interface, $\mathcal{E}_C$, are obtained from the boundary conditions in (2). Since $\mathcal{E}_I$ is constant in the undoped barrier layer, the potential dropped across the barrier layer is

$$\psi_I = \mathcal{E}_I W_I \tag{5}$$

where W_I is the barrier layer width. With $\mathcal{E}_C$, ψ_C is numerically solved from (3). Once ψ_I and ψ_C are obtained from a fixed value of ψ_A, the electrostatic potentials are summed to obtain V using (1).

With the electrostatics now fully described, we now turn to the simulation of current transport in the SIS structure. In the

thermionic emission regime, the hole current can be modeled as in [23]:

$$J = A^*T^2\left[\exp\left(-\frac{q\Phi_C}{kT}\right) - \exp\left(-\frac{q\Phi_A}{kT}\right)\right] \quad (6)$$

where J is the current density and A^* is the effective Richardson's constant (in our simulations, we have used the value of $A^* = 79.2$ A/cm^{2}K^2 that corresponds to Si [30] since holes are thermionically injected from the $Si_{1-x}Ge_x$ layers into the Si barrier; this choice, as shown below, does not affect the extraction of ΔE_v).

Holes thermionically emitted from the cathode to the anode confront the energy barrier $q\Phi_C$ and holes emitted in the reverse direction from the anode to the cathode have to surmount the energy barrier $q\Phi_A$. The two exponential terms in (6) reflect the exponential dependence of the current on these two energy barriers. With no applied bias V, the two barriers are equal and no current flows. With an applied bias such that $\Phi_A \gg \Phi_C$, many authors simplify (6) by discarding the exponential Φ_A term because holes emitted from the cathode overwhelm those 'back' emitted from the anode. Although this approximation is appropriate for biases $V > 3kT$, we will show in subsequent analysis that it is not accurate enough to extract barrier information at *small* biases—the conditions needed to minimize tunneling and accurately extract small ΔE_v, as argued above.

From Fig. 2, Φ_C can be expressed as

$$q\Phi_C(V,T) = \Delta E_v - q\psi_C(V,T) - \eta(T)kT = \Delta\hat{E}_v - \eta(T)kT \quad (7)$$

where we define the effective energy barrier, $\Delta\hat{E}_v$, as

$$\Delta\hat{E}_v = \Delta E_v - q\psi_C(V,T). \quad (8)$$

The band bending at the accumulated cathode-insulator interface, ψ_C, depends weakly on temperature and bias. $\psi_C(V,T)$, however, vanishes at zero bias for all temperatures. Hence, $\Delta\hat{E}_v$ reduces to ΔE_v at zero bias from (8). We will use this fact later to obtain ΔE_v.

$\eta(T)$ in (7) is the reduced Fermi level position with respect to the valence band in the bulk of the $Si_{1-x}Ge_x$ layers. We define it to be negative in a non-degenerate semiconductor. Since thermionic emission is a thermally activated mechanism, it is essential to account for all temperature dependent terms such as $\eta(T)$ in the extraction process, particularly in our case of non-degenerate $Si_{1-x}Ge_x$ layers. The need for accurate models of $\eta(T)$ in the determination of ΔE_v in SIS heterostructures has been recognized [24]. A calculation of $\eta(T)$ requires the incorporation of freeze-out effects if the doping level is below the Mott transition. Since no freeze-out model currently exists for p-type $Si_{1-x}Ge_x$, we use Li's model for boron-doped Si [31].

We can separate Φ_A into its various components as was performed for Φ_C in (7). Fortunately, Fig. 2 shows that Φ_A is related to Φ_C in the following way:

$$\Phi_A = \Phi_C + V. \quad (9)$$

We substitute (9) into (6) and rearrange to obtain:

$$\log\frac{J}{T^2[1-\exp(-\frac{qV}{kT})]} = \log A^* - \frac{q\Phi_C(V,T)}{kT}. \quad (10)$$

The expression $1 - \exp(-\frac{qV}{kT})$ in the denominator inside the logarithm of the left-hand side accounts for the 'back' thermionic emission from the anode layer and it becomes significant at small biases. This term has always been ignored in the SIS literature because of the large biases typically utilized.

With Φ_C broken down into its various components, we substitute (7) into (10) and move all temperature dependent components of Φ_C to the left side to obtain:

$$\log\frac{J}{T^2[1-\exp(-\frac{qV}{kT})]} - \eta(T) - \frac{q\Phi_C(V,T)}{kT} = \log A^* - \frac{\Delta E_v}{kT}. \quad (11)$$

Thus if we plot the left hand terms versus $1/T$ in an Arrenhius format for a given bias, the slope of the curve yields ΔE_v. Since all temperature terms are accounted for in the left-hand side, all bias points yield the same value of ΔE_v.

The approach described in (11) demands that $\eta(T)$ and $\psi_C(V,T)$ be known. $\eta(T)$ can be modelled rather accurately from a knowledge of the doping level. Errors can easily creep in a calculation of $\psi_C(V,T)$. Fortunately, we can use the fact that ψ_C vanishes at zero bias and rewrite (11) as

$$\log\frac{J}{T^2[1-\exp(-\frac{qV}{kT})]} - \eta(T) = \log A^* - \frac{\Delta\hat{E}_v}{kT} \quad (12)$$

where we have used the expression of $\Delta\hat{E}_v$ from (8). This extraction scheme draws out $\Delta\hat{E}_v$ instead of ΔE_v from the slopes of the Arrenhius plots of (12). Unlike the previous extraction, $\Delta\hat{E}_v$ depends on bias and temperature. As more bias is applied, the band-bending at the accumulated cathode-insulator interface, ψ_C, increases resulting in a decrease of $\Delta\hat{E}_v$. This difference, however, disappears at zero bias because $\psi_C(V,T)$ vanishes at zero bias for all temperatures. Hence, the extrapolation of $\Delta\hat{E}_v$ to zero bias gives ΔE_v accurately.

Fig. 3 illustrates the ΔE_v extraction methodology described by (12) for a hypothetical structure with a ΔE_v of 150 meV. We compare the results of our extraction scheme (12), displayed in solid line), with the conventional way (open circles) based on the following equation:

$$\log\frac{J}{T^2} - \eta(T) = \log A^* - \frac{\Delta\hat{E}_v}{kT} \quad (13)$$

where the term inside the square brackets in (12) has been droped, as done by most authors for $V > 3kTs$. We see from the figure that at small biases, the $1 - \exp(-\frac{qV}{kT})$ term plays an extremely important role in producing a correct extraction of ΔE_v and cannot be ignored.

III. Experimental

A schematical cross section of the heterostructure device is shown in Fig. 4. Device fabrication was carried out on B-doped (100) p^+-Si substrates with a resistivity of 0.016 Ω·cm.

TABLE I
SUMMARY OF KEY HETEROSTRUCTURE PARAMETERS

sample ID	Ge%	thickness (Å)				doping (cm^{-3})		
		Si cap	front SiGe	Si barrier	back SiGe	front SiGe	Si barrier	back SiGe
D6	10.0	743	600	500	571	8×10^{16}	5×10^{16}†	8×10^{16}
D4	16.5	1000‡	652	284	908	5×10^{16}	7×10^{16}†	1×10^{17}
D5	17.0	1000‡	500‡	500‡	500‡	9×10^{16}‡	N/A	9×10^{16}‡
D9	17.5	743	257	457	214	7×10^{18}	2×10^{17}†	7×10^{18}
D7	25.0	185	207	110	240	9×10^{16}‡	N/A	9×10^{16}‡

† unintentional doping ‡ nominal value N/A not available

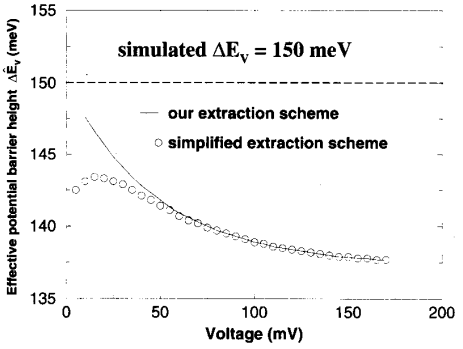

Fig. 3. ΔE_v extracted from the Arrenhius plot using different extraction schemes. A hypothetical structure of $\Delta E_v = 150$ meV is assumed. The solid line used (12) and the circles used (13). The circles extrapolate to a ΔE_v value 5 meV less than the actual ΔE_v value.

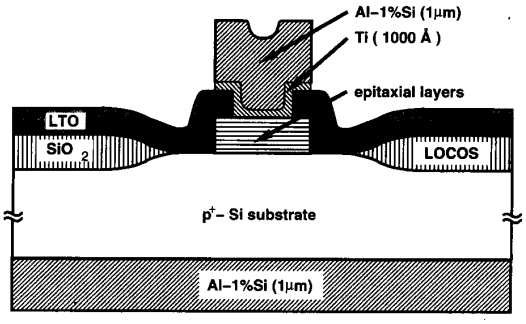

Fig. 4. Schematic cross section of the fabricated SIS heterodiodes.

After LOCOS for device isolation, SIS heterostructures were grown using ultra-high-vacuum chemical-vapor-deposition (UHV/CVD) with the reactor nominally set at 550°C ($\simeq$ 500°C wafer temperature) [2], [32]. For the sample with $x = 25\%$, the nominal reactor temperature was 500°C. Unpatterned dummy wafers for material characterization were also grown simultaneously on a p-Si substrate.

A typical device heterostructure consist of three main portions: the back contact layers, the SIS structure and the front contact layers. Epitaxial growth began with a p^+-doped layer sequence to provide good contact to the substrate and allow terminal access from the wafer back. The layer structure consist of an initial 100 Å p^+-Si buffer and a final 100 Å p^+-$Si_{1-x}Ge_x$ contact to the SIS structure. An approximately 33 Å thick Ge composition ramp was inserted between the growth of the two layers to grade the p^+-Si/p^+-$Si_{1-x}Ge_x$ interface. The grading helps prevent barrier spiking effects caused by abrupt junction growth. All layers are doped with $N_A = 1 \times 10^{19}$ cm^{-3}.

The SIS structure is subsequently grown. It consists of 200 to 1000 Å p-$Si_{1-x}Ge_x$ layers Boron-doped between 8×10^{16} and 7×10^{18} cm^{-3} sandwiching a nominally undoped Si barrier ranging from 110 to 500 Å in thickness. The bottom interface includes a 16 Å spacer layer to ensure abrupt Ge and doping transitions at the heterojunction interface. The top heterojunction interface has first a 16 Å ramp to reach the desired Ge composition followed by another 16 Å spacer for the doping concentration to catch up. Structure parameters for the SIS heterostructures of the samples used in this work are listed in Table I.

Finally, highly p^+-doped front ohmic contact layers for terminal access from the wafer front complete the heterostructure. These layers consist of an initial 100 Å p^+-$Si_{1-x}Ge_x$ followed by a final 185 to 743 Å p^+-Si cap. A $\simeq$ 33 Å Ge grading was performed again between the p^+-$Si_{1-x}Ge_x$ layer and the final cap. The p^+-Si_{1-x} Ge_x layer is doped with B to 1×10^{19} cm^{-3} and the top p^+-Si cap is doped to 1×10^{20} cm^{-3}.

The Ge compositions, layer thicknesses and the doping levels of the samples were designed around various constraints. Three Ge compositions were selected: 10%, 17%, and 25%. Overall device design precluded us from keeping the $Si_{1-x}Ge_x$ layers below the Matthews–Blakeslee critical layer thickness limit [33], as would have been desirable. However, in every heterostructure, the total SiGe thickness was kept below experimental reports of high quality fully strained but metastable layers [34]–[41]. This means that our samples are probably in a relaxation-prone state. To ensure that the $Si_{1-x}Ge_x$ layers remain fully coherent after device fabrication, we designed all post-growth thermal steps so that the processing temperature do not exceed the growth temperature of the heterostructures.

Optimal doping values of the $Si_{1-x}Ge_x$ layers were selected based on computer simulations. From discussions in the previous section, we can choose to minimize the errors associated with the band-bending at the accumulated cathode-insulator interface, $\psi_C(V,T)$, under an applied bias by increasing the doping concentration of the $Si_{1-x}Ge_x$ layers. However, we avoided doping the layers so much that we had to worry about heavy doping effects. For a composition around 17%, the impact of doping was experimentally studied by growing an additional sample with SiGe layers doped degenerately. We also grew two samples at $x = 17\%$ with different Si barrier thicknesses to test the impact of insulator thickness on the

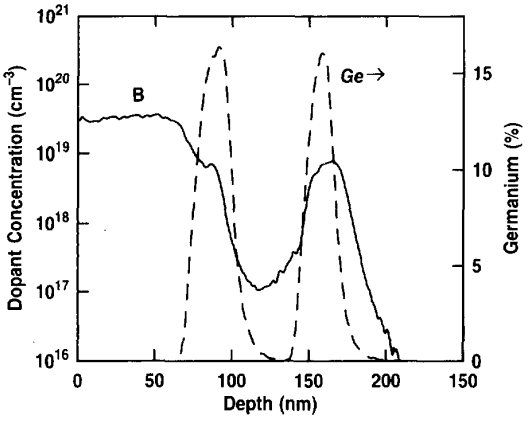

Fig. 5. SIMS profile of a calibration sample grown on lightly doped substrate with $x = 17.5\%$.

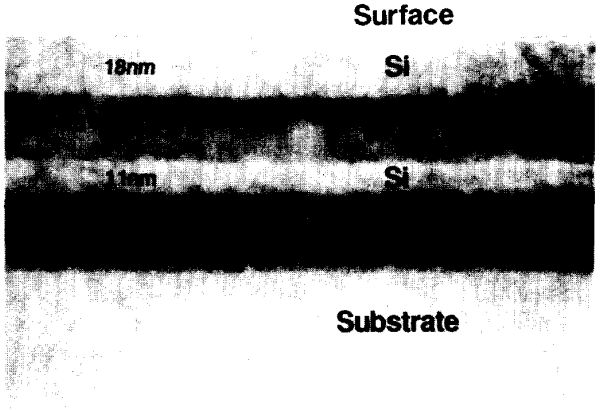

Fig. 6. Cross-sectional TEM profile of calibration sample with $x = 25\%$.

tunneling current across the barrier at small biases, a parasitic path to be minimized.

After heterostructure growth, device processing proceeded as follows [42]. Mesa isolation was performed by dry etching. The mesa dimensions, ranging from 6.25×10^{-6} to 9×10^{-4} cm^2, are smaller than the LOCOS windows as shown in Fig. 4. The mesa sidewalls were then passivated by depositing 3000 Å of low-temperature oxide (LTO) at 400°C. Contact holes were opened by first using reactive ion etching (RIE) to remove all but 500 Å of the oxide. The remaining oxide was later removed in a 50:1 H_2O:buffered HF solution. This scheme prevents overetching into the thin Si cap layer. We contacted the wafer front by first sputtering a 1000 Å Ti layer followed by 1 μm of Al-1%Si. The Ti barrier layer prevented the Al from spiking through the thin Si cap layer and destroying the device during contact sintering. The wafer back was contacted using 1 μm of Al-1%Si. After patterning the metal, the contacts were sintered in forming gas at 400°C for 30 minutes.

The wafers were subsequently die-sawed and mounted into chip carriers for temperature-dependent measurements

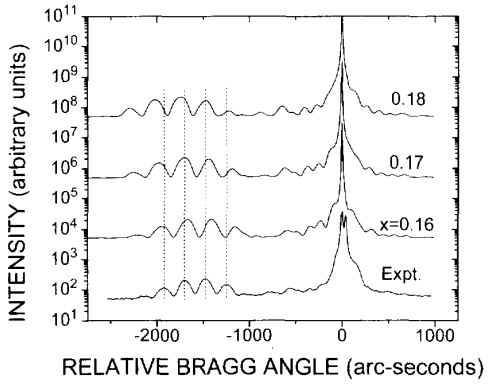

Fig. 7. Measured (bottom trace) and simulated (top three traces) (004) Double-Crystal X-ray Diffraction spectra of calibration sample for $x = 17.5\%$. The best simulated fit to data is corrected +0.5% due to Vegard's law deviations [43].

in a variable-temperature liquid-helium cryostat system. The cryostat controlled the temperature from 4 to 250 K with a resolution of 1 K. With the wafer back at ground and voltage applied to the device front, current-voltage characteristics were obtained.

IV. Results

The heterostructures were characterized by a variety of techniques. Layer thicknesses were derived from extensive calibration prior to the device runs using secondary ion mass spectroscopy (SIMS) and cross section transmission electron microscopy (XTEM), as shown in Figs. 5 and 6, respectively. The combination of these measurements give an uncertainty in layer thicknesses of less than 10%. Ge composition was determined from Rutherford back scattering (RBS), symmetric (004) double-crystal X-ray diffraction (DCXD) (Fig. 7), and Auger spectroscopy. A close fit between the raw RBS spectra and the computer simulation based on layer thicknesses derived from XTEM data was obtained for sample D7. Auger spectroscopy on the same sample confirms the Ge composition of 25%. The DCXD data in Fig. 7 shows a good fit between the raw spectra and the results of a simulation using dynamic diffraction theory for sample D9 ($x = 17\%$). All compositions were corrected by known deviations to Vegard's law [43]. This was a small correction. For example, for sample D9 it represents only an increase in the Ge mole fraction from 17% to 17.5%. All together, the Ge composition is obtained to within one percentage point. Asymmetric (115) DCXD revealed that with the exception of the sample with $x = 25\%$, all heterostructures are fully coherent within the resolution of the technique. The sample with $x = 25\%$ was found to be 25% relaxed after growth.

The doping levels are obtained from SIMS (Fig. 5) with a resolution of 30%. Fig. 5 reveals a boron doping concentration between 5×10^{16} and 2×10^{17} cm^{-3} in the nominally undoped Si barrier. This is probably due to unintentional boron in the ultra-high-vacuum chamber during the barrier layer growth. We will discuss the implications of this doping to the extraction of ΔE_v measurements in the next section.

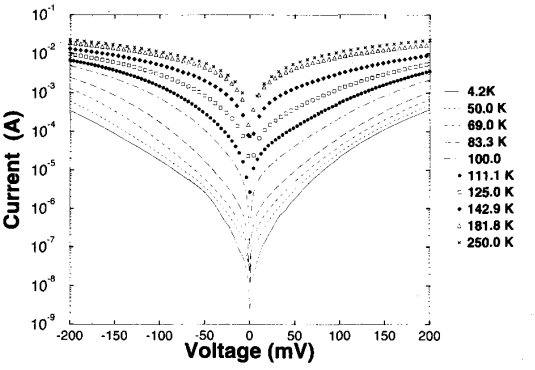

Fig. 8. Current-voltage (I-V) characteristics for a $x = 16.5\%$ sample for selected temperatures. Device area is 4×10^{-4} cm^2.

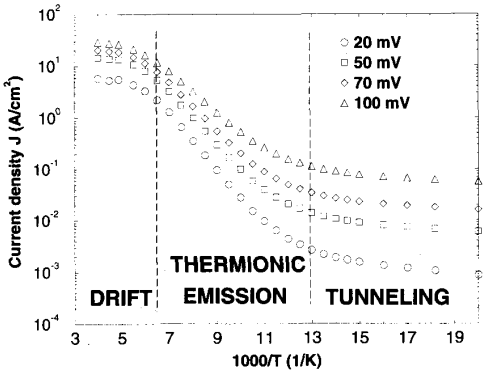

Fig. 9. Current density versus 1000/T for $x = 16.5\%$ sample as a function of bias for selected temperatures showing three distinct current transport regimes.

Typical I-V characteristics measured between 4.2 and 250 K for sample D4 ($x = 16.5\%$) are shown in Fig. 8. The current increases with bias and temperature and it is rather symmetric around $V = 0$. From measurements in neighbouring devices with different dimensions, we determined that the device current scales linearly with the mesa area in the temperature range where thermionic emission dominates. Since the current densities are very small, less than 100 A/cm^2, series resistance effects are negligible.

For selected biases, Fig. 9 shows the current density, J, versus $1000/T$. In this sample, J displays three regimes as a function of temperature. For $T > 160$ K, J appears to be insensitive to T and is probably limited by hole drift through the i-Si barrier. In an intermediate temperature regime, J drops exponentially with T, indicating a dominance of hole thermionic emission. For $T < 77$ K, J becomes independent of T as hole tunneling prevails. The rather narrow temperature range where Fig. 9 shows that the current is thermally activated illustrates the problems with measuring small ΔE_v values discussed in Section II. While nothing can be done about the high temperature end of the thermionic emission regime, the low T portion of it can be extended by minimizing tunneling. This demands the use of very small biases and relatively thick barriers. Fig. 9 in fact shows that tunneling currents are reduced hundredfold at $T = 50$ K when the bias is reduced from 100 mV to 20 mV. In contrast, the thermionic emission current at $T = 100$ K is only reduced tenfold.

Fig. 10 shows the Arrenhius plot of (12) for the same sample as Fig. 9 for selected positive biases. The Arrenhius plot exhibits three regimes similar to those in Fig. 9. In the intermediate thermionic emission regime a least squares method was used to fit the data with a straight line that spans at least three orders of magnitude for all samples. The slopes of the fitted lines yield the effective energy barrier height, $\Delta \hat{E}_v$, at various fixed positive biases. We display the extracted $\Delta \hat{E}_v$ values as a function of bias in Fig. 11 for several heterodiodes at different Ge compositions.

As expected from theory, $\Delta \hat{E}_v$ increases as bias is reduced because the accumulated band bending of the injecting $Si_{1-x}Ge_x$ layer diminishes. In our voltage convention, extrapolating $\Delta \hat{E}_v$ to zero bias from the right or positive

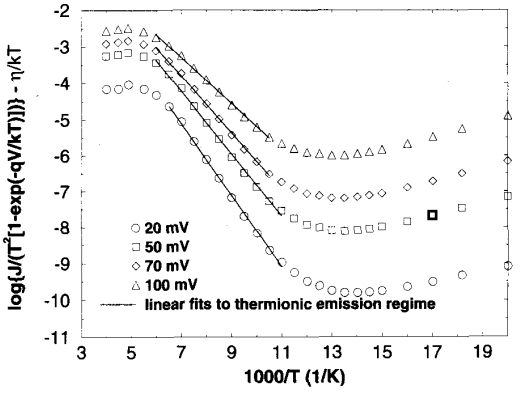

Fig. 10. Arrenhius plot for $x = 16.5\%$ Ge sample for fixed positive biases. Least squares fit are performed in the thermally activated regime and are shown as solid lines.

bias in Fig. 11 gives ΔE_v for the front interface. Similarly, extrapolating from the left or negative bias gives ΔE_v for the back interface. Table II collects these extracted ΔE_v values as a function of Ge composition under the heading "uncorrected." Corrections are required to account for the residual doping in the Si barrier layer. This is discussed in the next Section.

V. Discussion

SIMS analysis in Fig. 5 reveals that the nominally undoped Si barrier layer is moderately doped p-type to about 1×10^{17} cm^{-3}. This was found to be the case for all samples. This unintentional doping results in the formation of two hole accumulation regions on the $Si_{1-x}Ge_x$ side of the $Si/Si_{1-x}Ge_x$ interfaces even in the absence of any applied bias. In this instance, our method of extrapolating $\Delta \hat{E}_v$ to zero bias will *underestimate* the true ΔE_v by the amount of the band bending, as shown by (8).

In order to account for this band bending, we have to calculate the surface electric field at both interfaces of the Si barrier. This calculation is simplified by the fact that simple modeling of the position of the Fermi level with respect to the

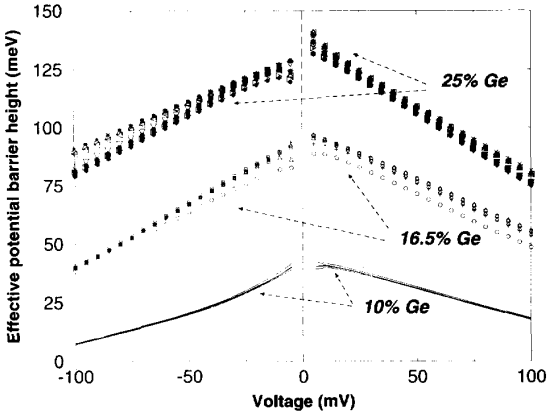

Fig. 11. Effective heterodiode barrier height, $\Delta \hat{E}_v$, as a function of bias at three different compositions. For each composition, measurements on several diodes are shown.

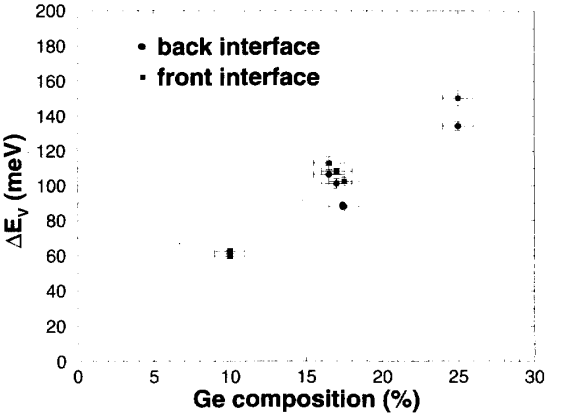

Fig. 12. Extracted ΔE_v for front and back interfaces for all samples as a function of Ge composition. The error bars are shown in solid lines.

TABLE II
TABLE OF FINAL RESULTS. UNCORRECTED ΔE_v REFERS TO RAW DATA RESULTING FROM THE EXTRAPOLATION OF $\Delta \hat{E}_v$ TO ZERO BIAS (SEE FIG. 13). $q\psi_{C0}$ IS THE AMOUNT OF BAND BENDING DUE TO THE RESIDUAL DOPING IN THE INSULATOR. ΔE_v IS THE FINAL VALENCE BAND DISCONTINUITY

Sample ID	x(%)	interface	uncorrected ΔE_v (meV)	$q\psi_{C0}$ (meV)	ΔE_v (meV)
D6	10.0	front	42	18	60
		back	44	19	63
D4	16.5	front	96	18	114
		back	92	14	106
D5	17.0	front	83	26	109
		back	76	25	101
D9	17.5	front	98	5	103
		back	84	4	88
D7	25.0	front	142	8	150
		back	126	8	134

valence band at the center of the barrier indicates that at the temperatures of interest all boron dopants in the barrier layer are ionized and the barrier layer is entirely depleted of holes. Then, the electric field at both interfaces with the barrier at zero bias can easily be obtained from:

$$\epsilon_C \mathcal{E}_C = \epsilon_A \mathcal{E}_A = \frac{qN_I W_I}{2\epsilon_I} \tag{14}$$

where N_I is the ionized boron doping concentration in the insulator layer. Here, we have assumed that the structure is symmetrically doped and hence $\mathcal{E}_C = \mathcal{E}_A$ for both the cathode and anode layers at zero bias.

After obtaining the surface electric field from (14), we numerically solve for the temperature dependent band bending, $\psi_{C0}(T) = \psi_{A0}(T)$, at zero bias from (3) and (4) in the temperature range in which thermionic emission dominates. We found that $\psi_{C0}(T)$ is quite insensitive to temperature in this range. Table II lists the average value of $\psi_{C0}(T)$ for the different samples. We obtain the final ΔE_v value by adding $\psi_{C0}(T)$ to ΔE_v. The final ΔE_v values are collected in Table II and graphed in Fig. 12 as a function of Ge composition.

Error bars for ΔE_v are derived from analyzing the spread of extrapolated $\Delta \hat{E}_v$ values to zero bias, the variation of the zero bias band bending correction in the thermionic emission temperature range $\psi_{C0}(T)$, and the uncertainty of active dopant levels in the $Si_{1-x}Ge_x$ and Si barrier layers. The errors from these three sources are added quadratically and are shown as vertical solid lines in Fig. 12. As determined in the previous section, the error in the Ge composition is ± 1 percentage points. Errors arising from our choice of material parameters were verified to be substantially smaller than the experimental uncertainty. This is because the method relies on the *change* of current with temperature and not on the absolute value of the current. As a result it is the temperature dependence of η that we must model accurately and not its actual value. The choice of material parameters has a very weak impact on the temperature evolution of η.

Fig. 12 shows that ΔE_v increases with Ge composition in an almost linear fashion. Except for the 10% Ge sample, the back interface generally has a lower ΔE_v value than the front interface by an amount between 10 to 20 meV. This difference cannot be atributed to the slight doping asymmetry observed by SIMS. It might however be due to different interface quality at the two heterojunctions that possibly arises from interface roughness [44]. For high Ge compositions, the growth front of the $Si_{1-x}Ge_x$ layer becomes rough on a microscopic scale [44]. When an unstrained Si layer is deposited on top, it smooths out the growth front. As a result, the back interface is in general expected to be rougher than the top one for high Ge compositions. This is consistent with our observations.

The results obtained on the three samples with Ge compositions around 17% provide great confidence in our extraction technique. Two of these samples are identical with the exception of the Si barrier which is 500 Å for one sample and 250 Å for another. The obtained values of ΔE_v are within the resolution of the measurement. This confirms that our extraction technique is not affected by tunneling and that the residual B doping in the Si barrier is correctly accounted for. In a third sample, the doping level in the SiGe layers

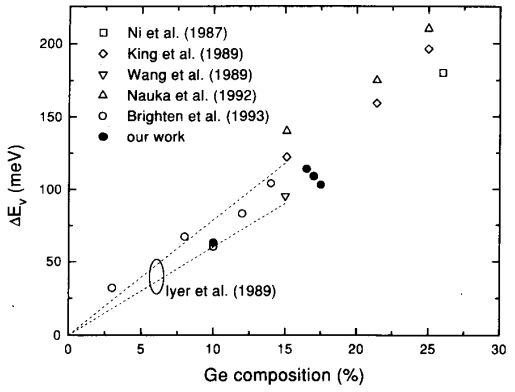

Fig. 13. Summary of experimental measurements of ΔE_v in strained $Si_{1-x}Ge_x$/Si on (100) Si.

was increased by two orders of magnitude. The ΔE_v values extracted from this sample for the anomalous back interface are low but those obtained for the well behaved front interface are identical to the other samples of the same composition within the accuracy of our technique.

Our obtained ΔE_v value for $x = 25\%$ lies below an extrapolation of our results for $x = 10$ and $x = 17\%$. This is most surely due to the fact that this sample is 25% relaxed, as mentioned above. A drop in ΔE_v with the loss of coherence is expected theoretically [10], [11] and has been reported experimentally [9], [18], [45].

We compare our experimental ΔE_v results for the top interface with those reported by other authors in the range of $0 < x < 25\%$ in Fig. 13. Only experimental data for fully coherent layers is included in this figure. We find that our data agree well with those of Brighten *et al.* [19], [20], Ni *et al.* [12], Wang *et al.* [15], and Iyer *et al.* [9]. The data set from Iyer *et al.* [9] was obtained on graded-base Si/SiGe HBT's and is indicated by the space enclosed by the broken lines in Fig. 13.

In King's experiments [13], ΔE_v is extracted from the comparison of HBT characteristics between two wafers with identical structures but different Ge compositions in the base. This is a rather indirect procedure which is error prone. Futhermore, the bases of the HBT's were degenerately doped with B. If bandgap narrowing in Si and $Si_{1-x}Ge_x$ is different for the same doping level, this difference will show up in the final ΔE_v value. Nauka *et al.* [18] performed their measurements by means of admittance spectroscopy. This technique is vulnerable to traps.

A fit to our data for the top interface of fully strained samples yields $\Delta E_v \simeq 6.4x$ meV. The agreement between our transport-type device extraction method and other techniques as different as C-V [19], [20], X-ray photoelectron spectroscopy [12], as well as indirect determinations from HBT's [9] and modulation-doped heterostructures [15], provides substantial confidence in the value of ΔE_v between strained SiGe and (100) Si for small Ge compositions. Our error bars, however, preclude us from making any meaningful statements about the magnitude of ΔE_c. This will require special-purpose heterostructures that rely on electron transport.

VI. Conclusion

We have carried out a transport-based device-type measurement of the valence band discontinuity of strained $Si_{1-x}Ge_x$ on (100) Si using SIS heterostructures grown by UHV/CVD for $10 < x < 25\%$. A new analytical procedure is demonstrated that allows the extraction of small ΔE_v values. Our experiments indicate that $\Delta E_v \simeq 6.4x$ meV for $0 < x < 17.5\%$. Our results also consistently indicate that for $x > 10\%$, the bottom $Si/Si_{1-x}Ge_x$ interface has a smaller ΔE_v than the top interface. This finding might arise from strain-induced interface roughness at the bottom interface that is smoothed out by the intermediate Si barrier layer.

Acknowledgment

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References

[1] T. P. Pearsall, "Silicon-Germanium alloys and heterostructures: Optical and electronic properties," *CRC Critical Reviews in Solid State and Materials Sciences*, vol. 15, p. 551, 1989.

[2] B. S. Meyerson, "UHV/CVD growth of Si and Si:Ge alloys: Chemistry, physics, and device applications," *Proc. IEEE*, vol. 80, p. 1592, 1992.

[3] S. S. Iyer, G. L. Patton, S. L. Delage, S. Tiwari, and J. M. C. Stork, "Silicon-Germanium heterojunction bipolar transistors by molecular beam epitaxy," *IEDM Tech. Dig.*, p. 874, 1987.

[4] T. I. Kamins, K. Nauka, J. B. Kruger, J. L. Hoyt, C. A. King, D. B. Noble, C. M. Gronet, and J. F. Gibbons, "Small-geometry, high performance, Si-$Si_{1-x}Ge_x$ heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 10, p. 503, 1989.

[5] G. L. Patton, J. H. Comfort, B. S. Meyerson, E. F. Crabbé, G. J. Scilla, E. D. Fresart, J. M. C. Stork, J. Y.-C. Sun, D. L. Harame, and J. N. Burghartz, "75 GHz f_T SiGe-base heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 11, p. 171, 1990.

[6] E. F. Crabbé, B. S. Meyerson, D. L. Harame, J. M. C. Stork, A. Megdanis, J. Cotte, J. Chu, M. Gilbert, C. Stanis, J. H. Comfort, G. L. Patton, and S. Subbanna, "113-GHz f_T graded-base SiGe HBTs," *51st Device Res. Conf.*, 1993. Abstract in *IEEE Trans. Electron Devices*, vol. 40, p. 2100, 1993.

[7] R. People, "Indirect band gap of coherently strained Ge_xSi_{1-x} bulk alloys on (001) silicon substrates," *Phys. Rev. B*, vol. 32, p. 1405, 1985.

[8] D. V. Lang, R. People, J. C. Bean, and A. M. Sergent, "Measurement of the bandgap of Ge_xSi_{1-x}/Si strained layer heterostructures," *Appl. Phys. Lett.*, vol. 47, p. 1333, 1985.

[9] S. Iyer, G. L. Patton, J. M. C. Stork, B. S. Meyerson, and D. L. Harame, "Heterojunction bipolar transistors using Si-Ge alloys," *IEEE Trans. Electron Devices*, vol. 36, p. 2043, 1989.

[10] R. People and J. C. Bean, "Band alignments of coherently strained Ge_xSi_{1-x}/Si heterostructures on $\langle 001 \rangle$ Ge_ySi_{1-y} substrates," *Appl. Phys. Lett.*, vol. 48, p. 538, 1986.

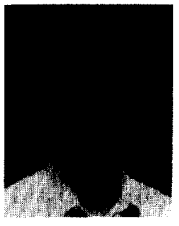
[11] C. G. Van de Walle and R. M. Martin, "Theoretical calculations of heterojunction discontinuities in the Si/Ge system," *Phys. Rev. B*, vol. 34, p. 5621, 1986.

[12] W.-X. Ni, J. Knall, and G. V. Hansoon, "New method to study band offsets applied to strained Si/$Si_{1-x}Ge_x$ (100) heterojunction interfaces," *Phys. Rev. B*, vol. 36, p. 7744, 1987.

[13] C. A. King, J. L. Hoyt, and J. F. Gibbons, "Bandgap and transport properties of $Si_{1-x}Ge_x$ by analysis of nearly ideal Si/$Si_{1-x}Ge_x$/Si heterojunction bipolar transistor," *IEEE Trans. Electron Devices*, vol. 36, p. 2093, 1989.

[14] R. C. Taft, J. D. Plummer, and S. S. Iyer, "Demonstration of a p-channel BICFET in the Ge_xSi_{1-x}/Si system," *IEEE Electron Device Lett.*, vol. 10, p. 14, 1989.

[15] P. J. Wang, F. F. Fang, B. S. Meyerson, J. Nocera, and B. Parker, "Two-dimensional hole gas in $Si/Si_{0.85}Ge_{0.15}/Si$ modulation-doped double heterostructures," *Appl. Phys. Lett.*, vol. 54, p. 2701, 1989.
[16] W.-X. Ni and G. V. Hansson, "Band offsets in pseudomorphically grown $Si/Si_{1-x}Ge_x$ heterostructures studied with core-level x-ray photoelectron spectroscopy," *Phys. Rev. B*, vol 42, p. 3030, 1990.
[17] S. Khorram, C. H. Chern, and K. L. Wang, "Measurement of valence band offset in strained Ge_xSi_{1-x}/Si heterojunctions," *Mat. Res. Soc. Symp. Proc.*, vol 220, p. 181, 1991.
[18] K. Nauka, T. I. Kamins, J. E. Turner, C. A. King, J. L. Hoyt, and J. F. Gibbons, "Admittance spectroscopy measurements of band offsets in $Si/Si_{1-x}Ge_x/Si$ heterostructures," *Appl. Phys. Lett.*, vol. 60, p. 195, 1992.
[19] J. C. Brighten, I. D. Hawkins, A. R. Peaker, E. H. C. Parker, and T. E. Whall, "The determination of valence band discontinuities in $Si/Si_{1-x}Ge_x/Si$ heterojunctions by capacitance-voltage techniques," *J. Appl. Phys.*, vol. 74, p. 1894, 1993.
[20] J. C. Brighten, I. D. Hawkins, A. R. Peaker, E. H. C. Parker, and T. E. Whall, "The determination of valence band discontinuities and interface charge densities in $Si/Si_{1-y}Ge_y/Si$ heterojunctions," *Semicond. Sci. Technol.*, vol. 8, p. 1487, 1993.
[21] L. Vescan, R. Apetz, and H. Lüth, "Determination of the valence band offset of $Si/Si_{0.7}Ge_{0.3}/Si$ quantum wells using deep level transient spectroscopy," *J. Appl. Phys.*, vol. 73, p. 7427, 1993.
[22] S. R. Forrest, "Measurement of energy band offsets using capacitance and current measurement techniques," *Heterojunction Band Discontinuities: Physics and Device Applications*, F. Capasso and G. Margaritondo, Eds. New York: Elsevier, 1987, p. 311.
[23] T. W. Hickmott, P. M. Solomon, R. Fischer, and H. Morkoç, "Negative charge, barrier heights, and the conduction-band discontinuity in $Al_xGa_{1-x}As$ capacitors," *J. Appl. Phys.*, vol. 57, p. 2844, 1985.
[24] J. Batey and S. L. Wright, "Energy band alignment in GaAs:(Al,Ga)As heterostructures: The dependence on alloy composition," *J. Appl. Phys.*, vol. 59, p. 200, 1986.
[25] D. Arnold, A. Ketterson, T. Henderson, J. Klem, and H. Morkoç, "Electrical characterization of GaAs/AlGaAs semiconductor-insulator-semiconductor capacitors and application to the measurement of the GaAs/AlGaAs band-gap discontinuity," *J. Appl. Phys.*, vol. 57, p. 2880, 1985.
[26] C. K. Peng, A. Ketterson, and H. Morkoç, "Determination of the conduction-band discontinuity between $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ using n^+-InGaAs/InAlAs/n^--InGaAs capacitors," *J. Appl. Phys.*, vol. 60, p. 1709, 1986.
[27] P. Collot, E. Barbier, P. E. Schmidt, C. Arnodo, C. Gaonach, and J. Favre, "Electrical characterization of $In_{0.53}Ga_{0.47}As/Al_{0.4}Ga_{0.6}As/GaAs$ pseudomorphic semiconductor/insulator/semiconductor heterostructures," *Appl. Phys. Lett.*, vol. 58, p. 367, 1991.
[28] J.-H. Huang, T. Y. Chang, and B. Lalevic, "Measurement of the conduction-band discontinuity in pseudomorphic $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ heterostructures," *Appl. Phys. Lett.*, vol. 60, p. 733, 1992.
[29] V. A. K. Temple and J. Shewchun, "The exact low-frequency capacitance-voltage characteristics of metal-oxide-semiconductor (MOS) and semiconductor-insulator-semiconductor (SIS) structures," *IEEE Trans. Electron Devices*, vol. 18, p. 235, 1971.
[30] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1981.
[31] S. S. Li, "The dopant density and temperature dependence of hole mobility and resistivity in boron doped silicon," *Solid-State Electron.*, vol. 21, p. 1109, 1978.
[32] B. S. Meyerson, "Low-temperature silicon epitaxy by ultrahigh vacuum/chemical vapor deposition," *Appl. Phys. Lett.*, vol. 48, p. 797, 1986.
[33] J. W. Matthews and A. E. Blakeslee, "Defects in epitaxial multilayers," *J. Crystal Growth*, vol. 27, p. 118, 1974.
[34] A. T. Fiory, J. C. Bean, L. C. Feldman, and I. K. Robinson, "Commensurate and incommensurate structures in molecular beam epitaxially grown Ge_xSi_{1-x} films on Si(100)," *J. Appl. Phys.*, vol. 56, p. 1227, 1984.
[35] R. People and J. C. Bean, "Calculations of critical layer thickness vs. lattice mismatch for Ge_xSi_{1-x}/Si strained-layer heterostructures," *Appl. Phys. Lett.*, vol. 47, p. 322, 1985.
[36] Y. Kohama, Y. Watanabe, and Y. Fukuda, "Electron-beam-induced current observation of misfit dislocations at $Si_{1-x}Ge_x/Si$ interfaces," *Japn. J. Appl. Phys.*, vol. 26, p. L1944, 1987.
[37] Y. Kohama, Y. Fukuda, and M. Seki, "Determination of the critical layer thickness of $Si_{1-x}Ge_x/Si$ heterostructures by direct observation of misfit dislocations," *Appl. Phys. Lett.*, vol. 52, p. 380, 1988.
[38] D. J. Eaglesham, E. P. Kvam, D. M. Maher, C. J. Humphreys, G. S. Green, B. K. Tanner, and J. C. Bean, "X-ray topography of the coherency breakdown in $Ge_xSi_{1-x}/Si(100)$," *Appl. Phys. Lett.*, vol. 53, p. 2083, 1988.
[39] R. Hull and J. C. Bean, "Variation in misfit dislocation behavior as a function of strain in the GeSi/Si system," *Appl. Phys. Lett.*, vol. 54, p. 925, 1989.
[40] J.-M. Baribeau, S. Kechang, and K. Munro, "X-ray diffraction of strain relaxation in $Si\text{-}Si_{1-x}Ge_x$ heterostructures," *Appl. Phys. Lett.*, vol. 54, p. 323, 1989.
[41] S. R. Stiffler, J. H. Comfort, C. L. Stanis, D. L. Harame, E. de Frésart, and B. S. Meyerson, "The thermal stability of SiGe films deposited by ultrahigh-vacuum chemical vapor deposition," *J. Appl. Phys.*, vol. 70, p. 1416, 1991.
[42] C. Gan, "Direct measurement of $Si_{1-x}Ge_x/Si$ valence band discontinuity using a semiconductor-insulator-semiconductor (SIS) structure," MIT, S.M. thesis, 1992.
[43] J. P. Dismukes, L. Ekstrom, and R. J. Paff, "Lattice parameter and density in Germanium-silicon alloys," *J. Phys. Chem.*, vol. 68, p. 3021, 1964.
[44] K. Goto, J. Murota, T. Maeda, R. Schütz, K. Aizawa, R. Kircher, K. Yokoo, and S. Ono, "Fabrication of a $Si_{1-x}Ge_x$ channel metal-oxide-semiconductor field-effect transistor (MOSFET) containing high Ge fraction layer by low-pressure chemical vapor deposition," *Jpn. J. Appl. Phys.*, vol. 32, p. 438, 1993.
[45] J. C. Sturm, E. J. Prinz, P. M. Garone, and P. V. Schwartz, "Band-gap shifts in silicon-Germanium heterojunction bipolar transistors," *Appl. Phys. Lett.*, vol. 54, p. 2707, 1989.



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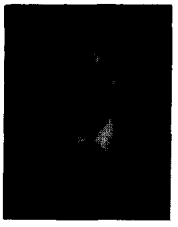

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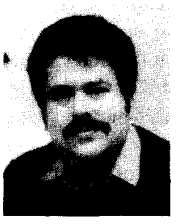

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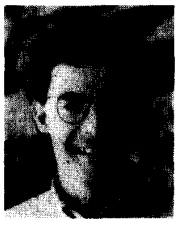
He then joined the IBM Thomas J. Watson Research Center as a Research Staff Member. His early work was in the field of amorphous semiconductors, primarily hydrogenated amorphous carbon films, investigating their electronic properties as related to local atomic ordering. His more recent work has focused on low temperature epitaxy, demonstrating unique materials and devices in a number of metastable material systems. He invented the ultrahigh vacuum/chemical vapor deposition (UHV/CVD) technique. He presently manages the Electronic Materials Group within the Physical Sciences and Technology Department at the IBM T. J. Watson Research Center.

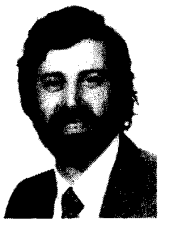
Dr. Meyerson received the Young Authors Award from the American Association of Crystal Growth in 1987 for developing the UHV/CVD technique. He won the 1991 MRS Medal for his work in silicon-Germanium materials, leading to the fabrication of record fast HBT's. In 1992 he was named an IBM Fellow. In 1993 he received the Electronics Division Award of the Electrochemical Society for fabricating novel silicon-Germanium alloy structures and devices.



Emmanuel F. Crabbé (S'81–M'88) was born in Mexico City in 1959. After two years at the Université Katholique de Louvain in Belgium, he completed the B.S. degree in electrical engineering from the University of Missouri at Columbia. He received the M.S. and Ph.D. degrees in electrical engineering from Stanford University in 1983 and 1988, respectively.

He joined IBM T. J. Watson Research Center in 1988 to work on SiGe bipolar transistors and FET's. Since 1992 he has been working on high-performance CMOS logic in the IBM Semiconductor Research and Development Center.

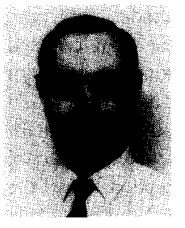
Dr. Crabbé served on the program committee of the European Solid State Device Research Conference in 1992, and has since been a member of its Technical Program Committee.



Charles G. Sodini (S'80–M'82–SM'90) was born in Pittsburgh, PA, in 1952. He received the B.S.E.E. degree from Purdue University, Lafayette, IN, in 1974, and the M.S.E.E. and Ph.D. degrees from the University of California at Berkeley in 1981 and 1982, respectively.

He was a member of the Technical Staff at Hewlett-Packard Laboratories from 1974 to 1982, where he worked on the design of MOS memory and MOS devices with very thin gate dielectrics. He joined MIT, Cambridge, MA, in 1983, where he is currently a Professor in the Department of Electrical Engineering and Computer Science. His research interests are focused on IC fabrication, device modeling, and device level circuit design, with emphasis on analog and memory circuits.

Dr. Sodini held the Analog Devices Career Development Professorship in MIT's Department of Electrical Engineering and Computer Science, and was awarded the IBM Faculty Development Award from 1985 to 1987. He was the 1989 General Chairman of the International Electron Device Meeting. He was the Technical Program Co-Chairman for the 1992 Symposium on VLSI Circuits and is currently the 1993–1994 Co-Chairman of the Symposium.



L. Rafael Reif (M'79–SM'90–F'93) was born in Maracaibo, Venezuela, on August 21, 1950. he received the Ingeniero Electrico degree in 1973 from the Universidad de Carabobo, Valencia, Venezuela, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1975 and 1979, respectively.

During 1973–1974 he was an Assistant Professor at the Universidad Simón Bolivar, Caracas, Venezuela. In 1978 he became a Visiting Assistant Professor in the Department of Electrical Engineering, Stanford University. In 1980 he joined MIT, where he is a Professor in the Department of Electrical Engineering and Computer Science. He is presently working on the low-temperature CVD of epitaxial and polycrystalline silicon and Si-Ge alloys, and on novel fabrication technologies for high-speed bipolar transistors and thin-film transistors.

Dr. Reif held the Analog Devices Career Development Professorship of MIT's Department of Electrical Engineering and Computer Science, and was awarded the IBM Faculty Fellowship of MIT's Center for Materials Science and Engineering from 1980 to 1982. He also received a Presidential Young Investigator Award in 1984. He is a member of Tau Beta Pi, the Electrochemical Society, and the American Physical Society.