Velocity Saturation in the Extrinsic Device: A Fundamental Limit in HFET's

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***Abstract*—We have carried out an experimental study revealing that velocity saturation ($v_{\rm sat}$) occurring in both the extrinsic source and drain sets a fundamental limit on maximum drain current and useful gate swing in HFET's. Using AlGaAs/ n^+-InGaAs HFET's as a vehicle, we find that first g_m and eventually f_T decline at high currents in two stages. Initially, the approach of $v_{\rm sat}$ in the extrinsic device causes the *small-signal* source and drain resistances (r_s and r_d) to rise dramatically, primarily degrading g_m. As the current increases further, the *large-signal* source and drain resistances (R_s and R_d) grow significantly as well, pushing the intrinsic HFET toward the linear regime. Combined with the rapid rise of r_s and r_d, the accompanying increase in gate-drain capacitance forces f_T to decline through a strongly enhanced Miller effect. We associate this two-fold mechanism with a new regime of HFET operation, which we call the *parasitic-resistance blow-up* regime.**

I. Introduction

THE heterostructure field-effect transistor (HFET) is playing an increasingly important role in a number of high-power, high-frequency telecommunications applications demanding devices capable of achieving high values for figures of merit such as transconductance (g_m) and f_T maintained over a broad gate-voltage (V_{GS}) swing. In order to properly design circuits to fit these applications, circuit designers must have access to accurate HFET models that are valid over the device's full range of possible operating biases. To this end, there has been a great deal of work to date focusing on understanding and modeling the intrinsic device, including the effects of both mobility-limited and velocity-saturation-limited electron transport. In contrast, the role of the extrinsic device in the region between the gate and ohmic contacts has received little attention and has been generally modeled with only simple resistances attached to a core intrinsic model. Yet the extrinsic device plays a key role in determining the behavior of a real HFET and in setting ultimate performance limits.

The extrinsic region is well known to contribute to the parasitic source and drain resistances which degrade figures of merit such as transconductance (g_m), f_T, and $f_{\rm max}$ [1], [2]. The parasitic resistances also impact the large-signal capabilities of the device by increasing the knee voltage ($V_{DS}^{\rm sat}$) [3]. These facts have motivated the development of a variety of self-aligned gate fabrication schemes to try to reduce source and drain resistance in FET's [4].

Electron velocity saturation ($v_{\rm sat}$) occurring in the *intrinsic* device has been recognized to impact device operation [5]. To date, however, there has been no recognition that $v_{\rm sat}$ can also occur at high currents in the *extrinsic* regions of an HFET. When this happens, the source and drain resistances can rise dramatically, causing figures of merit such as g_m and f_T to decline. Although this mechanism may be masked in many HFET designs by other performance-degrading effects which dominate first, such as gate leakage current [6], parasitic MESFET formation [7], or electron real-space transfer [6], it can be of importance in HFET's with large insulator bandgaps and optimized design. The onset of $v_{\rm sat}$ in the extrinsic device will ultimately limit the useful gate-swing and current capabilities of HFET's, particularly in devices optimized for power and employing a sizeable gate-drain gap (regardless of gate-source configuration) in order to achieve high breakdown voltage.

In this study, we investigate the impact of the extrinsic device on HFET performance using a pseudomorphic AlGaAs/n^+-InGaAs HFET as a vehicle [8]. Because of its undoped pseudoinsulator layer and strained channel, this design is immune to the parasitic MESFET formation of the MODFET [7] and displays reduced gate leakage and real-space transfer [8]. In addition, the device is not self aligned, making the role of the extrinsic regions easier to observed.

II. Theory

The fundamental limits on device performance set by the impact of the extrinsic source and drain can be understood in terms of the simplified small-signal equivalent circuit shown in Fig. 1. We focus for the moment on the small-signal source and drain resistance elements r_s and r_d, which we take to represent the extrinsic source and drain (ohmic contact resistance is neglected for simplicity in this section). Typically, the extrinsic source and drain are modeled as simple linear resistances with values obtained from low-current measurements. In such a model, r_s and r_d are taken to remain equal to their low-current values R_{s0} and R_{d0}, respectively, regardless of current. This basic model leads to the well known degradation of g_m through source and drain degeneration [10].

A simple linear resistance is not an adequate model for the extrinsic regions in a real HFET, however. A more accurate model is that of a region with fixed sheet charge density, $Q_{\rm ext}$, and with a carrier velocity versus electric field relation,

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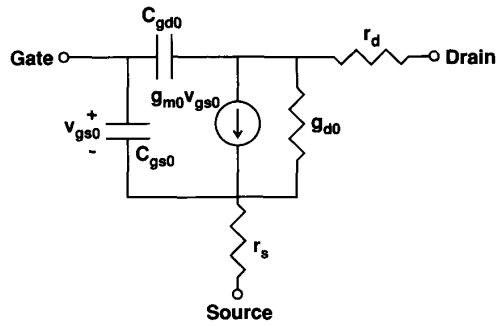

Fig. 1. Simplified HFET small-signal equivalent circuit model used in device analysis.

$v_e(\mathcal{E})$, that includes velocity-saturation. One possible I–V characteristic for, say, the extrinsic source that captures the key features of such an improved model is given as follows:

$$I_D = WQ_{\text{ext}} v_e\left(\frac{V_s}{L_{sg}}\right) \tag{1}$$

with

$$v_e(\mathcal{E}) = \frac{v_{\text{sat}}\mathcal{E}}{[\mathcal{E}_{\text{crit}}^{\gamma} + \mathcal{E}^{\gamma}]^{1/\gamma}} \tag{2}$$

and

$$v_{\text{sat}} = \mu_e \mathcal{E}_{\text{crit}}. \tag{3}$$

Here, V_s is the voltage dropped across the extrinsic source, W is the device width, L_{sg} is the gate-source extrinsic gap, Q_{ext} is the sheet charge density in the extrinsic source, μ_e is the carrier mobility in the extrinsic region, and γ is a fitting parameter determining how sharply v_e approaches saturation velocity v_{sat} as the electric field moves past the critical field $\mathcal{E}_{\text{crit}}$. Combining (1)–(3) into a single expression for the I–V characteristic of the intrinsic source yields:

$$I_D = \frac{1}{R_{s0}} \cdot \frac{V_s}{\left[1 + \left(\frac{V_s}{V_{\text{crit}}}\right)^{\gamma}\right]^{1/\gamma}} \tag{4}$$

where

$$R_{s0} = \frac{L_{sg}}{WQ_{\text{ext}}\mu_e} \tag{5}$$

is the low-current source resistance and

$$V_{\text{crit}} = \mathcal{E}_{\text{crit}} L_{sg} \tag{6}$$

is the critical voltage separating the low- and high-field behaviors. We demonstrate below that this expression fits quite closely experimental I–V curves of transmission line model (TLM) test structures.

Using this model, the large- and small-signal source resistances are a function of drain current I_D described, respectively, by

$$R_s = \frac{V_s}{I_D} = \frac{R_{s0}}{\left[1 - \left(\frac{I_D}{I_{D,\text{sat}}}\right)^{\gamma}\right]^{1/\gamma}} \tag{7}$$

and

$$r_s = \frac{dV_s}{dI_D} = \frac{R_{s0}}{\left[1 - \left(\frac{I_D}{I_{D,\text{sat}}}\right)^{\gamma}\right]^{1+(1/\gamma)}} = \frac{R_s^{\gamma+1}}{R_{s0}^{\gamma}} \tag{8}$$

where

$$I_{D,\text{sat}} = \frac{V_{\text{crit}}}{R_{s0}} = WQ_{\text{ext}} v_{\text{sat}} \tag{9}$$

is the maximum current supported by the extrinsic source. Similar expressions apply to the extrinsic drain.

Thus while at low I_D the extrinsic device regions are well modeled by linear resistors of values R_{s0} and R_{d0}, we note that as I_D approaches the limiting value of $I_{D,\text{sat}}$, r_s, r_d, R_s, and R_d all diverge regardless of the initial low-current resistance values. This *parasitic-resistance blow-up* regime is responsible for degrading g_m and f_T at high currents.

We first consider g_m which, referring to the circuit in Fig. 1, may be expressed as

$$g_m = \frac{g_{m0}}{1 + r_s g_{m0} + (r_s + r_d) g_{d0}} \tag{10}$$

where r_s and r_d are the small-signal parasitic resistances associated with the source and drain, respectively [10]. From (7) and (8), we note that r_s and r_d rise much more rapidly with I_D than do R_s and R_d. This first stage consequently brings down g_m. Because g_{d0} is typically much smaller than g_{m0} in an HFET biased in saturation, the blowup of r_s has far more impact on g_m than that of r_d. Referring once again to Fig. 1, we may also consider the behavior of f_T [2] (see bottom of page). For the simple linear resistor parasitic source and drain model, and for a typical device in which $C_{gd0} \ll C_{gs0}$ and $g_{d0}(R_{s0} + R_{d0}) \ll 1$, this expression reduces to

$$f_T \simeq f_{T0} = \frac{g_{m0}}{2\pi C_{gs0}}. \tag{12}$$

Thus this simple model predicts that f_T is hardly impacted by parasitic resistance at all.

If we include r_s and r_d blowup, however, we find that both terms in the denominator of (11) rise at high I_D and contribute to bringing f_T down. This decline of f_T is dominated in a typical HFET by the second term involving C_{gd0} because it is multiplied by a term containing g_{m0}. Thus f_T degrades due to the Miller effect.

Comparing the dominating terms in the expressions for f_T and g_m, we note while g_m suffers significant impact from r_s as $g_{m0}r_s \sim 1$, f_T is not seriously degraded by the extrinsic device

$$f_T = \frac{g_{m0}}{2\pi\{C_{gs0}[1 + g_{d0}(r_s + r_d)] + C_{gd0}[1 + (g_{m0} + g_{d0})(r_s + r_d)]\}} \tag{11}$$

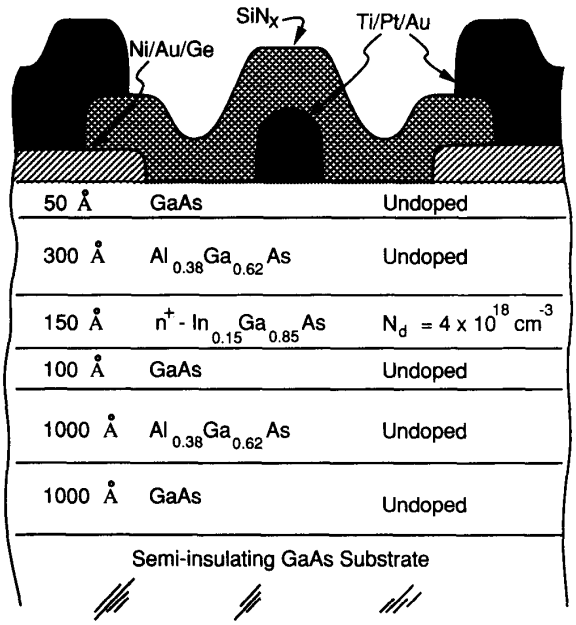

Fig. 2. Schematic cross section of the AlGaAs/n$^+$-InGaAs HFET.

until $1 + g_{m0}(r_s + r_d) \sim C_{gs0}/C_{gd0}$. Since $C_{gs0} \gg C_{gd0}$ in a well designed HFET, r_s and r_d generally must rise to much higher values to initiate the decline of f_T compared with g_m. Thus based on this argument alone, we expect f_T to fall off at higher I_D than g_m. However, we have not yet accounted for a possible increase in C_{gd0} at high I_D.

Indeed, at sufficiently high I_D, the large-signal resistances, R_s and R_d, and thus the extrinsic ohmic drop, begin to blow up as well and to push the intrinsic device rapidly toward the onset of the linear regime regardless of the applied drain-source bias. The channel becomes less and less isolated from the drain ohmic contact, causing both C_{gd0} and g_{d0} to increase significantly. Because the decline of g_m is dominated by the rapid rise in $g_{m0}r_s$, this second stage has only a modest impact on the decline of g_m. However, combined with the blowup of r_s and r_d, the rapid rise in C_{gd0} results in a dramatic enhancement of the Miller effect term in (11), significantly accelerating the fall-off of f_T.

The next section describes an experimental observation of parasitic resistance blowup in AlGaAs/n$^+$-InGaAs HFET's.

III. Experimental Results and Discussion

As a vehicle for this experiment, we have studied pseudomorphic AlGaAs/n$^+$-InGaAs HFET's with $L_g = 1.7\,\mu$m and $W_g = 200\,\mu$m. Our MBE-grown heterostructure (shown in Fig. 2) and details of device fabrication are described in (8).

Fig. 3 shows the behavior of g_m (measured at DC) and f_T versus I_D for a typical microwave device biased at $V_{DS} = 5$ V. This drain-source bias is large enough to place the device in the saturation mode of operation in which I_D is largely insensitive to V_{DS}. We note a distinct three-regime behavior as a function of I_D, with both g_m and f_T initially rising for

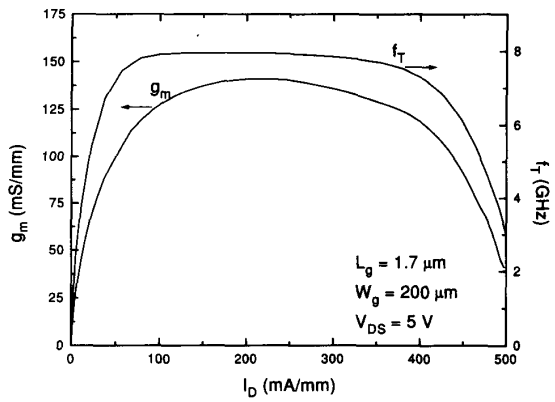

Fig. 3. g_m andf_T versus I_D for a typical $L_g = 1.7\,\mu$m device.

low I_D, just above threshold, flattening into broad plateaus for larger I_D, and finally declining at high I_D. The first two regimes have been explored in detail elsewhere [9], establishing mobility-limited transport ($\mu_e \simeq 1750\,\mathrm{cm^2/Vs}$) in the regime of g_m and f_T rise and velocity-saturation-limited transport ($v_{\mathrm{sat}} \simeq 8.8 \times 10^6\,\mathrm{cm/s}$) in the plateau regime. In looking at the high-I_D regime, our previous scaling study [9] demonstrated that the performance decline was not due to the onset of gate leakage, or the formation of a parallel MESFET (which is not possible in our undoped-device design). To assess the possibility that real-space transfer is limiting our devices, we have also looked for a characteristic dip in I_D and rise in I_G at high V_{GS} as V_{DS} is raised into the device's saturation mode of operation [11]. This signature, clearly seen in other device designs [6], is absent from our devices, thus indicating no significant real-space transfer. In our present study, we focus in detail on establishing the mechanism behind this high-bias regime which ultimately limits the maximum I_D and gate-swing the device can achieve.

In Fig. 4, we examine low-frequency g_m versus I_D for V_{DS} stepped from 0.5 V to 6 V. We note that for $V_{DS} < 5$ V, an increase in V_{DS} delays the decline of g_m out to higher I_D. This indicates that the decline of g_m at low V_{DS} is due to the device entering the linear regime, preventable by increasing V_{DS} and predicted by a simple linear resistor model for the extrinsic device. However, we find that the three curves for V_{DS} equal to 5 V, 5.5 V, and 6 V lie virtually on top of one another even though g_m is falling off. Small increases in V_{DS} do not delay this fall off, indicating that the decline of g_m at high I_D and V_{DS} is actually due to some other phenomenon.

Examining the high-I_D region of decline more closely to Fig. 3, we also note that while g_m and f_T both share a similar three-regime behavior, g_m begins to decline first and falls to 90% of peak by about 360 mA/mm. On the other hand, f_T maintains a broader plateau, remaining above 90% of peak out to about 410 mA/mm. These features, general to all our devices at high I_D, suggest that the degrading mechanism impacts g_m and f_T through two different avenues. We now consider this behavior in detail.

Comparing the behavior of the falloff of g_m and f_T in our devices with the parasitic resistance blowup theory presented

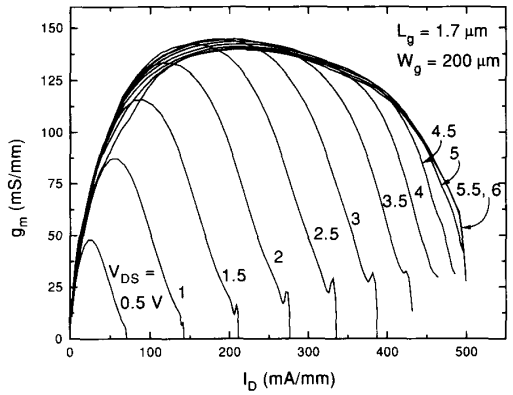

Fig. 4. g_m versus I_D for a typical $L_g = 1.7\,\mu$m device for varying V_{DS}.

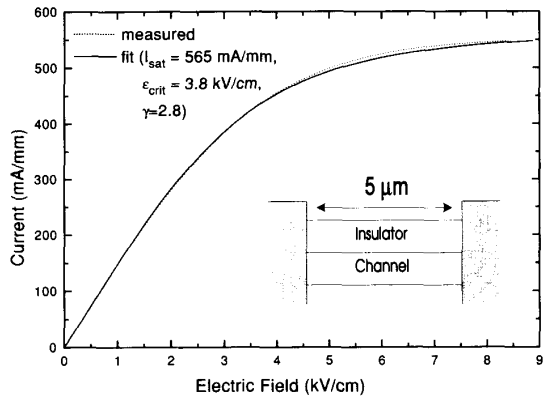

Fig. 5. Current versus electric field (measured and fit) for a 5 μm TLM test structure.

earlier requires that we first establish a method of determining r_s and r_d accurately as a function of bias. At this point, we must also take ohmic contact resistance into account.

Because the ungated extrinsic regions of our non-self-aligned device structure are very similar to that of a TLM test structure [13], we expect the I–V curve of a neighboring TLM to serve as a good model for that of extrinsic device. Specifically, (1)–(3) apply to the TLM as well, but with V_s replaced by V_{TLM} (representing the potential across the TLM after contact resistance correction) and the gate-source gap L_{sg} replaced by the TLM gap $L_{\rm gap} = 5\,\mu$m. In Fig. 5, we plot the measured current versus electric field $(V_{TLM}/L_{\rm gap})$ together with a modeled curve obtained by fitting the measured data to (1)–(3). The contact resistance correction is $2 \cdot R_c = 2 \cdot 0.6\,\Omega$-mm, as measured on identical TLM structures of varying gap length [8].

Fig. 5 shows that while current rises linearly with electric field for currents below approximately 300 mA/mm, it eventually saturates to a value of about 550 mA/mm. We note that (1)–(3) yield an excellent fit to our measured data, with the parameters $I_{D,\rm sat} = 565$ mA/mm, $\mathcal{E}_{\rm crit} = 3.8$ kV/cm, and $\gamma = 2.8$.

We can use this experimental curve to deduce the large- and small-signal source and drain resistance of a typical HFET

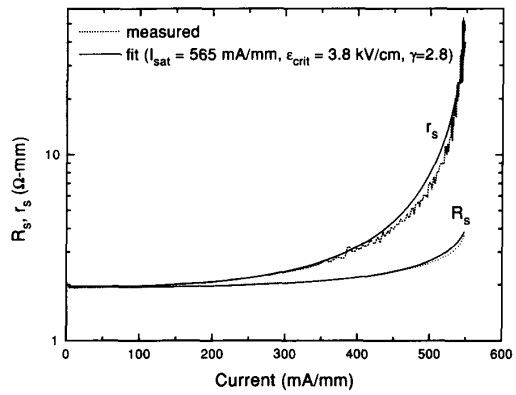

Fig. 6. Large- and small-signal source resistance versus current for a 2 μm source-gate gap (deduced from data of Fig. 5 as discussed in text).

with gate-source gap L_{sg} and gate-drain gap L_{dg} using the following relations:

$$R_s = R_c + L_{sg}\frac{\mathcal{E}}{I} \tag{13}$$

$$R_d = R_c + L_{dg}\frac{\mathcal{E}}{I} \tag{14}$$

$$r_s = R_c + L_{sg}\frac{d\mathcal{E}}{dI} \tag{15}$$

$$r_d = R_c + L_{dg}\frac{d\mathcal{E}}{dI}. \tag{16}$$

Fig. 6 shows, as an example, both R_s and r_s versus I expected in a typical HFET L_{sg} of 2 μm, together with modeled curves obtained by applying (13)–(16) to the model in Fig. 5. In our devices, $L_{dg} = 2\,\mu$m as well. We note that the behavior of the extrinsic source is well modeled by a constant, linear resistance at low currents. At larger currents, however, first r_s (at about 300 mA/mm) and then R_s (at about 425 mA/mm) increase dramatically. We observe that these two points correlate well with the fall-off of g_m and f_T, respectively, as shown in Fig. 3.

Our model, described by (1)–(3) and (13)–(16), permits us to interpolate smoothly between measured data points, providing values for r_s and r_d at any given value of I_D. Using these values, we may then deduce the remaining Fig. 1 circuit elements g_{m0}, g_{d0}, C_{gs0}, and C_{gd0} directly from the y-parameters of the device (calculated from the s-parameters measured at 1.1 GHz [12]). We plot g_{m0}, g_{d0}, C_{gs0}, and C_{gd0} versus I_D in Fig. 7, together with measured g_m and g_d. We point out that the 1.1 GHz g_m data shown here is equal within 5% to the low frequency data presented in Fig. 3 due to the very low frequency dispersion of our HFET design [8]. Since g_m is a sensitive function of r_s, this low dispersion applies to our resistance data as well and thus justifies our use of low frequency TLM data to extract a model for extrinsic resistance in our devices.

Considering g_m first, we observe that while measured g_m falls off at high I_D as previously noted, the extracted intrinsic transconductance g_{m0} remains flat our to $I_D = 475$ mA/mm, the maximum current was measured. This directly indicates that the falloff of g_m at high I_D is due solely to r_s and r_d blowup, according to (10), rather than to any actual

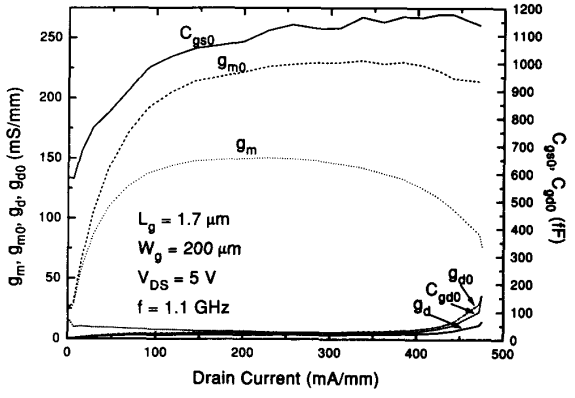

Fig. 7. $g_m, g_{m0}, g_d, g_{d0}, C_{gs0}$, and C_{gd0} versus drain current at 1.1 GHz for a typical $L_g = 1.7\,\mu$m, $W_g = 200\,\mu$m device.

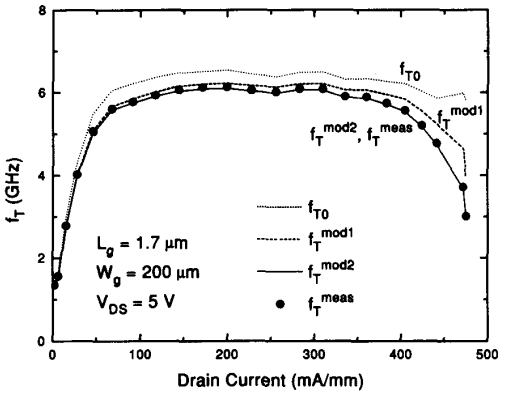

Fig. 8. Three calculated models of f_T compared with measured f_T versus drain current for a typical $L_g = 1.7\,\mu$m, $W_g = 200\,\mu$m device. f_T^{meas} (filled circles) is measured data, f_{T0} is modeled through (12), f_T^{mod1} is modeled through (17), and f_T^{mod2} is modeled through (11).

degradation of the intrinsic device. As a check of consistency, we examine the I_D behavior of the remaining equivalent circuit element values, such as C_{gs0}, extracted using the very same resistance values. We note that the curve of C_{gs0} behaves just as expected for an HFET operating in saturation, rising slowly once the device is biased beyond threshold and asymptotically approaching the geometric capacitance (calculated as $\sim 1100fF$ for this device). This behavior agrees with direct C–V measurements taken on test diodes to within 7%, after normalizing the area.

Before considering the decline of f_T, we first note that, for I_D beyond about 400 mA/mm, both g_{d0} and C_{gd0} begin to rise significantly. This rise marks the point at which the ohmic drop across the velocity-saturated extrinsic device has increased sufficiently to force the intrinsic device close to the onset of the linear regime. As the device nears the linear regime, isolation between the channel and drain contact starts to disappear. The onset of this phenomenon is the second mechanism through which the parasitic-resistance blowup regime degrades the device, particularly f_T.

Considering (11), we find that the rise in C_{gd0} has a significant impact on f_T and, combined with the blowup of r_s and r_d, is the mechanism responsible for its decline at high I_D. In order to explore this mechanism, we plot four quantities versus I_D in Fig. 8. The first quantity, f_T^{meas} is the actual measured data and is shown as filled circles. On the same plot, we also show the quantity f_{T0}, the value of f_T calculated from the simplified expression in (12). This is the value we would expect to observe in the absence of parasitics r_s, r_d, and C_{gd0}. We note that in the absence of these degrading elements, f_T remains flat out to high I_D. Next, we plot the quantity f_T^{mod1}. Here, we introduce to (12) the impact of rising C_{gd0} compounded by the Miller effect:

$$f_T^{\text{mod1}} = \frac{g_{m0}}{2\pi\{C_{gs0} + C_{gd0}[1 + g_{m0}(r_s + r_d)]\}}. \qquad (17)$$

We find that, with this new term in place, f_T^{mod1} does indeed decline at high I_D and agrees well with f_T^{meas}. This agreement demonstrates that f_T^{mod1} captures the dominating terms that are most responsible for bringing down f_T^{meas}. However, compared with the full expression for f_T given in (11), (17) ignores the impact of g_{d0} and thus results in a small discrepancy when compared to f_T^{meas}. This discrepancy is removed entirely by using our full (11) model for f_T, plotted as f_T^{mod2}.

Thus by using only source and drain resistance values deduced from independent, DC measurements on TLM test structures, we are able to obtain excellent agreement between modeled and measured values of g_m and f_T. We find that, while measured g_m and f_T decline at high current, g_{m0}, and f_{T0} remain flat. This confirms that the high-current degradation of our HFET's is not due to any intrinsic degradation, but rather to the impact of parasitic resistance blowup as summarized in (10) and (11).

As devices are scaled down and optimized, we expect parasitic resistance blowup to have increasing impact for several reasons. First, there is a growing trend for devices optimized particularly for power to employ both an undoped or surface depleted cap layer as well as a sizeable gate-drain gap in order to achieve an acceptable breakdown voltage [16], [17]. The sheet charge density in the extrinsic drain of such devices is relatively low compared with doped-cap or self-aligned implanted devices, making extrinsic drain resistance blowup a potentially significant issue. In addition, submicron devices are beginning to enter a regime in which velocity overshoot can occur in the channel, particularly in undoped channel devices. This overshoot does not occur in the extrinsic device due to the much lower electric fields, turning the extrinsic device into a performance bottleneck. Examining (11) and the subsequent discussion, we also note that the drain current at which f_T begins to fall off is influenced by the ratio of the gate-source to the gate-drain capacitance. Since this ratio decreases in proportion to decreasing gate length, we expect the fall-off of f_T to occur at lower I_D in smaller gate length devices. Finally, gate leakage current at given device bias has been seen to decrease with scaled down gate length [8]. In devices limited by the onset of significant gate leakage at larger gate lengths, the reduction in I_G with scaled down gate length may eventually unmask the influence of the extrinsic device and

shift the performance bottleneck to the blowup of the parasitic resistance.

IV. Conclusion

In this study, we have demonstrated velocity-saturation in the extrinsic device as the factor ultimately limiting I_D and gate swing in HFET's and causing figures of merit such as g_m and f_T to degrade at high I_D. Using AlGaAs/n$^+$-InGaAs HFET's as a vehicle, we have found that the approach of $v_{\rm sat}$ in the extrinsic source first causes the small-signal parasitic resistances to rise rapidly, forcing g_m to decline. At larger I_D, the large-signal source and drain resistances blowup as well, forcing the intrinsic device toward the linear regime and resulting in a rise in both g_{d0} and C_{gd0}. Combined with rising r_s and r_d, the rise in C_{gd0} causes a large Miller effect which brings down f_T still further. The limiting role of extrinsic device through these two mechanisms will become increasingly important as devices undergo submicron scaling and optimization through suppression of other limiting mechanisms such as gate leakage.

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