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AN INVESTIGATION OF DEEP LEVELS IN InAlAs/n$^+$-InGaAs HETEROSTRUCTURE FET's

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Abstract

A deep level investigation has been performed on InAlAs/n$^+$ - InGaAs metal-insulator doped-channel FET's. Two deep levels located in the InAlAs buffer have been measured :(i) a hole-like trap, reported for the first time and (ii) an electron trap linked to the kink effect.

Introduction

The InAlAs/InGaAs heterostructure FET (HFET) on InP is a basic device for the realization of electronic and optoelectronic integrated circuits (ICs). Because of its undoped insulator and thin, heavily-doped channel, the InAlAs/n+-InGaAs Metal-Insulator Doped-channel FET (MIDFET) has great potential for power handling (1). This device can be used for power microwave and laser driver IC's. However, we know from the GaAs experience that IC's designed for large signal applications suffer from trap-related parasitic effects such as current transients, sidegating, frequency-dependent characteristics, kink effect,... (2). These traps are mainly located in the semi-insulating substrate and buffer layers. They also play a detrimental role in InP-based HFET's (3), but few studies have been carried out on trap signatures. In this paper, we present deep level characterization performed on InP MIDFETs.

Device structure and performances

The studied device is a doubly-strained MBE-grown $In_{0.41}Al_{0.59}As/n^+$ - $In_{0.65}Ga_{0.35}As$ HFET, as illustrated in Fig. 1. A detailed description of the fabrication steps, and DC and RF performances has been previously published (1). Breakdown voltages greater than 12 V, and

Cap layer	: $In_{0.53}Ga_{0.47}As$;	50Å
Insulator	: $In_{0.41}Al_{0.59}As$;	300Å
Channel	: n^+ $In_{0.65}Ga_{0.35}As$ $N_D = 6\times10^{18} cm^{-3}$;	100Å
Sub-channel	: $In_{0.53}Ga_{0.47}As$;	75Å
Buffer layer	: $In_{0.52}Al_{0.48}As$;	1000Å
Semi Insulating InP		

Fig. 1 : Cross section showing the MBE-grown epitaxial layers design of the studied devices

drain current of 300 mA/mm of gate-width have been achieved together with f_t 15 GHz and f_{max} of 85-101 GHz for a gate-length, Lg, of 1.8 µm ; these devices demonstrate microwave large-signal capabilities. Our investigations have been conducted on HFET's with gate-widths, Wg of 30 µm and Lg's of 1.8 µm, 2.3 µm and 2.8 µm.

Existence of trapping mechanisms

The output I-V characteristics of the devices were found to be light sensitive, as shown in Fig. 2. This suggests the existence of deep-level electron trapping mechanisms and it is confirmed by the presence of kinks on the characteristics under illumination (4). However, the kink effect is weak : the corresponding peak amplitude on the output conductance, g_d, is not greater than 12 mS/mm. The kink effect is the most common trap-related parasitic effect. It has been widely studied and is now currently used as an indicator for the presence of traps in FET's and HEMT's. It has already been observed in InP MIDFET structures and explained by hot-electron transferred into and trapped by the InAlAs insulator and buffer layers. The trapping effect and its conduction mechanisms, however, were not established (5).

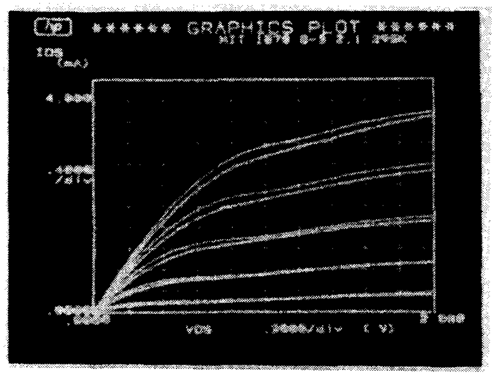

Fig. 2 : I-V characteristics measured at 295 K.
Upper curves : under illumination
Lower curves : in the dark

Traps measurement technique

The isothermal relaxation technique is used to identify deep level signatures in FET's. A description can be found elsewhere (6). This technique is based on the analysis of trap-related drain current transients obtained under gate-switching conditions with the drain-voltage, V_{DS}, fixed in the saturation region. This technique is therefore able to study the device under bias conditions well representative of actual operation. The devices have been biased at $V_{DS} = 2.6$ V and the gate voltage switched from $V_{GS} = 0$ V ($I_{DS} = I_{DSS}$) to a near pinch-off voltage, V_{GS} (off). V_{GS} (off) was chosen to be the voltage which maximized the drain current transient amplitude. This value of V_{GS} (off) corresponds to I_{DS} (static) I_{DSS} /10 at 295 K. It was ratio which was then held constant during the temperature scan from 150 K to 350 K.

Trap signatures

Typical Arrhenius plots of the thermal emission and capture time constants are reported in Fig. 3. An electron emission process is identified at low temperatures, while an electron capture process is identified at high temperatures. The thermal activation energy (Ena) and capture cross section (σna) of the electron trapping center are respectively 0.51 - 0.52 eV and 5 x10^{-14} cm^2 . A maximum N_T of 2 x 10^{15} cm^{-3} was measured for Lg = 1.8 µm. N_T is the concentration of traps modulated by the transient. N_T showed gate-length dependence, dropping to 3 x 10^{14} cm^{-3} for Lg = 2.3 µm. This could be due to lower trap-filling for longer gate-length devices. Moreover, we observed that N_T is linked to the kink amplitude and there is no significant peak on g_d when N_T<3 x $10^{14}$$cm^{-3}$ (Lg = 2.8 µm). For the hole-like trapping center, Epa, σpa, and the maximum measured values of N_T are respectively 0.61 eV, 1.5 x 10^{-17} cm^3 and 1.2 x 10^{15} cm^{-3}. To our knowledge, this is the first measurement of a hole-like trap in InAlAs.

Discussion

Similar electron trap signatures have been reported in Si-doped MBE-grown $In_{0.52}$ $Al_{0.48}As$ layers lattice-matched to InP (7), (8). The electron trap does not seem to be a DX-center-like-complex because the devices we studied did not present I-V characteristics collapse. A recent analysis (9) also finds a similar deep electron trap, labelled TED1, and supports the conclusion that its characteristics are related to the lattice-matched $In_{0.52}Al_{0.48}As$ material itself, and are independent of growth conditions and techniques, and the doping concentration.

For V_{GS} near pinchoff, the space charge region is able to modulate traps located in the buffer layer. If V_{GS} was selected well above pinchoff, the drain current transient amplitude was negligible. This indicates that the traps are located in the $In_{0.52}Al_{0.48}As$ buffer layer. It also indicates that there are no new traps introduced by doubly-straining the $In_{0.41}Al_{0.59}As/In_{0.65}Ga_{0.35}As$ top layers.

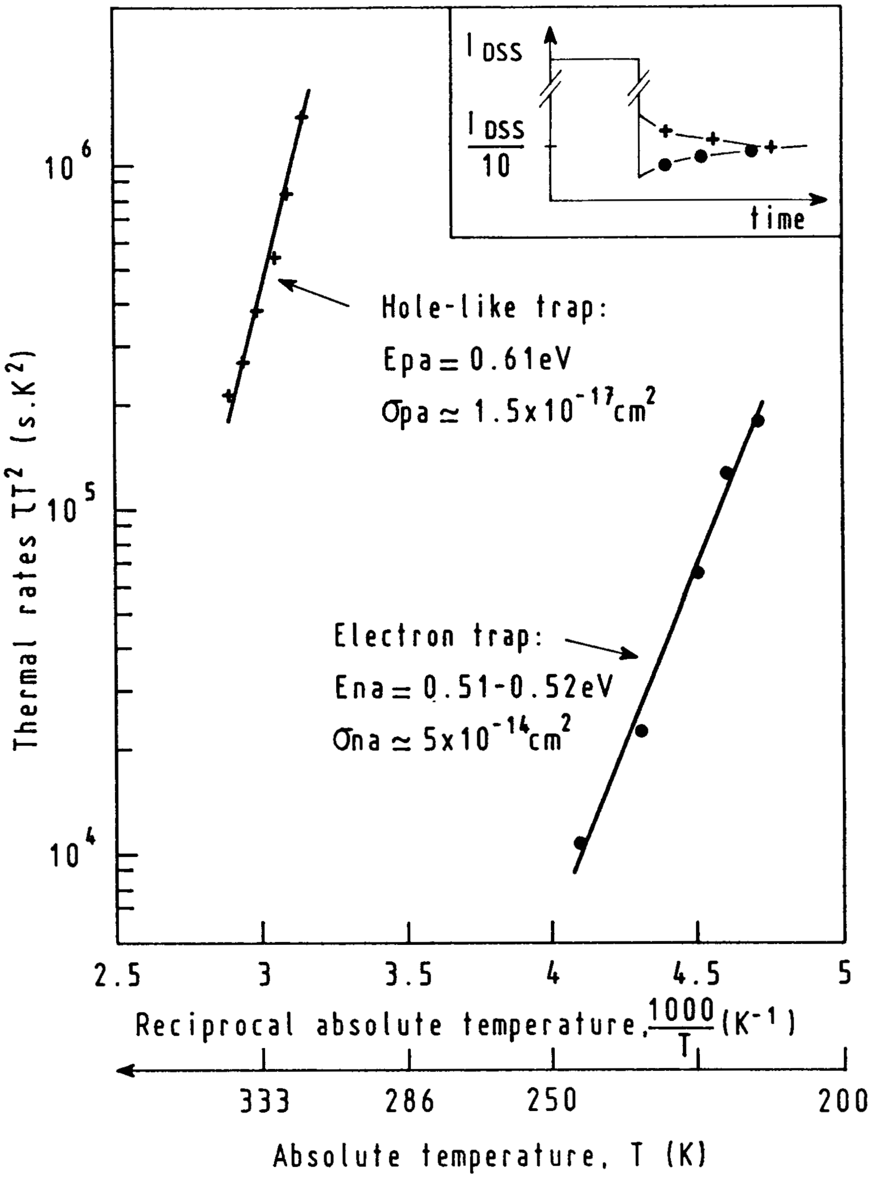

Fig. 3 : Arrhenius plots of deep levels. Associated drain current transients for the electron trap (-●-) and hole-like trap (-+-) are illustrated in the insert.

The role of the electron trap in producing the kink is confirmed by the fact that devices with higher N_T also had a higher kink amplitude. The mechanism by which these electron traps cause the kink effect is explained in ref (10). It is interesting to point out that the conduction band discontinuity of the lattice-matched InGaAs/InAlAs subchannel/buffer is ΔEc = 0.52 eV (11). We found that the energy of the electron trap is 0.51 - 0.52 eV from the InAlAs conduction band, thus the trap conduction mechanism could be by electron tunneling.

Conclusion

Two deep levels located in the InAlAs buffer layer have been measured : (i) a hole-like trap, reported for the first time and (ii) an electron trap, previously identified in the literature. The electron trap was linked to the kink effect. Trap concentrations are low : a maximum measured value of 2 x 10^{15} cm^{-3}. This value is about one order of magnitude lower than that we usually measure in GaAs buffer layers for similar gate-length devices.

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