A Recessed-Gate InAlAs/n$^+$-InP HFET with an InP Etch-Stop Layer

David R. Greenberg, *Student Member, IEEE,* Jesús A. del Alamo, *Member, IEEE,* and Rajaram Bhat, *Member, IEEE*

Abstract—**We have exploited both the attractive transport properties and the etch selectivity of InP in a novel InAlAs/n$^+$-InP metal-insulator-doped-channel heterostructure FET (MIDFET). In several other material systems, the MIDFET has been shown to be well-suited to high-power telecommunications applications. Our device employs InP both as the channel layer as well as an etch-stop layer in a selective-etch recessed-gate process. L_g = 1.8-μm devices achieve g_m and $I_{D,\max}$ values of 224 mS/mm and 408 mA/mm, respectively, the highest reported values for any InP channel HFET with $L_g \geq 0.8$ μm, including MODFET's. These figures combine with a breakdown voltage of 10 V, and peak values of f_T and $f_{\max}$ of 10.5 and 28 GHz, respectively. Our selective-etch recessed-gate process contributes to excellent device performance while maintaining a tight 60-mV threshold voltage distribution (13 mV between adjacent devices).**

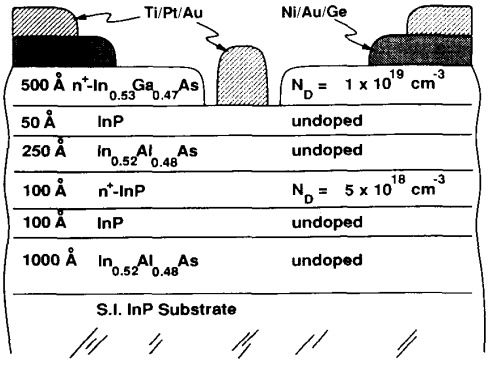

Fig. 1. Schematic cross section of the InAlAs/n$^+$-InP MIDFET.

THERE is a growing interest in the use of InP as the active channel layer in heterostructure field-effect transistors (HFET's) designed for high-power telecommunications applications because of its exceptional breakdown field and saturation velocity [1]–[3]. Recently, the metal-insulator-doped-channel HFET (MIDFET) has shown particular promise for such applications in several material systems including AlGaAs/n$^+$-GaAs [4], pseudomorphic AlGaAs/n$^+$-InGaAs [5], [6], and InAlAs/n$^+$-InGaAs [7], [8]. Featuring an undoped wide-bandgap pseudoinsulator layer with a thin, heavily doped channel, the MIDFET achieves high drain-current (I_D) linearity over a broad gate-source voltage (V_{GS}) swing, extremely broad plateaus in the V_{GS} dependence of f_T and $f_{\max}$, large breakdown voltage, and low-frequency dispersion in transconductance (g_m) [6]. These merits combine to make the MIDFET ideally suited to benefit from an InP channel. In addition, the availability of highly selective wet etchants for InGaAs and InAlAs against InP opens a variety of new fabrication possibilities employing InP as an etch stop layer. In this study, we present a novel InAlAs/n$^+$-InP MIDFET, featuring both a thin n$^+$-InP channel layer as well as an InP etch-stop layer in a selective-etch recessed-gate process. Our design results in excellent performance without sacrificing tight threshold voltage (V_T) uniformity, an important concern in a manufacturing environment.

Our heterostructure, shown in Fig. 1, consists of a 500-Å n$^+$-$In_{0.53}Ga_{0.47}As$ cap ($N_D = 1 \times 10^{19}$ cm^{-3}), a 50-Å InP etch-stop layer, a 250-Å $In_{0.52}Al_{0.48}As$ pseudoinsulator, a 100-Å n$^+$-InP channel ($N_D = 5 \times 10^{18}$ cm^{-3}), a 100-Å InP subchannel, and a 1000-Å $In_{0.52}Al_{0.48}As$ buffer/electron confinement layer. The device layers are grown on a semi-insulating (100) InP substrate at 76 torr in a low-pressure horizontal MOCVD reactor using trimethyl organometallic compounds [9].

We begin fabrication with a mesa wet etch, followed by Ni/Au/Ge ohmic contact deposition, patterning, and RTA annealing at 420°C for 10 s in an AG Associates Heatpulse 410. After gate photolithography, the n$^+$-InGaAs cap is selectively etched down to the InP etch-stop layer with 1:10:220 H_2SO_4:H_2O_2:H_2O etchant just prior to the deposition and lift-off of Ti/Pt/Au gates. Precise timing of the etch or iterative monitoring of I_D is obviated by the better than 300:1 selectivity of this etchant for InGaAs on InP, which we have verified in etch tests. Finally, we conclude fabrication with Ti/Pt/Au pad formation. For a reference, we also fabricate devices from a sample in which the cap layer is completely etched off prior to the mesa etch.

Fig. 2 shows g_m and I_D versus V_{GS} for a L_g = 1.8-μm and W_g = 200-μm MIDFET at V_{DS} = 4 V. We obtain a sharp pinchoff at $V_T = -1.8$ V. For $V_{GS} \geq -1.8$ V, g_m rises with V_{GS} in an approximately linear dependence and peaks due to the onset of significant gate leakage at 224 mS/mm, leading to a maximum I_D of 408 mA/mm. These are the highest values reported for InP-channel HFET's of

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D. R. Greenberg and J. A. del Alamo are with the Massachusetts Institute of Technology, Cambridge, MA 02139.

R. Bhat is with Bell Communications Research, Red Bank, NJ 07701.

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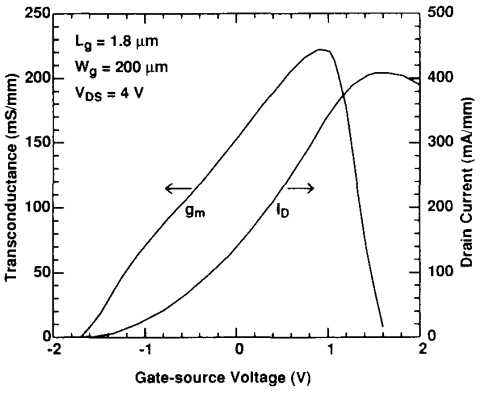

Fig. 2. g_m and I_D versus V_{GS} for a 1.8-μm × 200-μm MIDFET (V_{DS} = 4 V).

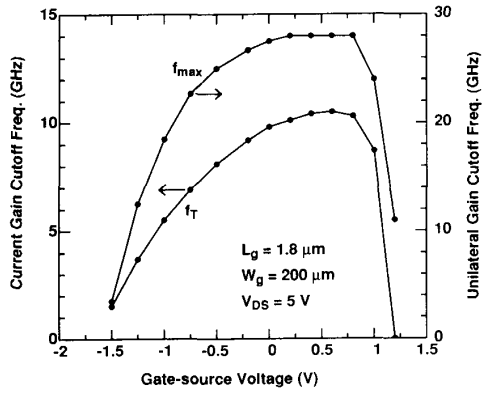

Fig. 4. f_T and f_{max} versus V_{GS} for a 1.8-μm × 200-μm MIDFET (V_{DS} = 5 V).

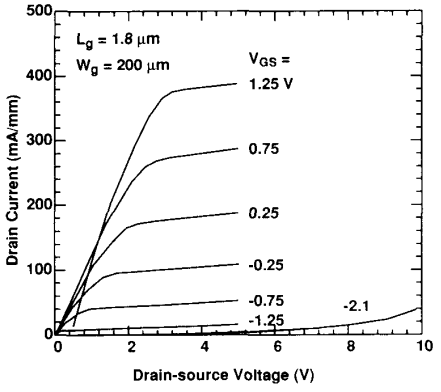

Fig. 3. I_D versus V_{DS} for a 1.8-μm × 200-μm MIDFET, showing drain-source breakdown.

$L_g \geq 0.8$ μm, including MODFET's [2], [3]. Fig. 3 shows I_D versus V_{DS} for the same device. Drain conductance is 6 mS/mm at peak g_m, which yields a high voltage gain of 40. In addition, we observe a drain-source breakdown voltage BV_{DS} of about 10 V, defined at I_D = 40 mA/mm (10% of maximum I_D). The majority of I_D beyond breakdown flows through the gate, indicating that the intrinsic gate structure is responsible for breakdown rather than the channel.

Like g_m, f_T and f_{max} rise linearly with V_{GS}, as shown in Fig. 4, peaking at 10.5 and 28 GHz, respectively. From the value of f_T, we can extract an average channel electron velocity v_e of 1.2×10^7 cm/s. The linear rise of both g_m and f_T with V_{GS} clearly indicates that our devices remain in the mobility-limited electron transport regime over their entire operating range ($\mu_n \simeq 1600$ cm^2/V · s, as determined from the slope of f_T versus V_{GS} near threshold). This is in contrast with the broad g_m and f_T plateaus due to velocity saturation v_{sat} that are visible in MIDFET's of similar L_g fabricated in other material systems [10], [11]. The absence of v_{sat} in our n$^+$-InP channel devices stems from the high electric field of about 10 kV/cm needed to approach v_{sat} in InP [12], which is larger than the average field of about 7 kV/cm achieved in our devices at peak g_m. These factors emphasize the need for submicrometer L_g scaling to fully realize the benefits of the InAlAs/n$^+$-InP MIDFET design. As long as peak f_T remains mobility-limited, however, we expect f_T to scale up as $1/L_g^2$, to an estimated 30 GHz at L_g = 1 μm, comparable with L_g = 1-μm InP-channel MODFET's [13].

From a manufacturing point of view, V_T uniformity is of great importance. Conventional recessed-gate processes that employ a timed etch or I_D monitoring have difficulty in realizing high V_T uniformity because they are unable to control the depth of the cap etch with sufficient precision. By using an InP etch stop layer, however, our devices achieve a tight 60-mV standard deviation in V_T about an average V_T of -1.77 V for 30 devices (with V_T measured to a resolution of 10 meV by extrapolating $I_D^{1/2}$ versus V_{GS} to the V_{GS} axis). Most of the observed V_T variation results from a monotonic shift in V_T from -1.67 to -1.91 V in moving across the wafer due to growth-related channel doping variation and not from our cap etch. Indeed, the V_T difference between adjacent devices has a standard deviation of only 13 mV over 15 pairs of devices, which is at the limit of our V_T resolution.

The excellent values of g_m and I_D achieved in our devices is due in large part to a reduction in parasitic R_s by our cap layer. Comparison with the uncapped reference device shows that, for small currents (below 100 mA/mm), the cap reduces the extrinsic sheet resistance R_{sh} from about 1400 to about 600 $\Omega/\square$, as measured using the floating-gate TLM technique [14]. This reduction is due to the well-known screening of surface Fermi level pinning [15]. At larger currents (above 100 mA/mm), however, R_{sh} drops dramatically to 50 $\Omega/\square$, the value of R_{sh} for the cap layer itself. This suggests that the cap acts to further reduce extrinsic R_s by conducting I_D above 100 mA/mm in parallel with the extrinsic channel. At these high currents, the potential drop in the extrinsic channel is sufficient to turn on the cap/pseudoinsulator/extrinsic channel SIS junction, which has a low effective barrier height (less than 0.1 eV) due to the high doping level in the cap layer. The point at which the SIS junction turns on and parallel conduction through the cap begins is clearly marked by a kink in g_m versus V_{GS} at

I_D = 100 mA/mm. By 400 mA/mm, R_s is reduced to about 1.5 $\Omega \cdot$ mm. The resulting low R_{sh} of the extrinsic source makes our devices very insensitive to the gate–source gap (L_{gs}). In particular, devices fabricated with L_{gs} ranging from 2 μm (the standard gap length) through 10 μm display a drop in peak g_m of less than 10% in moving from the smallest to largest L_{gs}.

In summary, we have fabricated high-performance InAlAs/n$^+$-InP MIDFET's using InP both as the channel layer and as a novel etch-stop layer in a selective-etch recessed-gate process. Our devices achieve outstanding values of peak g_m and I_D. We find that our selectively recessed cap significantly reduces R_s by participating in current conduction in parallel with the extrinsic channel, contributing to performance without sacrificing tight uniformity in V_T.

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