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An InAlAs/InAs MODFET

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Abstract—**We report what we believe is the first InAs modulation-doped field-effect transistor (MODFET) using an epitaxial heterostructure based entirely on arsenides. The heterostructure was grown by MBE on InP and contains a 30-Å InAs channel. An L_G = 2-μm device displays well-behaved characteristics, showing sharp pinch-off (V_{th} = −0.8 V) and small output conductance (5 mS/mm) at 300 K. The maximum transconductance is 170 mS/mm with a maximum drain current of 312 mA/mm. Strong channel quantization results in an unprecedented breakdown voltage of −9.6 V, a several-fold improvement over previous InAs MODFET's based on antimonides. Low-temperature magnetic field measurements show strong Shubnikov–de Haas oscillations which, over a certain range of gate voltage, strongly hint that the electron channel resides in the InAs layer.**

THE small electron effective mass of InAs makes this material an attractive candidate for the active channel of heterostructure field-effect transistors (HFET's) since it results in high electron mobility and large electron peak velocity with potential for high-performance devices [1]. Additionally, the low effective mass of InAs might bring about stronger electron quantization and longer electron coherence lengths, which is promising for quantum-effect electronic devices with high operating temperatures [2]. Recently, the first InAs channel HFET's have been fabricated with barriers based on antimonides [3], [4]. It would, however, be of interest to develop InAs channel HFET's that only contain arsenides because of their well-established growth and processing technologies.

In this paper we describe the fabrication and characterization of an InAlAs/InAs MODFET. The device shows excellent characteristics at room temperature with strong channel quantization resulting in a very large breakdown voltage. We have carried out low-temperature magnetic field measurements to confirm that the electron channel resides in the InAs layer.

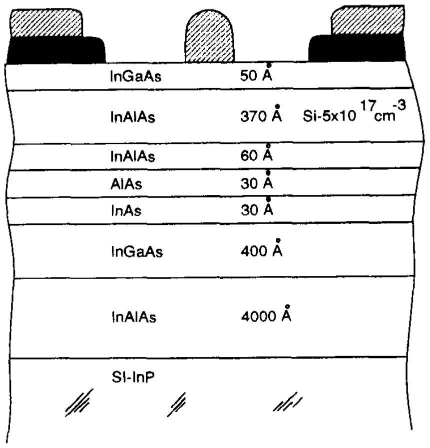

Fig. 1. Cross section of device structure.

For the growth of our heterostructure, we have taken advantage of recent progress in MBE growth of highly strained AlAs/InAs heterostructures on InP for resonant tunneling devices [5]. The heterostructure shown in Fig. 1 consists, from top to bottom, of a 50-Å undoped $In_{0.53}Ga_{0.47}As$ cap, a 370-Å n$^+$-$In_{0.52}Al_{0.48}As$ (Si doped at 5 × 10^{17} cm^{-3}) supply layer, a 60-Å undoped $In_{0.52}Al_{0.48}As$ spacer, a 30-Å undoped AlAs barrier, a 30-Å undoped InAs channel, a 400-Å undoped $In_{0.53}Ga_{0.47}As$ buffer, and an undoped 4000-Å $In_{0.52}Al_{0.48}As$ buffer on a (100) SI-InP substrate.

Except for the InAs and AlAs layers, growth was carried out at an As/In beam-equivalent pressure ratio of 25 and a growth rate of 0.8 μm/h. The substrate growth temperature for all the layers except the InAs layer was 490°C. In order to maintain two-dimensional growth, the InAs layer was grown at 420°C after a growth interruption during which the substrate temperature was ramped down. Then a monolayer of GaAs was grown on top of the InAs to prevent evaporation and, with growth interrupted again, the temperature was ramped up to 490°C [6]. The InAs and AlAs layers were grown at one monolayer/second. The InAs thickness was limited to 30 Å because reflection high-energy electron diffraction (RHEED) oscillations were no longer observed for thicker InAs layers. This is consistent with the maximum thickness of InAs of 30 Å that de Miguel *et al.* were able to grow by MBE and still observe strong photoluminescence in $In_{0.52}Al_{0.48}As$/InAs quantum wells on InP [7], [8].

Device processing proceeded with mesa isolation using a H_2SO_4:H_2O_2:H_2O in a 1:10:220 solution. The etch rate was about 60 Å/s. Ohmic contacts were formed by rapid-thermal annealing a 50-Å Ni/50-Å Au/250-Å Ge/450-Å Au/100-Å Ni/500-Å Au multilayer in an AG Associates 410 reactor at 360°C for 10 s. Finally, a 350-A/3500-Å bilayer of Ti/Au was lifted off to form the gate and pads. The measurements reported here are for a typical L_G = 2-μm and W_G = 20-μm MODFET with a source-drain separation of 10 μm.

The room-temperature output characteristics, shown in

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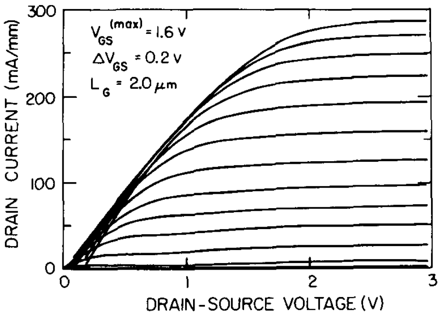

Fig. 2. I_D-V_{DS} characteristics of an L_G = 2-μm device at room temperature.

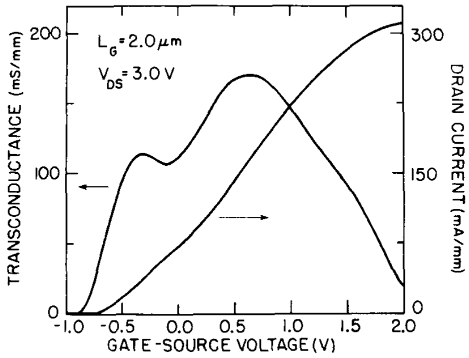

Fig. 3. Transconductance and I_D-V_{GS} characteristics of an L_G = 2-μm device at room temperature.

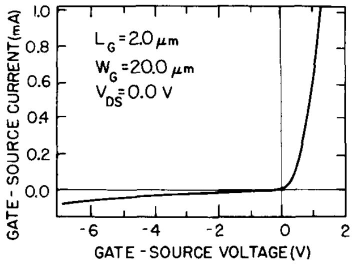

Fig. 4. Gate current characteristics of a 2-μm device at room temperature (V_{DS} = 0 V).

Fig. 2 for a typical device, are well behaved, displaying a sharp pinch-off ($V_{th} = -0.8$ V) and small output conductance (5 mS/mm). These characteristics represent a significant improvement over InAs HFET's based on antimonides which have not shown complete pinch-off and also have rather large output conductances at V_{DS} as small as 1 V [3], [4]. The transconductance at $T = 300$ K, shown in Fig. 3, displays a double-hump feature and has a maximum g_m of 170 mS/mm. We will show that the first hump corresponds to the initial turn-on of the InAs layer and the second corresponds to the additional turn-on of the InGaAs layer underneath the InAs. The intrinsic transconductances g_{mo}, calculated after accounting for source resistance (computed below) for the first and second peak, are 180 and 380 mS/mm, respectively. As Fig. 3 shows, there is a broad gate voltage of roughly 1.5 V at which the transconductance is greater than 100 mS/mm. This allowed a maximum drain current of 312 mA/mm before the onset of parallel conduction through the InAlAs barrier.

An outstanding feature of this device is its high breakdown voltage. As Fig. 4 shows, the reverse gate leakage current is as small as 78 μA at $V_{GS} = -7$ V ($V_{DS} = 0$ V). The breakdown voltage of this device occurred at $V_{GS} = -9.6$ V. This is a significant improvement over previous InAs HFET's which at best had a source-drain breakdown voltage of less than 1.5 V. Our results arise from the artificial enlargement of the bandgap produced by strong electron quantization in the 30-Å InAs well, as Bahl and del Alamo have experimentally found in quantum-channel InAlAs/InGaAs HFET's [9].

The contact resistance measured using a four-probe transmission-line method (TLM) was 0.3 Ω · mm and the sheet resistance was 728 Ω/□ at room temperature. The series resistance, including the contact resistance, for our 4-μm gate-source gap was 3.2 Ω · mm. From Fig. 3, the K factor for the first hump, which is attributed below to transport through the InAs layer, equals 328 mS/mm · V. Taking into account series resistance, this translates into a mobility of 5400 cm^2/V · s for the InAs layer. The K factor for the second hump, which results from the additional turn-on of the InGaAs layer, is 129 ms/mm · V. From this we calculate the mobility to be 9000 cm^2/V · s for the InAs/InGaAs channel.

In order to try to confirm that transport is actually taking place through the InAs channel, we carried out low-temperature magnetic field measurements [6]. In a fixed magnetic field, we observed strong oscillations in the gate voltage dependence of the transconductance at 4 K that are a result of the Fermi level sweeping through the fixed Landau levels produced by the magnetic field [10]. From the spacing between two oscillations, ΔV_{GS}, we can directly extract the gate-channel capacitance as a function of V_{GS} [10]. The capacitance was confirmed to be independent of magnetic field for field strengths between 2 and 6 T. It is important to emphasize that these measurements are carried out on the actual FET's and are not CV characteristics taken on adjoining diode test structures.

For V_{GS} between 0 and -0.5 V, the capacitance was found to be $2.08 \pm 0.15 \times 10^{-7}$ F/cm^2. From this value we estimate the channel depth to be 529 ± 45 Å. This is very close to the center of the InAs layer, which from the MBE growth calibrations is expected to be at 525 Å. As the InGaAs channel turns on with V_{GS} greater than about 0 V, the capacitance decreases to $1.76 \pm 0.11 \times 10^{-7}$ F/cm^2, corresponding to a channel depth of 644 ± 46 Å. This is 134 Å from the InAs/AlAs interface, well into the InGaAs subchannel. The capacitance data have a standard deviation of 6-7%, which translates in an uncertainty in the centroid position comparable to the InAs layer thickness. In itself, therefore, this measurement cannot unequivocally place the electron channel in the InAs layer. The unusual fact that the capacitance *drops* as V_{GS} increases, however, is consistent with our hypothesis that at around 0 V, the electrons start spilling out of the InAs well into the InGaAs layer. This set of measurements strongly hints at the existence over a certain regime of V_{GS} of an electron channel inside the InAs well.

These findings suggest that the first rise in the transconductance curve of Fig. 3 arises from transport in the InAs channel and the second rise in g_m has its origin in the further turn-on of the InGaAs layer underneath. The small dip in transconductance in the transition between the two regimes might arise from a reduction of mobility that results from enhanced intersubband scattering [11]. This has been observed in AlGaAs/GaAs MODFET structures at low temperatures when a second subband in the 2DEG begins to be occupied. In our case, as simple calculations show, the first subband is entirely confined to the InAs well but the second one extends into the InGaAs layer.

The mobility of the InAs layer, about 5400 $\text{cm}^2/\text{V} \cdot \text{s}$, is relatively low in comparison with what one might expect from such a low effective mass material. Transport asymmetry in the sample suggests that there might be some dislocations which would limit the mobility. A second possibility is the roughening of the InAs/AlAs interface as a result of excessive strain. This was observed by TEM by de Miguel *et al.* in their 30-Å InAlAs/InAs quantum-well structure [7], [8]. If any of these are the case, then in order to increase the mobility in future devices, the InAs layer should be thinner. A final possibility for our low μ_e would have its origin from the severe warping of the conduction band of InAs [12]. This results in a much heavier electron effective mass at high energies [12], where electrons in our strongly quantized channel are likely to reside. This could well be a fundamental limitation of InAs FET's.

In conclusion, we have reported excellent device characteristics with sharp pinch-off and unprecedented breakdown voltages in InAlAs/InAs MODFET's. The results show substantial improvements in device characteristics over InAs MODFET's based on antimonides. This is largely due to the more established growth and processing technologies of arsenides over antimonides and the effective bandgap enhancement through strong electron quantization.

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