In estimating the overshoot width, a model with v_{av} was used and the resultant overshoot width was much wider than that simply evaluated from Γ to L valley separation, or predicted by Monte Carlo sumulations [6]. The present calculation answers the apparently wider overshoot width. For example, for a given v_{eff} value of 1.5×10^7 cm/s and a saturation velocity of 5×10^6 cm/s (that is, $v_{eff}/v_s = 3$), the curves for $v_o/v_s = 8$ in Fig. 3 present $W_o/W_C \approx 0.75$ on the v_{av} curve, whereas $W_o/W_C \approx 0.5$ on the v_{eff} curve. The W_o/W_C ratio of 0.5, which corresponds to an overshoot width of about 1000 Å in the previous structure, is fairly reasonable. Further discussion will need a modeling for the overshoot profile in the device to fit the present analysis.

In summary, the collector transit time and the effective carrier velocity in the collector with velocity overshoot have been analyzed using a step-like velocity profile model. It has been pointed out that the contribution of the overshoot to the reduction of the transit time is much greater than that estimated simply applying an average velocity v_{av} over the collector depletion layer. The effective velocity v_{eff}, which is defined by $W_C/2\tau_C$, varies more gradually with a fraction of the overshoot width than v_{av}.

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An All-Electrical Floating-Gate Transmission Line Model Technique for Measuring Source Resistance in Heterostructure Field-Effect Transistors

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***Abstract*—A new technique for determining the parasitic source resistance in Heterostructure Field-Effect Transistors (HFET's) is presented. The new technique is an improvement of the Floating-Gate Transmission Line Model (FGTLM), and uses purely electrical measurements, that is, there is no need to determine any critical lengths optically or by scanning electron microscopy. The technique is demonstrated in $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ Metal-Insulator Doped semiconductor Field-Effect Transistors (MIDFET's). The new technique holds great promise for automated measurements of source resistance in a manufacturing environment.**

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The parasitic source and drain resistances severely limit the performance of Heterostructure Field-Effect Transistors (HFET's). Specifically, since the source resistance R_s degrades the transconductance g_m, its minimization is of great relevance. In order to do that, one must first be able to measure R_s accurately. The Transmission-Line Model (TLM) method [1], [2], has been the most popular technique for measuring R_s. Also, a number of other techniques for evaluating the source resistance in metal-semiconductor field-effect transistors (MESFET's) and modulation-doped field-effect transistors (MODFET's) based on "end" resistance have been proposed [3]-[9]. Unfortunately, these techniques require simplistic assumptions on the behavior of gate current as a function of gate voltage. Typically, an exponential dependence is assumed [3]-[9]. However, a new, simple, and accurate measurement technique for extracting source resistance, called the Floating-Gate Transmission-Line Model (FGTLM) has been recently proposed and demonstrated by the authors [10]. This new technique does not place any restrictive requirements on the gate current.

The FGTLM technique accurately determines the values of the source and drain resistances by utilizing actual HFET structures of various gate lengths. The FGTLM provides two main advantages over the TLM. First, since measurements are carried out on the devices themselves, no special test structure that consumes valuable chip area is needed. Second, unlike a field-effect transistor structure, the TLM structure does not have a "gate," and therefore, the spreading resistance due to current crowding at the source end of the gate cannot be correctly measured by the TLM.

In our original FGTLM work [10], the actual dimensions of the FET's were determined by using a scanning electron microscope (SEM) with a precision of 0.1 μm. As such, the measurement techniques utilized in the FGTLM were not purely electrical but involved microscopy techniques as well. This is a serious drawback for the FGTLM, particularly from a manufacturing viewpoint where fully automated testing is essential. The TLM suffers from the same drawback. In this brief we propose and demonstrate a new approach to our earlier work in which the need for detailed microscopy measurement techniques is completely eliminated. Thus our new approach, unlike the conventional TLM, can now be fully automated.

Fig. 1 is a linear resistive network which schematically represents a generic HFET with either a two-dimensional electron gas or a doped channel, biased in the linear mode of operation [10]. Using the FGTLM technique, floating-gate measurements of gate-source, gate-drain, and drain-source resistances are carried out [10]. For example, the gate-source resistance with the gate floating, $R_{gs}(\mathrm{fg})$, is measured by injecting a small current from source to drain, and measuring the voltage drop between gate and source, with a high-impedance voltmeter. Similarly for other resistances. By inspection of Fig. 1, one finds [10]

$$R_{gs}(\mathrm{fg}) = R_s + \tfrac{1}{2} R_{\mathrm{ch}} \tag{1}$$

$$R_{gd}(\mathrm{fg}) = R_d + \tfrac{1}{2} R_{\mathrm{ch}} \tag{2}$$

$$R_{ds}(\mathrm{fg}) = R_s + R_d + R_{\mathrm{ch}} \tag{3}$$

where fg in brackets implies that the gate is floating, and R_{ch} represents the channel resistance.

Similarly, the gate-source resistance measured with the source

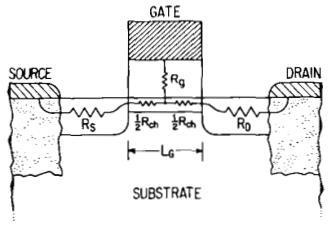

Fig. 1. Diagram of HFET showing inverted T-type linear resistive network, valid in the linear regime.

floating (fs) is found to be

$$R_{gs}(\text{fs}) = R_g \tag{4}$$

where R_g is the gate barrier resistance.

Furthermore, for short gate lengths we found [10]

$$R_{ch} = RL_g \tag{5}$$

$$R_g = \frac{1}{GL_g} \tag{6}$$

where R represents the resistance per unit length in the channel (in Ω/μm) and G represents gate-to-channel conductance per unit length of channel (in $\Omega^{-1} \cdot \mu\text{m}^{-1}$).

Substituting for R_{ch} and R_g from (5) and (6) into (1)–(4) gives

$$R_{gs}(\text{fg}) = R_s + \tfrac{1}{2}RL_g \tag{7}$$

$$R_{gd}(\text{fg}) = R_d + \tfrac{1}{2}RL_g \tag{8}$$

$$R_{ds}(\text{fg}) = R_s + R_d + RL_g \tag{9}$$

$$R_{ds}(\text{fs}) = \frac{1}{GL_g}. \tag{10}$$

Solving (10) for L_g and substituting for it in (7)–(9) gives

$$R_{gs}(\text{fg}) = R_s + \frac{1}{2}\frac{R}{G}\frac{1}{R_{gs}(\text{fs})} \tag{11}$$

$$R_{gd}(\text{fg}) = R_d + \frac{1}{2}\frac{R}{G}\frac{1}{R_{gs}(\text{fs})} \tag{12}$$

$$R_{ds}(\text{fg}) = R_s + R_d + \frac{R}{G}\frac{1}{R_{gs}(\text{fs})}. \tag{13}$$

According to (11), a plot of $R_{gs}(\text{fg})$ versus $1/R_{gs}(\text{fs})$ would yield a straight line, which when extrapolated to $1/R_{gs}(\text{fs}) = 0$, would give the value of R_s. Similarly, a plot of $R_{gd}(\text{fg})$ versus $1/R_{gs}(\text{fs})$ would yield a value for R_d, and a plot of $R_{ds}(\text{fg})$ versus $1/R_{gs}(\text{fs})$ would yield $(R_s + R_d)$.

The all-electrical technique was applied to $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ metal–insulator-doped semiconductor field-effect transistors (MIDFET's) with a thin and heavily doped channel. The details of fabrication of this specific device have been reported in [11]. FET's with a gate width of 28 μm and nominal gate lengths of 1, 1.5, 2, 3, 5, and 10 μm were measured in the present experiment. All the resistances were measured by a Kelvin technique to eliminate the influence of probe-contact resistance using an HP4145A semiconductor parameter analyzer. All the resistances were checked to be independent of bias for small excursions around zero, insuring that the linear model in Fig. 1 is valid.

Fig. 2 plots $1/R_{gs}(\text{fs})$ as a function of gate length, measured by SEM. Notice how the data follow a straight line, as (10) requires, intersecting very close to the origin. This confirms the validity of (10) in our experiment, and is a crucial test for determining the correctness of the all-electrical FGTLM. Although we used *actual* gate lengths to perform this check (to demonstrate the valdity of the method), the prospective user has to simply check that $1/R_{gs}(\text{fs})$ is directly proportional to *as-drawn* gate length, without requiring SEM measurements. In all the devices we have measured, this linearity has been found to hold.

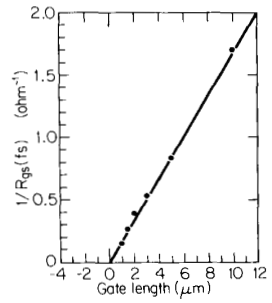

Fig. 2. Plot of $1/R_{gs}(\text{fs})$ versus L_g, displaying that our experimental data do indeed fall on a straight line passing through the origin, as (10) requires.

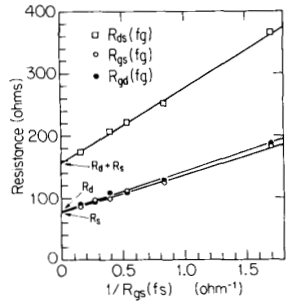

Fig. 3. Plots of $R_{gs}(\text{fg})$, $R_{gd}(\text{fg})$, and $R_{ds}(\text{fg})$ versus $1/R_{gs}(\text{fs})$. Experimental data fall on straight lines in each of the three cases demonstrating the validity of the all-electrical FGTLM technique.

Fig. 3 plots $R_{gs}(\text{fg})$, $R_{gd}(\text{fg})$, and $R_{ds}(\text{fg})$ as a function of $1/R_{gs}(\text{fs})$. Our experimental data do indeed fall on straight lines in each of the three cases, demonstrating the validity of our technique. Furthermore, the intersections with the ordinate axis yield an $R_s = 77.9\ \Omega$ (from $R_{gs}(\text{fg})$), an $R_d = 78.5\ \Omega$ (from $R_{gd}(\text{fg})$), and an $(R_s + R_d) = 157.9\ \Omega$ (from $R_{ds}(\text{fg})$). These values not not only display excellent internal consistency, but are also in good agreement with the respective values of $R_s = 76.7\ \Omega$, $R_d = 78.0\ \Omega$, and $(R_s + R_d) = 154.4\ \Omega$ reported in [10], that were extracted, on the same devices, with the aid of SEM measurements. The residual discrepancy between the two sets of data, about 2%, is due to the error in SEM measurement of gate-to-source spacing.

Because the all-electrical FGTLM technique does not rely on actual measurements of L_g (Fig. 3 is all that is needed), it is insensitive to any difference between the nominal gate length and the real gate length on the wafer. For the same reason, it is also insensitive to any differences that may exist between the metal gate length and the actual electrical gate length of the depletion region in the device. For this reason, the new technique can be applied to T-type or mushroom-type gates. It also works for asymmetrically placed gates, and for nonheterostructure FET's with some gate leakage, such as MESFET's or junction FET's (JFET's).

In conclusion, our new all-electrical FGTLM technique enables us to accurately and quickly extract the source and drain resistances without resorting to SEM measurements. The prospective user must check that $R_{gs}(\text{fg})$, $R_{gd}(\text{fg})$, and $1/R_{gs}(\text{fs})$ are directly proportional to *as-drawn* gate length; there is no need to confirm these direct proportionalities for *actual* gate lengths, which eliminates the need for SEM measurements. This provides a vital advantage over the TLM technique in that measurements can now be fully

automated. Therefore, our new technique can be implemented in a manufacturing environment.

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