Criteria for One-Dimensional Transport in Split-Gate Field-Effect Transistors

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Abstract

We have fabricated AlGaAs/GaAs split-gate field-effect transistors with different lengths and widths in order to establish geometric design criteria for one-dimensional (1D) transport. The experiments show a more negative 1D threshold voltage for zero length split-gate devices (constrictions) than finite length split-gate devices for the same given width. The experiments reveal the existence of a *critical width* between the gates below which a 1D regime cannot be supported in split-gate FETs longer than 0.5 μm.

Introduction

The rapid miniaturization of today's electronic devices will soon lead to devices with dimensions comparable to the electron wavelength. In this regime the electron energy levels are quantized. MODFETs and quantum well lasers are recent examples of two-dimensional (2D) quantized heterostructure devices which have found multiple applications in communication systems. The logical next step is to study one-dimensional (1D) electronic systems and explore original device concepts which might result in new breakthroughs in device functionality.

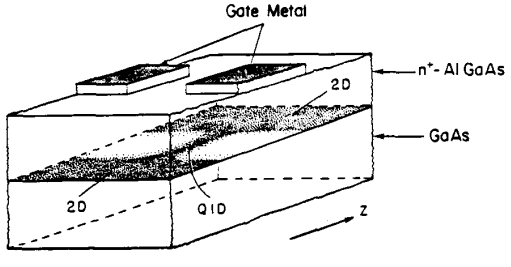

Figure 1. Conceptual illustration of the quantum wire formed in a split-gate field-effect transistor.

A split-gate field-effect transistor (FET) is essentially an FET with a narrow slit in the gate [1]. If a modulation-doped FET (MODFET) semiconductor structure is designed normally on or depletion-mode, then the split-gate scheme is an easy way to obtain a narrow channel field-effect transistor. A negative gate voltage depletes the 2D electron gas (2DEG) underneath the gates but leaves a narrow conducting channel in between, as shown in Fig. 1. If the electrical width of this channel is comparable to the electron wavelength (about 500 Å), then the device in this regime is inherently an FET with a 1D channel or a field-effect quantum wire. The channel length compared to the coherence length of the material determines whether transport through the channel is ballistic or diffusive.

The purpose of this work is to establish the geometrical criteria of split-gate AlGaAs/GaAs FETs for 1D transport.

Fabrication

In our experiments a split-gate scheme is used to create a 1D electron channel at the interface of an AlGaAs/GaAs modulation doped FET (MODFET) structure grown by MBE. The heterostructure consists, from top to bottom, of a 5 nm undoped GaAs cap, a 42 nm AlGaAs barrier doped with Si at 5×10^{18} cm^{-3}, a 7.5 nm undoped AlGaAs spacer, and a 1 μm GaAs buffer. The mobility of the 2D electron gas is 7,200 cm^2/V·sec at room temperature, 55,000 cm^2/V·sec at 77 K, and 100,000 cm^2/V·sec at 4.2 K. The 2D carrier density at 4.2 K is 9×10^{11} cm^{-2} and 1×10^{12} cm^{-2} at 77 K and 300 K. The devices were isolated by a mesa etch. Ohmic contacts were formed by annealing Au/Ge/Ni at 420° C for two minutes. The gate pads consist of an optically defined, lifted-off Ti/Au bilayer. The actual confining split-gates were fabricated using electron-beam lithography and are connected to the large optically-defined gates.

The confining gates were defined by electron-beam exposure of a bilayer PMMA (polymethylmethacrylate) resist. Two molecular weights of PMMA were cast in solutions of MIBK (methylisobutylketone), in a process similar to that described in reference [2]. The resist was exposed with 50 keV electrons using a JEOL JBX5DII electron-beam lithography system. In our work, the actual 1D channel is confined by two 40 nm wide lifted-off Au/Pd lines drawn with a single electron-beam pass, as shown in Fig. 2. In this approach there is no need to expose the area contained inside these lines. This reduces electron beam

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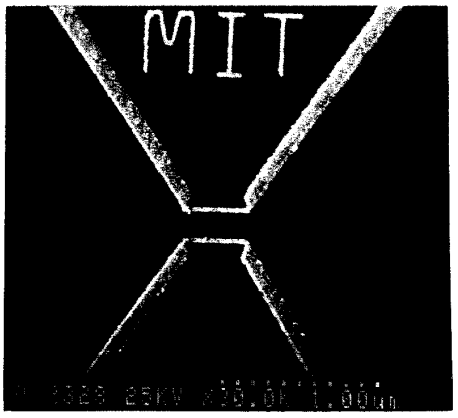

Figure 2. Scanning electron micrograph of a 0.5 μm long, 0.2 μm wide quantum wire. The white areas are the Au/Pd gates.

writing times, gate leakage, and gate capacitance.

Devices with different lithographic dimensions of the split-gate were fabricated:

- the distance between the confining gates, defined as the lithographic width, W, was varied from 0.1 μm to 0.5 μm in increments of 0.05 μm for the constrictions, including a continuous gate (W = 0.0 μm) and varied from 0.1 μm to 0.3 μm in increments of 0.05 μm for the quantum wires;
- the lengths, L, of the confining gates in the direction of electron transport were 0.0 μm (constriction, shown in Fig. 3), 0.5 μm, and 1.0 μm.

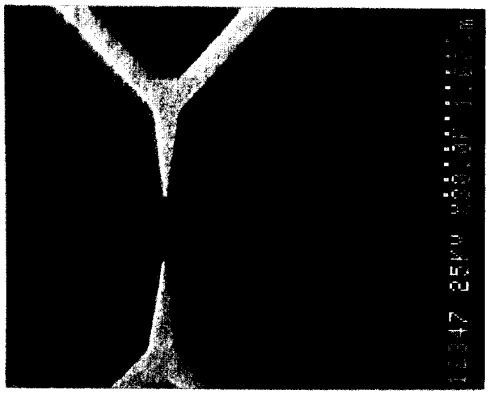

Figure 3. Scanning electron micrograph of a constriction. The separation between the confining gates is 0.3 μm.

Results

The source current versus gate-source voltage (I_S-V_{GS}) characteristics of the split-gate MODFETs were obtained by two techniques. The first consisted of using a lockin technique at 96 Hz with the drain-source voltage (V_{DS}) at typically 100 μV rms. V_{GS} was swept and I_S was measured in phase with V_{DS}. This approach minimized the impact of gate leakage since the gate current was DC to the first order. In the second set-up, an HP4145B Semiconductor Parameter Analyzer was utilized to directly obtain the I_S-V_{GS} characteristics of the devices. V_{DS} was in this case 25 mV. Both techniques were used at 4.2 K and 300 K.

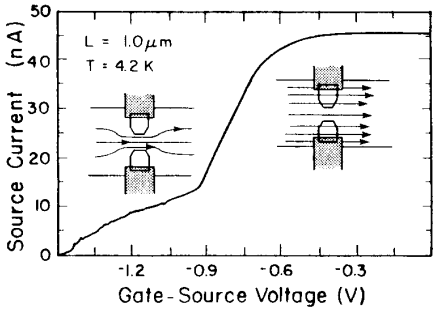

Figure 4. I_S-V_{GS} characteristics of a 1.0 μm long quantum wire. The inset illustrations show, from left to right, the 1D regime and the 2D regime respectively. The tail in the curve is the 1D regime. V_{DS} was 100 μV.

Fig. 4 shows typical I_S-V_{GS} characteristics obtained using technique 1 for a wire length L = 1.0 μm and width W = 0.25 μm at 4.2 K. Two prominent features are observed. The 2D regime is characterized by a linear drop in current, I_S, with respect to the gate voltage, V_{GS}, as the 2DEG is depleted underneath the gates. The 1D regime manifests itself as a prominent tail in the I_S-V_{GS} characteristics as the narrow channel is pinched off through the fringing fields of the gate, displaying a more negative threshold voltage than the 2D regime. We define the intercept of the linear drop off and the 1D tail as the 2D threshold voltage, V_{t2D}. The 1D threshold voltage, V_{t1D}, is defined as the pinch off voltage (I_S = 0). These distinct features, shown

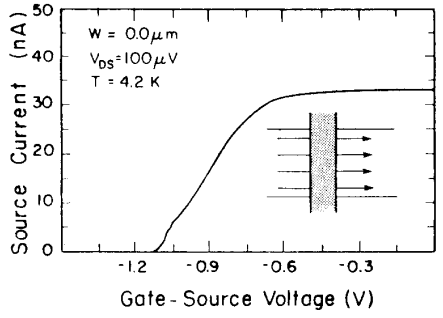

Figure 5. I_S-V_{GS} characteristics of a device with a continuous gate between source and drain. Only a 2D regime is observed.

in Fig. 4, were observed at temperatures from 4.2 K to 300 K. The identification of these two regimes was verified by: 1) examining the characteristics of a continuous gate FET, shown in Fig. 5, in which only a single linear current drop was observed; 2) the independence of the 1D regime to magnetic field, shown in Fig. 6; 3) and the observation of 1D ballistic quantized steps [3-5] in the tail for a 0.5 μm long quantum wire at 4.2 K, shown in Fig. 7 [6].

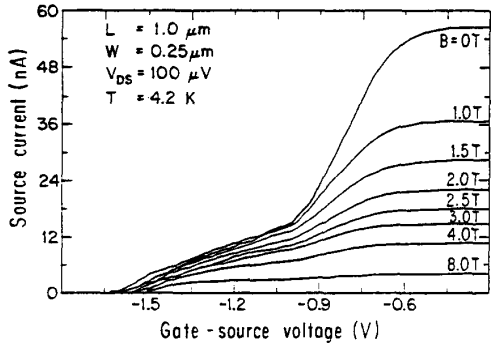

Figure 6. I_S-V_{GS} characteristics of a 1.0 μm device in an orthogonal magnetic field up to 8 Tesla.

With the establishment of the two different regimes represented in the I_S-V_{GS} characteristics, a detailed analysis of the presence or absence of the 1D regime in the different fabricated devices was undertaken. The I_S-V_{GS} characteristics of 1.0 μm long quantum wires with different widths are shown in Fig. 8, as obtained with technique 2 at 300 K. The characteristic tail of the 1D regime is only present in the wires with distances between the gates greater than 0.2 μm, as indicated by the shading in Fig. 8. Statistical measurements for the 1.0 μm long quantum wires show a *critical width* of about 0.2 μm below which the 1D regime cannot be supported. This can be understood if the electrostatic action of the gate extends beyond its geometrical dimensions, as has been found in submicron MESFETs [7]. An upper limit for the wire width that can be pinched off arises from gate leakage and gate breakdown, as seen in the upper trace of Fig. 8.

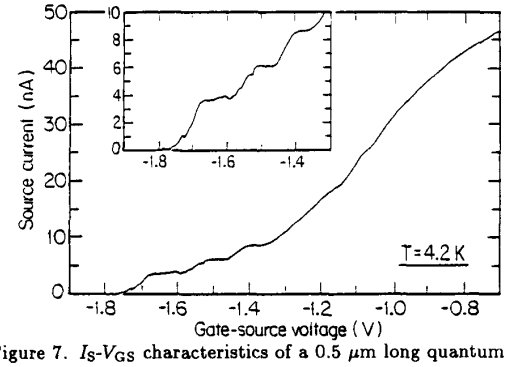

Figure 7. I_S-V_{GS} characteristics of a 0.5 μm long quantum wire at T = 4.2 K with V_{DS} = 100 μV. The quantized steps in current arise from near ballistic 1D transport.

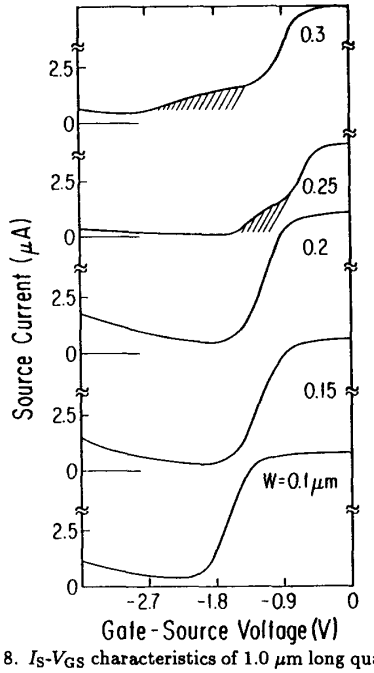

Figure 8. I_S-V_{GS} characteristics of 1.0 μm long quantum wires at V_{DS} = 25 mV and T = 300 K. Widths between confining gates vary from 0.1 μm to 0.3 μm. The shaded tail shows the 1D regime.

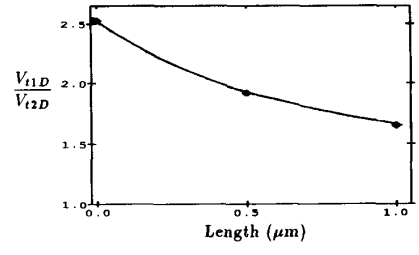

Figure 9. The ratio of the 1D threshold voltage, V_{t1D}, to the 2D threshold voltage, V_{t2D}, as a function of the length of the confining split-gates for W = 0.25 μm.

We also studied the effect of length of the split-gate on the I_S-V_{GS} characteristics. Fig. 9 shows the results of the ratio between the 1D threshold voltage and the 2D threshold voltage, V_{t1D}/V_{t2D}, as a function of length for W = 0.25 μm. The ratio drops quickly from 0.0 μm to 0.5 μm but saturates with increasing wire lengths. This can be expected since the split-gate first pinches off the channel at the middle of the confining gate. For this reason the longer wires were easier to turn off than the constrictions which also have a finite electrostatic length. The constrictions ($L \simeq 0.0$ μm) showed a more negative V_{t1D} than the wires and

did not display the critical width (within our experimental resolution of 0.1 μm) observed in the wires.

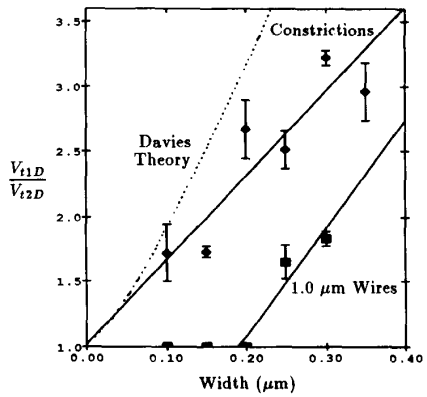

Figure 10. The ratio of the 1D threshold voltage, V_{t1D}, to the 2D threshold voltage, V_{t2D}, as a function of the separation between the confining gates for constrictions and 1.0 μm long quantum wires.

The experimental results for the constrictions and the 1.0 μm wires are summarized in Fig. 10 which plots the ratio between the 1D threshold voltage and the 2D threshold voltage as a function of width for the two lengths. Each data point represents an average over several devices.

Discussion

Our experiments reveal that both wire length and width impact the existence and the onset of the 1D regime in split-gate FETs. Davies [8] has theoretically studied this problem and concluded that the ratio V_{t1D}/V_{t2D} is only a function of the geometry of the problem (wire width and depth from the surface of the 2DEG). Davies work, however, did not include the impact of wire length, *i.e.* only infinitely long wires were modeled. These results should then be applicable to our $L \geq 0.5$ μm devices. Davies theoretical curve is plotted in Fig. 10 overlapping the plots of our experimental results.

A distinct difference between Davies theoretical results and our experimental results is observed in that Davies results do not predict the *critical width* that we experimentally obtain. The slope of V_{t1D}/V_{t2D} *vs.* W that Davies predicts, however, is close to our experimental observations. The fact that Davies predictions are close to V_{t1D}/V_{t2D} for our constrictions is a coincidence since his theory does not apply in this regime.

There are a number of possibilities as to the origin of the critical width in the 1D regime in split-gate wires. A basic assumption in Davies theory is that, through gate voltage, one modulates the potential at the metal-covered semiconductor surface while the potential at the gap surface is unchanged. Due to the imperfect screening of surface states, this transition might not be abrupt. This would result in an extension of the effective electrostatic gate beyond the lithographic gate dimensions. In fact, in our experiments this extension is approximately 0.1 μm (half of the critical width). This would bring Davies theory close to our experimental results. Further work is needed to sort out this hypothesis.

The relationship between the ratio of the two threshold voltages and the length of the confining split-gates can be understood by simple electrostatic arguments. Split-gates of finite length, 0.5 μm and 1.0 μm, act as line charges while the constrictions act more like point charges. The electric fields arising from the gate voltage of a line charge drops off as $\frac{1}{r}$ while the field of a point charge drops off as $\frac{1}{r^2}$. Therefore the constrictions are harder to turn off than the longer wires.

Conclusion

We have established relationships between the dimensions of the split-gate FET and the existence of 1D transport. The effect of length and width of the confining gates on 1D transport was studied. In $L = 1.0$ μm FETs, we have observed a critical width of 0.2 μm for the confining split gates below which 1D transport cannot be supported. Constrictions did not reveal a critical width to within our experimental resolution. This information can be used in designing future devices based on 1D electron channels.

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